Correlation of single trapping and detrapping effects in drain and gate currents of nanoscaled nFETs and pFETs

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***Abstract* — The correlation of discrete gate and drain current fluctuations is revealed in nanoscaled SiON pFETs and nFETs, demonstrating that discrete trapping and detrapping events in the same single states are responsible of both I_D and I_G random telegraph noise (RTN). The high and low gate current I_G-RTN levels are independent of temperature but the switching rates are thermally activated indicating that the trapping and detrapping events are consistent with nonradiative multiphonon theory.**

***Index Terms* — Random Telegraph Noise RTN, Gate current RTN, I_G-RTN, drain current RTN, I_D-RTN, gate leakage current, MOSFET, reliability, variability, SiON.**

I. Introduction

As a consequence of the reduction of both the gate oxide thickness and the lateral dimensions of the CMOS devices, the amount of oxide defects has decreased to a numerable level, allowing the decoupling of their collective behavior. In ultra thin gate oxide field effect transistors (FETs), discrete fluctuations of the gate leakage current are distinguishable [1], resulting in significant time-dependent variations in this important FET parameter. Likewise, in nanoscaled FETs, drain current fluctuations at inversion conditions have been recurrently reported and ascribed to trapping and detrapping events in the gate oxide [2-3].

Recently, discrete increases of the drain current, i.e. drops of the threshold voltage V_{TH}, in nanoscaled devices after gate bias temperature (BTI) stress have been seen in nFETs and pFETs with SiON and high-κ dielectrics and have been explained by the discharge of individual traps [4-9]. This effect has been described as the non-steady state case of the drain random telegraph noise I_D-RTN [4] (Fig. 1).

The correlation between the fluctuations in the drain current I_D-RTN and the gate current I_G-RTN has been pointed out by Chen *et al.* [10] for nFET devices. In this paper, we further explore the I_D-RTN and I_G-RTN correlation, not only for nFETs but also for pFETs, demonstrating that both effects are due to the charging and discharging of the same isolated defects. Consequently, we argue that the same states play a fundamental role in the two major reliability issues of CMOS technology: the threshold voltage instability and the gate leakage current (Fig. 1).

II. Devices and Experimental Setup

The transfer characteristics (I_D vs. V_G) and leakage current curves (I_G vs. V_G) were registered in different SiON pFETs and nFETs by means of Keithley 2636 SMUs. Afterward, I_D and I_G traces were simultaneously measured with a sample rate of 20ms at a target absolute gate current of 10pA. The transient characteristics of a selected nFET and a pFET were measured additionally at different gate voltages and temperatures ranging from 15 to 65ºC. The drain voltage V_D was fixed to |100|mV during all the characterizations.

The experimental V_G window that allows measuring simultaneously I_D-RTN and I_G-RTN is limited to a relatively narrow interval. This is because the largest I_D-RTN fluctuations with respect to I_D are observed at low V_G (close to V_{TH}) but I_G-RTN amplitude increases with V_G. This point

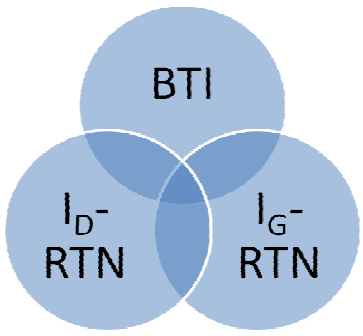

Fig. 1: Same states are argued to be responsible for the threshold voltage V_{TH} instabilities observed at stationary and dynamic bias conditions (I_D-RTN and BTI, respectively) [4] and the leakage current I_G fluctuations (I_G-RTN).

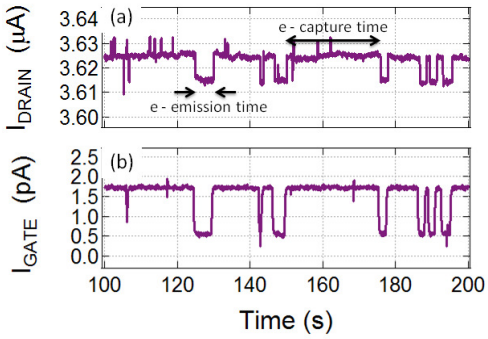

Fig. 2: (a) I_D and (b) I_G traces simultaneously registered by means of Keithley 2636 SMUs on a nanoscaled 90×35nm^2 2.3nm-EOT SiON nFET showing synchronized fluctuations and demonstrating the correlation between I_D and I_G RTN. The lower level of the drain current corresponds to the periods when the trap is negatively charged. Therefore, the emission and the capture times are obtained from the periods when the current is at low and high levels, respectively.

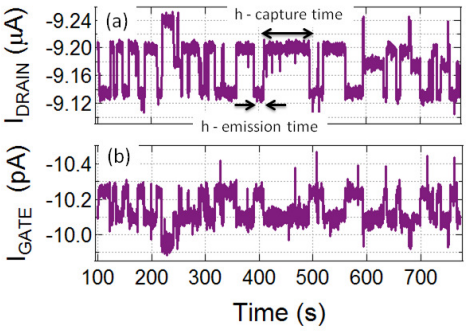

Fig. 3: The correlation between (a) I_D and (b) I_G RTN is also shown for SiON pFETs. However, it is observed that the high I_G level corresponds to the low I_D value. The low level of the drain current corresponds to the periods when a hole is trapped. The emission and capture times are obtained from the periods when the drain current is at low and high values, respectively.

is extended later on.

Nanoscaled devices with an area of W×L=70×35nm^2 were studied. 2.3nm-EOT SiON pFETs and nFETs were selected because they fulfill two essential requirements for this experiment: significant leakage current with a sufficient EOT.

(1) The thick EOT ensures high average I_D-RTN amplitude since ΔI_D is approximately proportional to the EOT of the stack [11-13]. So the thicker the gate oxide is, the larger the average I_D-RTN amplitude gets.

(2) However, the leakage current I_G decays exponentially with increasing the physical thickness of gate oxide. Therefore, thin oxides are mandatory to observe a sufficient gate current with our experimental setup.

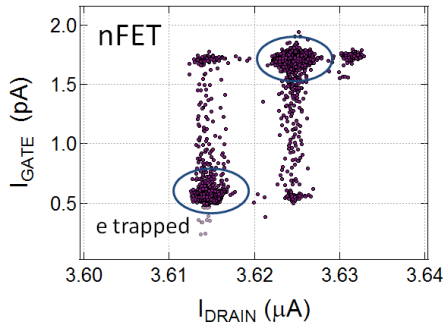

Fig. 4: Gate current I_G vs. drain current I_D from Fig. 2 for fixed sampling times. The correlation between both variables becomes more evident. The high I_G level corresponds to the high I_D value. The events registered outside of the expected clusters are due to the mismatch in the synchronization of the measured currents at the two terminals.

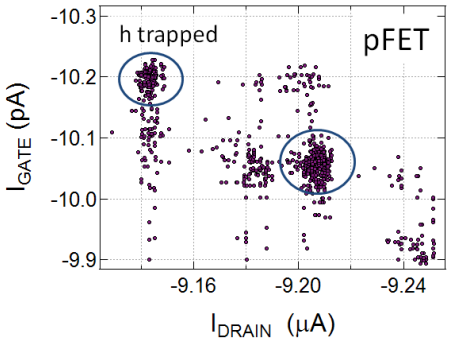

Fig. 5: Inverse correlation between I_D and I_G is found for the pFET (Fig. 3) with respect to the nFET case (see Fig. 4). The high I_G level corresponds to a low I_D value.

III. Correlation of Drain and Gate Current Random Telegraph Noises

Figures 2 and 3 show the I_G and I_D traces registered in parallel for a representative nFET and pFET, respectively. An *evident correlation of I_G-RTN and I_D-RTN* is observed for both cases. For the nFET, a high drain current level corresponds to a high gate current level. However, the correlation is inverted for the pFET, a high drain current level corresponds to a low gate current level. The correlation between I_D and I_G fluctuations is more evident in Figs. 4 and 5 where the gate current I_G is plotted vs. the drain current I_D at each measured time-stamp. Note that two main clusters appear in the graphs. The events registered outside of the expected clusters are due to the mismatch in the synchronization of the measured currents at the two terminals.

Figs. 2 and 3 also show that the absolute value of the drain current fluctuations ΔI_D is orders of magnitude larger than the I_G-RTN amplitude ΔI_G. Therefore, no direct conduction paths are formed between the gate and the source/drain terminals as it is the case of I_D-RTN and I_G-RTN after soft breakdown or in RRAM filaments inside a transistor [14-16].

The large I_D-RTN signals observed in Figs. 2 and 3 are due to the non-uniform potential at the Si/SiON interface caused by the random distributions of dopants in the channel and charged traps in the dielectric, as illustrated in Fig. 6. The potential fluctuations produce variations of the inversion charge density and, consequently, preferential conduction paths from the drain to the source. The charge and discharge of single oxide traps over critical positions of the conduction paths can produce significant fluctuations of the drain current

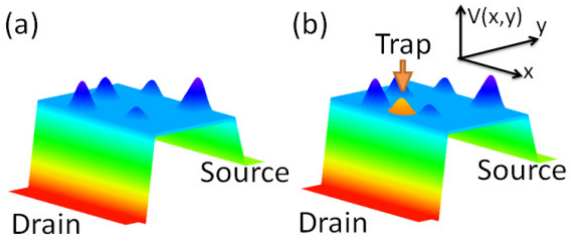

Fig. 6: (a) Percolation paths are formed between the drain and the source in a nanoscaled device due to potential fluctuations caused by random dopant distribution and charged gate oxide traps. (b) An additional charged trap may block a percolation path, causing a significant decrease of I_D.

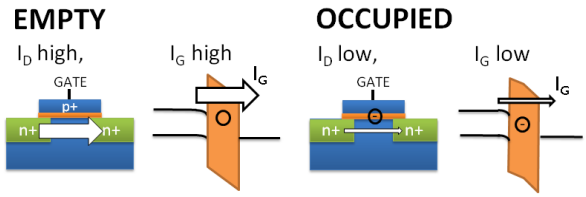

Fig. 7: According to the model presented in [14,15], *electron trapping* in the gate oxide of a nFET may cause a significant drop of I_D electron current and a simultaneous *raise of the oxide conduction band*, reducing the electron tunneling probability and therefore the gate leakage current.

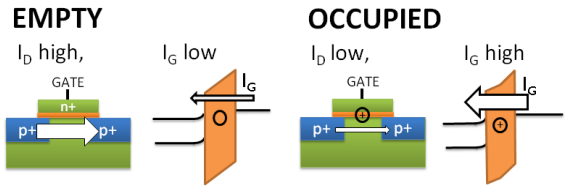

Fig. 8: *Hole trapping* in the gate oxide of a pFET may also cause a significant drop of $|I_D|$ hole current and a simultaneous *lowering of the oxide conduction band* thus increasing the electron tunneling probability and therefore the gate leakage current [14,17].

[11-12]. On the other hand, the I_G fluctuations may be explained either by (1) the local increase/decrease of the electron tunneling barrier [14,17] produced by an electron/hole trapped in the dielectric, as illustrated in Figs. 7 and 8 or by (2) trap assisted tunneling through defects with two possible states and, therefore, two possible pairs of emission and capture times [18-19].

(1) For the nFET in Figs. 2 and 4, the lower I_D level corresponds to the case of an electron trapped in the dielectric, and a sudden increase of the current is detected at the very moment that the electron is emitted. Figs. 2 and 4 show an important decrease of the leakage current when the electron is trapped. A higher leakage current is detected when the trap is discharged.

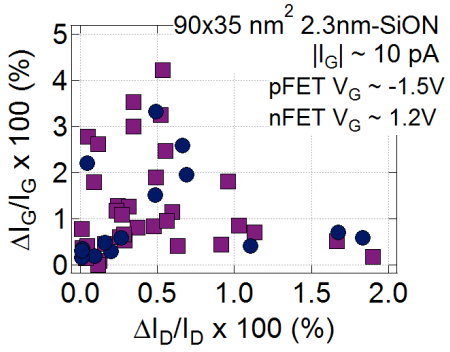

Fig. 9: No obvious correlation is found between the I_G-RTN and I_D-RTN amplitudes for nFETs or pFETs showing simultaneous I_G and I_D RTN. Low $\Delta I_D/I_D$ ratios are measured due to the large V_G used in the measurement (see Fig. 10).

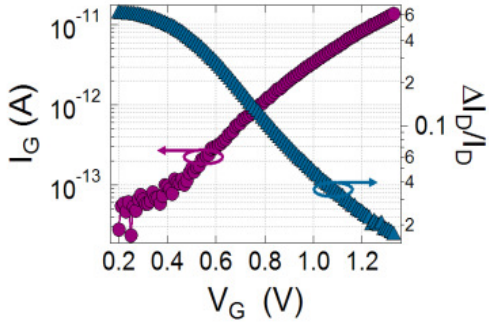

Fig. 10: (Left axis) Leakage current I_G and (right axis) $\Delta I_D/I_D$ for one of the 2.3nm-EOT SiON nFETs under study as a function of the gate voltage V_G. The $\Delta I_D/I_D$ curve is obtained by considering a constant threshold voltage shift ΔV_{TH} of 40mV in the entire V_G range. High gate voltages are mandatory to measure a reasonable gate current I_G (left axis). However, I_D-RTN sensitivity (right axis) is reduced at high gate voltages. Consequently, simultaneous measurement of I_D-RTN and I_G-RTN is limited to a relatively narrow V_G window.

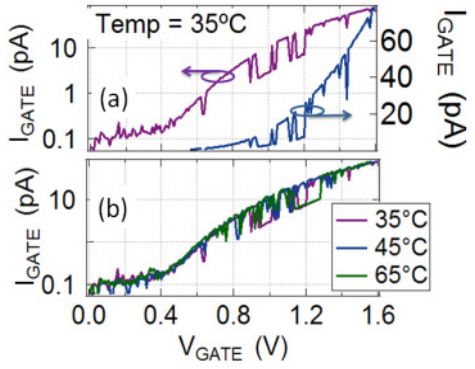

Fig. 11: (a) Charge and discharge processes are visible in the I_G-V_G curve. The vertical shift of the low and high I_G levels in log scale indicates a constant ratio between the two levels. (b) No thermal dependence of the high and low I_G envelopes is observed. However, *I_G current is modulated by a thermally activated process of trapping/detrapping of charge.*

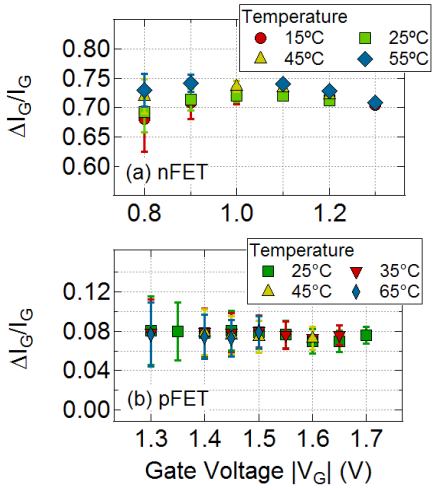

Fig. 12: Realtive gate current RTN ($\Delta I_G/I_G$) amplitude as a function of gate voltage V_G at different temperatures for (a) the same nFET as shown in Fig. 11 and (b) for a pFET.

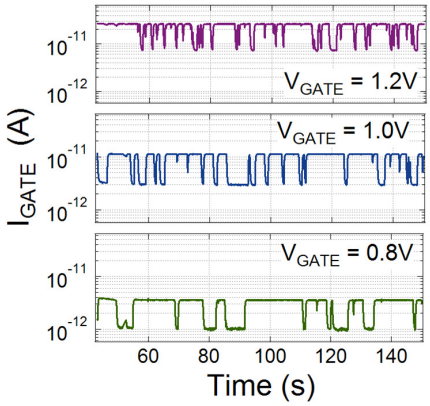

Fig. 13: High-to-low I_G ratio is constant in the range of scanned V_G, but emission and capture processes become more frequent with increasing V_G for the trap observed at Fig. 11.

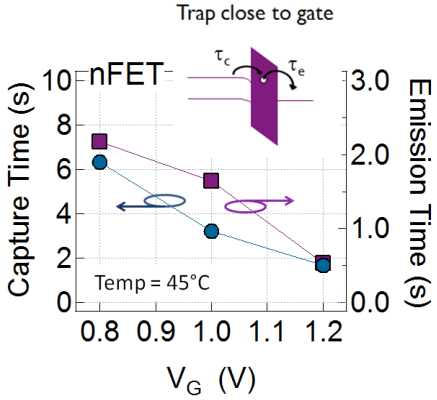

Fig. 14: Capture τ_c and emission τ_e times extracted at different V_G's for the nFET shown in Fig. 13. For this particular case, a decrease of τ_c is observed with V_G increasing. Conversely to NBTI experiments [20], τ_e decreases with V_G. This trend suggests the possibility of charge exchange also with the gate as sketched in inset.

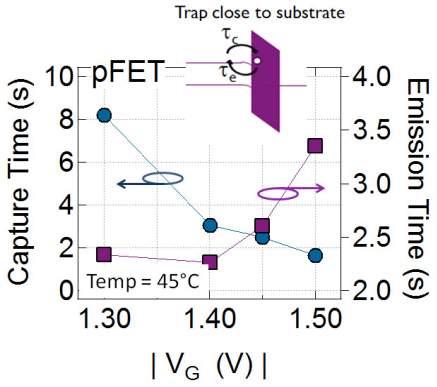

Fig. 15: τ_e and τ_c follow the same trend as NBTI experiments [20-21], hinting at charge exchange with the substrate.

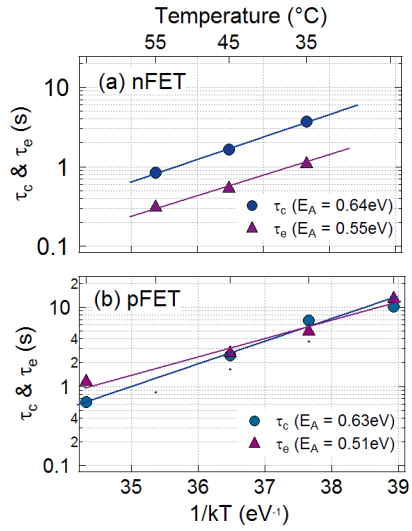

Fig. 16: Arrhenius plots of the emission τ_e and capture τ_c times for (a) an nFET at V_G = 1.2V and (b) a pFET at V_G = -1.45V show a strong temperature dependence of both parameters.

(2) For the pFET in Figs. 3 and 5, the inverse trend is observed: an I_D reduction (a hole capture) corresponds to an enlargement of I_G. Therefore the high level of leakage current is detected when the trap is positively charged as sketched in Fig. 8.

Therefore, the reverse correlation between I_G-RTN and I_D-RTN in nFETs and pFETs arises from the fact that the gate current is due to electron carriers, while the drain current is hole current for pFETs and electron current for nFETs.

At an $|I_G|$ of about 10pA, the correlation between I_D-RTN and I_G-RTN fluctuations was corroborated on 37 out of 235 pFETs and on 18 out of 308 nFETs. Fig. 9 shows the relative amplitude of the gate current RTN and drain current RTN for the devices showing simultaneously both effects. Although the number of analyzed devices is limited, the absence of devices showing simultaneously giant I_G-RTN and giant I_D-RTN is noted and, also, an approximately reciprocal relation between the amplitudes can be discerned. However, a larger sample size is necessary to draw definite conclusions.

In Fig. 9 it is also noted that $\Delta I_D/I_D$ is lower than $\Delta I_G/I_G$. This is due to the high V_G used as the sense voltage. $\Delta I_D/I_D$ reaches its maximum at low V_G values, provided that a single charge produces a constant V_{TH} shift over the entire V_G range (Fig. 10). In this experiment, however a high sense gate voltage V_G is used in order to obtain a reasonable gate current, resulting in a reduced $\Delta I_D/I_D$ ratio. On the other hand, the $\Delta I_G/I_G$ is constant in the entire V_G range, as observed in Fig. 11 and discussed in the next section. Therefore, it is feasible to observe I_D-RTN at low V_G and I_G-RTN at high V_G, limiting the possibility of simultaneously recording both effects to a narrow V_G window.

IV. Gate Current RTN

Figure 11 shows the I_G vs. V_G curves at different temperatures of a device showing giant gate current RTN. In Fig. 11, the charge and discharge processes are clearly observed during I_G-V_G tracing. Note that the high and low I_G levels are independent of temperature. The constant vertical shift between the low I_G and high I_G when plotted on a log scale, see Fig. 11(b), suggests a constant ratio between the two levels over the entire scanned V_G range. In order to further document this fact, Fig. 12(a) shows the relative amplitude $\Delta I_G/I_G$ as a function of gate voltage V_G for different temperatures. An approximately constant $\Delta I_G/I_G$ ratio is observed. These results, temperature independent gate current and constant ΔI_G ratio were also observed for the trap studied in a selected pFET device. Fig. 12(b) shows that the $\Delta I_G/I_G$ ratio is constant and independent of temperature and gate voltage. These facts are in agreement with both the charge blocking area model [14, 17] and the two state defect approach [18-19].

Fig. 13 shows the I_G traces registered on the same device as in Fig. 11 for different V_G's. A higher probability of emission and capture of charge, i.e. shorter capture τ_c and emission τ_e times, is observed with increasing V_G for the single trap under study. The emission and capture times are stochastic variables that follow an exponential distribution (not shown) [3]. This exponential distribution for the emission and capture times has been also reported for I_D-RTN and BTI experiments on nanoscaled devices [20-21]. Fig. 14 shows the average values of the emission τ_e and capture times τ_c obtained as a function of the gate voltage V_G from the traces presented in Fig. 13. As expected τ_c, decreases with V_G, thus, the capture probability increases. Interestingly, τ_e also decreases. This may point to electron capture from the silicon channel and emission into the polysilicon gate, as depicted in the inset of Fig. 14. Fig. 15 shows the τ_c and τ_e values as a function of V_G for a trap in a pFET. In this case, the capture time decreases with increasing the gate voltage and the emission time increases. This is the expected BTI behavior: reduction of τ_c and increase of τ_e with increasing V_G [20-21].

These different behaviors suggest the possibility of charge exchange not solely with the silicon channel (inset of Fig. 15) as assumed in BTI experiments, but also with the polysilicon gate (inset of Fig. 14). It may indicate that V_{TH} shifts observed in TDDS experiments [20] are due to traps placed close to the silicon interface, where the probability of charge emission to the gate is limited even at high (stress) gate voltages.

The *thermal activation of the charging and discharging* processes is demonstrated by repeating the experiment at different temperatures. Fig. 16 shows the Arrhenius plot of the capture and emission times for the traps in Figs. 14 and 15. For temperatures above 55 and 65°C the characteristic times for the traps in the nFET and the pFET, respectively, drop below the 1 second range, making the extraction of the emission and capture times difficult (the sampling time of our setup is 20ms). Activation energies E_A of about 0.6eV are extracted for the capture and the emission times. These large activation energies disagree again with the elastic tunneling theory extensively used for trapping/detrapping processes in the operation model of charge trap memories [22], spatial depth profiling [23], and I_D-RTN [24]. Moreover, these energies are similar to the ones obtained in BTI experiments on nanoscaled devices [5-7, 20-21]. We therefore conclude that the same traps are responsible for both effects, but traps placed closer to the gate present a higher probability of being emptied during stress, thus, not contributing to BTI.

V. Conclusions

In conclusion, the one-to-one correlation between I_G-RTN and I_D-RTN has been shown for both nFETs and pFETs. This correlation demonstrates that the same traps are responsible for both effects. Gate leakage current is modulated by a thermally activated process of trapping and detrapping of charge. I_G-RTN can be extremely useful as a fast technique to gather information on dielectric traps in ultra low EOT gate oxide capacitors without the necessity of full transistor processing.

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