State Drift Optimization of Memristive Stateful IMP Logic Gates

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INTRODUCTION

The use of memristive devices for new computational architectures enables the application of the same elements as latches and logics, which can significantly enhance the existing computational resources, open new computational paradigms, and reduce costs. Recently, the realization of material implication (IMP) in a gate, cf. Fig.1(a), including a conventional resistor (R_G) and two TiO2 switches (M_P and M_Q) was reported to enable stateful logic operations, where the memristive switches serve simultaneously as logic gates [1]. The switching dynamics in TiO_2 memristive devices is, however, significantly affected by electron tunneling through a varying width tunnel barrier w [2], cf. Fig.1(b), which strongly influences the electrical properties of logical operations. In particular, the resistance at high voltages important for digital applications is considerably reduced, cf. Fig.2. Thus, the linear memristive model can only be used for low voltage analog circuits, while nonlinear modeling has to be performed for digital design.

The design procedure of the IMP gate involves determining the proper values of the circuit parameters (R_G, V_{SET}, and V_{COND}) for optimally describing logic behavior. The only existing design procedure [3], based on a linear memristor model, is inconsistent with experimental data.

IMP GATE OPTIMIZATION

In this work we propose a new design procedure for reliably describing logic behavior at a desired frequency based on a switching dynamic model of TiO_2 memristors [2], for which the complex switching dynamics arising from ionic motion and modulation of an effective tunneling resistance with voltage and current is properly taken into account.

The initial logic states of the M_P and M_Q (p and q) are the inputs of the IMP gate. The final logic state of M_Q (q') after performing the IMP (including simultaneous application of two negative pulses, V_{SET} and V_{COND}) is the output of the gate. The only initial state which involves a switching (ON-switching of M_Q) is State 1 ($q \longleftarrow 1$). The voltages applied during the IMP logic operation tend to reduce the tunneling thickness w from w_{off} to w_{on}, thus affecting the memristance which is the error source (Fig.3). This phenomenon is named state drift (SD) [3].

The nonlinear memristor model helps reducing this error. Indeed, if the window $\Delta V_Q = |V_{Q1}-V_{Q3}|$ is large, the error accumulated on M_Q is minimal. We chose R_G at fixed different V_{COND} (V_{SET} is constant) to boost ΔV_Q. As follows from Fig.4, R_G corresponds to the maximum and is thus uniquely defined by the memristor's properties, V_{COND} and V_{SET}.

ΔV_Q increases with increased V_{COND} minimizing the SD on memristor M_Q. However, an increase in V_{COND} results in an increasing error on memristor M_P, because it tends to switch, when it should not. There is an optimum V_{COND} (Fig.5) for which the SD is minimum. Thus, V_{COND} and R_G are determined at any V_{SET}.

Fig.6 shows only a slight increase of V_{SET} with the IMP switching time decreased, in contrast to the linear dynamic models. This results in large power consumption benefits at higher IMP speed.

The work is supported by the European Research Council through the grant#247056 MOSILSPIN.

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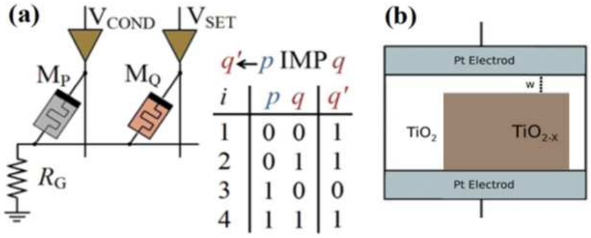

Fig. 1. (a) The IMP gate and the IMP truth table [1]. (b) The TiO_2 memristive device cross section [2].

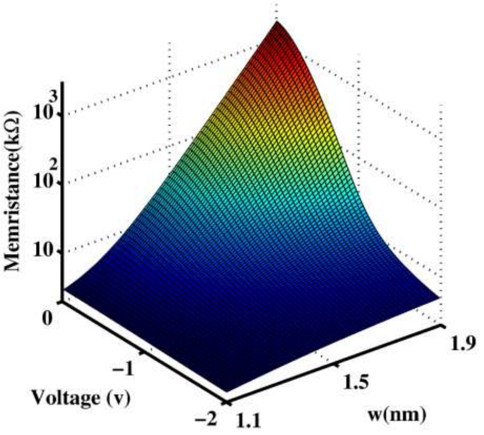

Fig. 2. The memristance as a function of *V* and *w*. A 0.4nm modulation in *w* (w_{off}=1.85nm and w_{on}=1.45nm [2]) provides a resistance ON-OFF-switching ratio about 40 at 0.2V readout voltage.

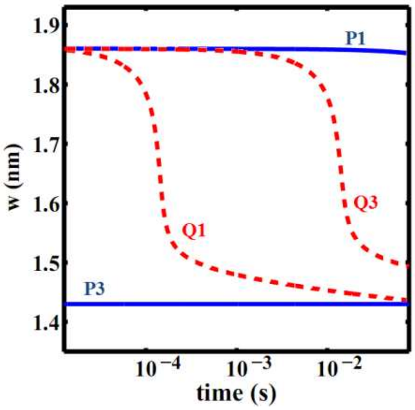

Fig. 3. The dynamic behavior of *w* in M_P and M_Q during the IMP operation plotted for State 1 and State 3. A high enough voltage modulation on M_Q (ΔV_Q=$|V_{Q1}$-$V_{Q3}|$) and also a high enough $V_{S,C}$ (=$|V_{SET}$-$V_{COND}|$) are needed to ensure the IMP correct logic behavior in State1 and State 3, respectively.

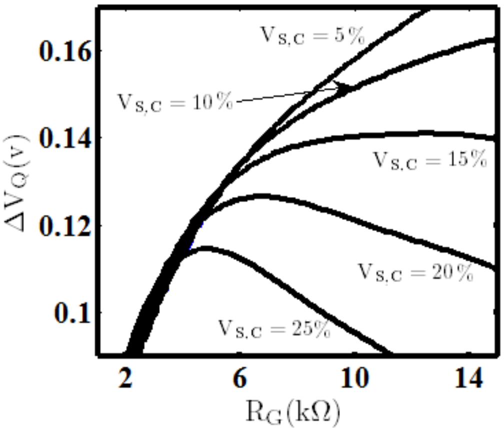

Fig. 4. R_G is chosen to maximize ΔV_Q and thus minimize the error on M_Q for fixed $V_{S,C}$ ($V_{S,C}$ = (V_{SET}-V_{COND})/V_{SET}).

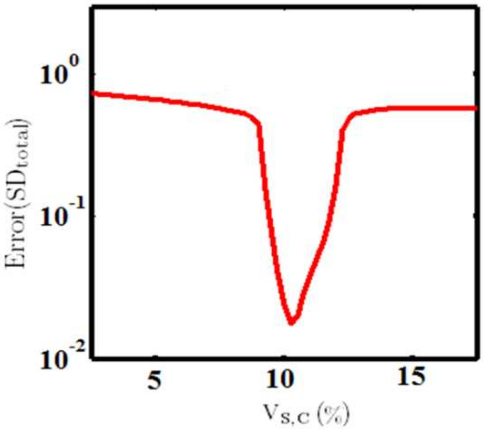

Fig. 5. The total error (state drift) as a function of $V_{S,C}$. The value of V_{SET} is chosen based on the minimum error obtained.

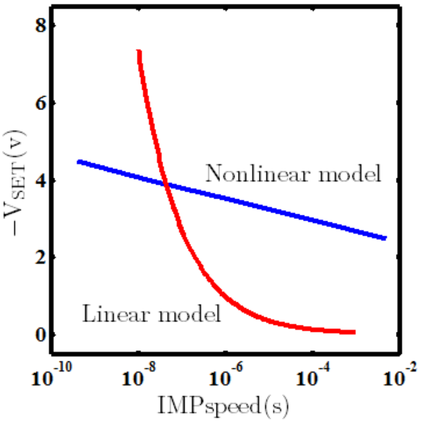

Fig. 6. (a) Dependence of V_{SET} on the IMP speed. The absolute value V_{SET} increases with switching time decreased. However, the decrease is much slower as compared to the one obtained with the linear memristor model.