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Physics Procedia 25 (2012) 99 – 104

Physics Procedia

2012 International Conference on Solid State Devices and Materials Science

Modeling Emerging Non-volatile Memories: Current Trends and Challenges

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Abstract

An important task of micro- and nanoelectronics is establishing a new universal memory type in a near future. Unlike DRAM and flash memories a new universal memory should not require electric charge storing, but alternative principles of information storage. For successful application a new universal memory has to be non-volatile and must also exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, and a simple structure. Several alternative principles of information storage are available. We focus on two memory technologies based on the resistance change principle, RRAM and the spin transfer torque (STT) RAM, which are the most promising candidates for future universal memory. We present a brief overview of the current state-of-the-art of these technologies and outline future trends and challenges from the perspective of modeling and simulation of the switching process.

Keywords: emerging memory; non-volatile memory; RRAM; STTRAM

1. Introduction

In modern microelectronic devices the dominant memory types are DRAM, SRAM, and flash memory. These types of memory store data as a charge state. For many decades these memory technologies have been successfully scaled down to achieve higher speed and increased density of memory chips at lower bit cost [1]. However, memories based on charge storage are gradually approaching the physical limits of scalability and conceptually new types of memories based on a different storage principle are gaining

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1875-3892 © 2012 Published by Elsevier B.V. Selection and/or peer-review under responsibility of Garry Lee
doi:10.1016/j.phpro.2012.03.056

momentum. Apart from good scalability, a new type of memory must also exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, and a simple structure [2]. In addition, non-volatility is highly desirable to preserve the data, when the power is off.

Alternative principles of information storage include the resistive switching phenomenon in insulators, the effect of changing the magnetoresistance, the domain wall motion along magnetic racetracks, the ferroelectric effect, and others. Some of the technologies based on these new storage principle are already available as product [such as phase change RAM (PCRAM), magnetoresistive RAM (MRAM), and ferroelectric RAM (FeRAM)], others only as prototype [such as carbon nanotube RAM (CNRAM), copper bridge RAM (CBRAM), spin-torque transfer RAM (STTRAM), and resistive RAM (RRAM)], while racetrack memory is available only as a memory concept.

From these technologies the two most promising candidates for future universal memory are RRAM and STTRAM. Currently, RRAM, CBRAM, and STTRAM have been demonstrated on 4Mb [3,4] and 64Mb [5] test chips, respectively. These technologies could be in mass production within 5-10 years [6].

In this paper we demonstrate how modeling approaches help creating a universal non-volatile memory based on RRAM and STTRAM, describe the current state-of-the art of these technologies, and highlight future trends and challenges.

2. Memories based on resistance change

Resistive change memory possesses the simplest structure in the form of metal-insulator-metal (MIM) sandwich. The electrical conductance of the insulator can be set at different levels by the application of an electric field, and this phenomenon can be used in memory devices. The state with high resistance (HRS) can mean logical 1 and the state with low resistance (LRS) can mean logical 0 or vice versa depending on the technology. The resistive switching phenomenon is either bipolar or unipolar, based on the voltage polarity of the SET and RESET processes. The switching operation is called bipolar, when the SET to LRS occurs at one voltage polarity and the RESET to the HRS on the reversed voltage polarity. The switching operation is called unipolar, when the switching procedure does not depend on the polarity of the write voltage. The resistive switching phenomenon is observed in different types of insulators, such as metal oxides, perovskite oxides, chalcogenide materials, and others. Three technologies of memory, CBRAM, PCRAM, and RRAM are based on the resistive switching. CBRAM, also called in the literature as memory with an Electrochemical Metallization (ECM) cell or Programmable Metallization Cell (PMC), is based on solid state electrolyte in which mobile metal ions can create a conductive bridge between the two electrodes under the influence of an electric field. The source of mobile metal ions is one of the electrodes, which is made from an electrochemically active metal, such as Ag, Cu, or Ni. Electrochemically inert metals, such as Pt, Ir, W, or Au are used for the second electrode [7]. PCRAM employs the difference in resistivity between crystalline and amorphous phases of a chalcogenide compound [8].

RRAM is based on metal oxides, such as NiO [9], CuO [10], TiO_x [11,12], HfO_2 [13], ZnO [14], WO [15], on the heterostructure of metal oxides [16], and perovskite oxides. The prototypes of RRAM shown by NDL [15] and Samsung [16] have already surpassed the scaling limit of charge-based storage memories. Despite this, a proper fundamental understanding of the RRAM switching mechanism is still missing, hindering further development of this type of memory. First and foremost, one needs a better understanding and control of physical SET/RESET processes by development of accurate models [6].

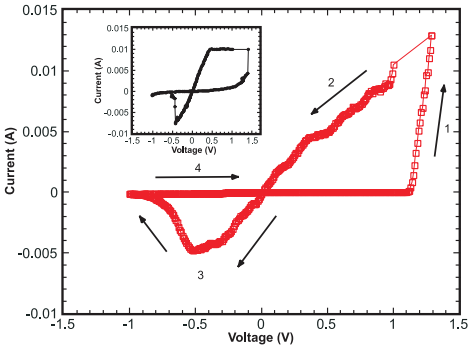

Figure 1. I-V characteristics showing the hysteresis cycle obtained from the stochastic model [19]. The inset shows the hysteresis cycle for M-ZnO-M from [14].

In the literature several physical mechanisms/models based on either electron or ion switching have been suggested for the explanation of resistive switching in perovskite oxides and in metal oxides with bipolar and unipolar switching. One of the first models of resistive switching proposed was a domain based model [17]. The insulating medium contains metallic domains, which inexplicitly correspond to charge traps in the real system such as dopants, vacancies, metallic clusters, and nanodomains. It is assumed in this model that there are just three types of domains. The top and bottom domains are taken to be smaller than the middle ones. This differentiation might be justified by the different electronic states close to the interfaces of the metal electrodes. Electrons move around by hopping between domains as well as between a domain and an electrode only, when an external voltage is applied. Resistive switching is explained on the basis of the filling and desolating these domains.

In [18] the resistive switching behavior is associated with the formation and rupture of a conductive filament (CF). The CF is formed by localized oxygen vacancies *V*. The conduction is due to electron hopping between these *V*. Rupture of a CF is due to a redox reaction in the oxide layer under a voltage bias which is possible after a formation of a depleted region with low electron occupation.

In [19] the temperature dependence of the site occupations in the low occupation region is analyzed. The results indicate that the decrease in switching time with increasing temperature reported in [18] may stem from the increased mobility of oxide ions rather than from the reduction in occupations of *V* in the low occupation region. These results demonstrated the necessity to include the dynamics of oxygen ions. For modeling the resistive switching by Monte Carlo techniques the dynamics of oxygen ions and electrons in an oxide layer in [19] was described as follows: formation of *V* by moving oxygen ions to an interstitial position; annihilation of *V* by moving an ion to *V*; an electron hop into a vacancy from an electrode; an electron hop from a vacancy to an electrode; an electron hop between two vacancies. The hopping rates for electrons are given in [19].

Figure 1 shows the RRAM switching hysteresis cycle. The simulated cycle is in agreement with the experimental cycle from [14] shown in the inset. The interpretation of the RRAM hysteresis cycle obtained from the stochastic model is as follows. If a positive voltage is applied, the formation of a CF begins, when the voltage reaches a critical value sufficient to create a vacancy by moving an oxygen ion to an interstitial position. The formation of the CF leads to a sharp increase in the current (Fig.1, Segment 1) signifying a transition to a state with low resistance. When a reverse negative voltage is then applied, the current increases linearly, until the applied voltage reaches the value at which an annihilation of *V* is triggered by means of moving an ion to *V*. The CF is ruptured and the current decreases (Fig.1, Segment 3). This is the transition to a state with high resistance.

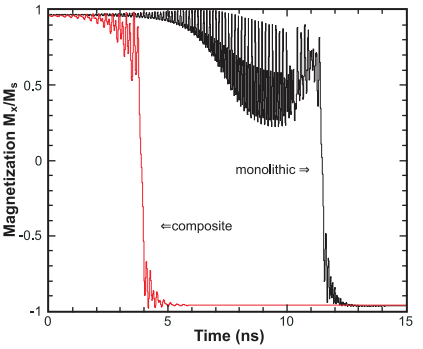

Figure 2. The switching process for an MTJ with composite and monolithic free layer for a pinned layer thickness of 10nm.

3. Magnetic memories: MRAM and STT-MRAM

Magnetic memory technologies include such types of memories as MRAM, STTRAM, and racetrack memory.

Racetrack memory [20] is currently available only as a concept. Only recently a demonstration of racetrack memory integrated with CMOS was reported [21]. We therefore focus our attention on MRAM and STTRAM in the following. The basic element of an MRAM is a magnetic tunnel junction (MTJ), a sandwich of two magnetic layers separated by a thin non-magnetic spacer. While the magnetization of the pinned layer is fixed due to the fabrication process, the magnetization direction of the free layer can be switched between the two states parallel and anti-parallel to the fixed magnetization direction. Switching in MRAM is performed by applying a magnetic field. In contrast to field-driven MRAM, STTRAM does not require an external magnetic field. Switching between the two states occurs due to the spin-polarized current flowing through the MTJ. The spin-polarized current is only a fraction of the total charge current. Therefore, high current densities are required to switch the magnetization direction of the free layer. These densities are, however, one to two orders of magnitude lower than those needed for the current-induced domain wall motion in racetrack memory [20]. This makes the STTRAM technology attractive for applications, including recently proposed domain wall motion by the field-like component of the spin torque [22].

The reduction of the current density required for switching and/or the increase of the switching speed are the most important challenges in this area [23]. Several strategies have been proposed to decrease the switching time below a few nanoseconds. Measurements [24] showed a decrease in the critical current density for a penta-layer magnetic tunnel junction with the two pinned magnetic layers in anti-parallel configuration compared to the three-layer MTJ. It follows that in the anti-parallel configuration of the fixed layers the spin currents from either of the pinned layers exert torques on the free magnetic layer in the same direction (full torque is the sum of the individual torques), which explains the decrease in the critical current density observed. An even more pronounced decrease of the switching current density is predicted by simulating the switching process in a penta-layer structure with a composite free layer [25]. The micromagnetic simulations are based on the magnetization dynamics described by the Landau-Lifshitz-Guilbert-Slonczewski equation. The Slonczewski's expressions [26] and [27] for the torque are used in a MTJ with a metal layer and with a dielectric layer between the ferromagnetic contacts, correspondingly. In the penta-layer structure the two spin torques are acting independently on the two opposite interfaces of the free ferromagnetic layer, provided its thickness is larger than the scale on which the electron spins entering into the ferromagnet become aligned to the ferromagnets' magnetization. The local effective field is calculated as a sum of the external, anisotropic, exchange, thermal, Ampere,

magnetostatic coupling between the pinned layers and the free layer, and demagnetizing field. The temperature dependence is modeled through a thermal field [28]. The structure studied is CoFe/spacer(1nm)/Py(4nm)/spacer (1nm)/CoFe (Py is $Ni_{81}Fe_{19}$) with an elliptical cross-section 90nm x 35nm. The system with a composite ferromagnetic layer is obtained by removing a central stripe of 5nm width from the monolithic free layer.

Figure 2 illustrates a substantial decrease of the switching time in the penta-layer structure with the composite free layer, for the same current density j=10MA/cm^2. The magnetostatic field causes the magnetization to tilt out of the XY plane. The non-zero angle between the fixed magnetization and the magnetization in the free layer results in the enhanced spin transfer torque, when the current starts flowing. In the case of the monolithic structure, however, the torque remains marginal in the central region, where the magnetization is along the X axis. As the amplitude of the end domains precession increases, the central region experiences almost no spin torque and preserves its initial orientation along the X axis, thus preventing the whole layer from alternating its magnetization orientation. This is, however, not the case when the central region is removed in the composite structure and the end domains become virtually independent. Due to the removal of the central region which represented the bottleneck for switching in the monolithic structure the shape anisotropy energy is decreased. However, its value is still sufficiently large for guaranteeing the thermal stability at operation conditions. Larger torques allows using lower current densities for switching.

4. Conclusion

Charge-based memory scaling will be at risk as technology scales down to 20nm, and conceptually new types of memory based on a different storage principle are gaining momentum. We demonstrated that RRAM and STTRAM are the most promising candidates for future universal memory. In particular, RRAM cells have already surpassed the scaling limits of charge-based storage memories. Despite this, a proper fundamental understanding of the RRAM switching mechanism is still missing, hindering further development of this type of memory. Therefore, a better understanding and control of physical SET/RESET processes through development of accurate models is urgently needed. The current challenge for the STTRAM technology is to reduce the switching current density. Perpendicular MTJs with interface-induced anisotropy show potential, but still require reducing damping and increasing thermal stability. Material and structure optimization through accurate modeling and simulations is a key ingredient in successful designing of future memory cells with low power consumption.

Acknowledgments

This research is supported by the European Research Council through the grant #247056 MOSILSPIN.

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