

### An Analytical Model for MOSFET Local Oxide Capacitance

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Practically all methods for extraction of the lateral interface state density profile  $N_{it}(x)$  from charge-pumping data employ the oxide capacitance  $C_{ox}$  [1-3] as a crucial parameter. Although Lee *et al.* [2] claimed that the coordinate dependence of the capacitance  $C_{ox}(x)$  due to the fringing effect should be respected, usually  $C_{ox}$  is treated as a constant parameter of the device [3]:  $C_{ox} = \epsilon_{ox}/t_{ox}$ , (1), where  $t_{ox}$  is the oxide thickness at the center of the device and  $\epsilon_{ox}$  is the dielectric permittivity. However, the electric field non-uniformity is of special importance for the extraction of the interface state density profile after hot-carrier stress because the  $N_{it}(x)$  peak is located near the drain end of the gate [4] where the capacitor non-ideality is most pronounced.

The conformal-mapping method is most helpful for fringing the electric field in simple two-dimensional boundary problems (which is just our case) by transforming the boundary to a soluble form [5]. A series of simulations (described below) allow us to draw a conclusion that for a local oxide capacitance consideration simplified structure of interest can be used. Namely, the gate contact can be interpreted geometrically as a ray instead of more complicated corner variant. The problem with the coordinate system is shown in Fig.1. The conformal transformation in Fig.1 reduces the pristine problem to the Laplace problem between two parallel infinitely long metallic plates at different potentials. The local oxide capacitance is then defined as the ratio between the surface charge density and interface potential and can be written as parametric system

$$x = \frac{t_{ox}(x)}{\pi} (\varphi + \exp(\varphi)), \quad C_{ox}(x) = \frac{\epsilon_{ox}}{t_{ox}(x)(1 + \exp(\varphi))}. \quad (2)$$

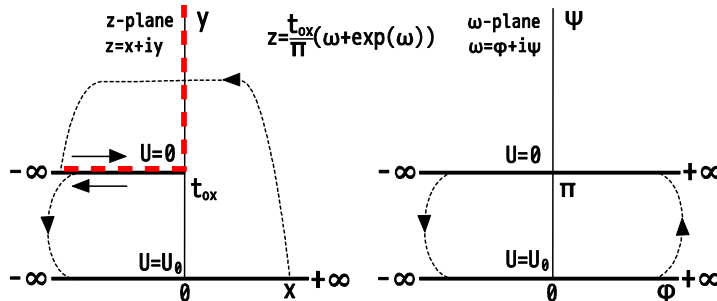
As experimental support in our work we use an n-MOSFET fabricated on a standard 0.35 $\mu$ m CMOS technology. The device architecture and the net doping profile are sketched in Fig.2. The drain-sided gate edge is the origin of the x-axis. The transistor was stressed at  $V_{ds}=6.5V$  and  $V_{gs}=2.8V$  for  $10^5s$ . The analytical solution for the potential and the electric field distribution in the oxide near the gate end following from suggested conformal map and that obtained by MiniMOS-NT [6] are presented in Fig.3. For evaluating the local oxide capacitance using device simulation we employ the method developed by Lee *et al.* [2]. The presence of a probe oxide charge ( $Q_{ot,uniform}$ ) which is set uniform leads to a local threshold voltage  $V_{th}(x)$  shift. The oxide capacitance is thus found as:  $C_{ox}(x) = -Q_{ot,uniform}/\Delta V_{th}(x)$ . A typical example of the  $V_{th}(x)$  shift induced by a uniform oxide charge density of  $10^{12} \text{ cm}^{-2}$  is shown in Fig. 1, inset. The comparison of the simulations and developed analytical approach for the local capacitance profile is presented in Fig.4. One may conclude that the obtained results are in good agreement. At the same time, the expression (1) even corrected for  $t_{ox}=t_{ox}(x)$  leads to a substantially different results. As expected, the most pronounced peculiarity is observed at the drain side of the gate where the abrupt change in the oxide thickness occurs (see Fig.1, inset). Note that an abrupt reduction in  $C_{ox}(x)$  is unphysical and such an approach should not be used. At  $x \rightarrow -\infty$  (or  $\varphi \rightarrow -\infty$ ) the obtained equation (2) asymptotically turns into well known expression for parallel-plate capacitance (1). From a detailed analysis of suggested conformal transformation we conclude that under the gate electrode the fringing effect can be neglected for distances larger than  $1.14t_{ox}(x=0)$  from the gate edge (this is reflected in Fig.4).

To extract the density of interface and oxide traps we employed analytical  $C_{ox}(x)$  profile incorporated into the scheme described in [1]. Extraction procedure output for  $10^5s$  is depicted in Fig.5. Role of the fringing effect at large stress times is obvious. Extracted  $N_{it}(x)$  and  $N_{ot}(x)$  profiles were subjected to further validation as input parameters for simulation of the transfer characteristics degradation due to the hot-carrier stress employing MiniMOS-NT. Comparison of simulated and experimental curves once again confirms applicability of developed model (see Fig.6).

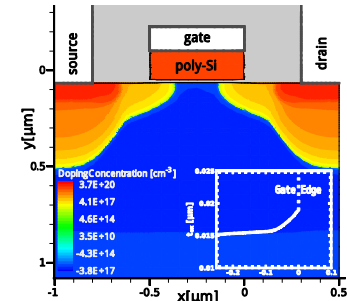
A new simple and accurate compact model for the MOSFET local oxide capacitance has been proposed. Simulations were carried out in order to investigate the scalability limits of developed approach. The spurious result produced with the model ignoring the  $C_{ox}(x)$  distribution may lead to an ambiguous picture of hot-carrier induced degradation. Our study may provide a theoretical basis and physical insights for the further refinement of conventional extraction techniques.

**References**

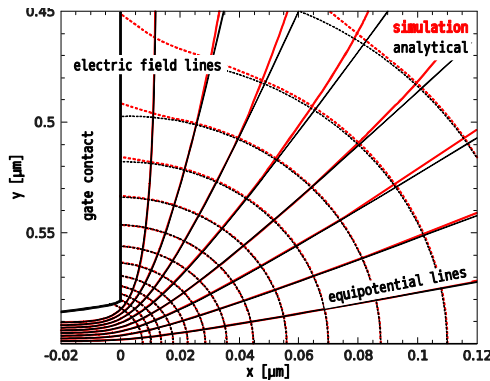
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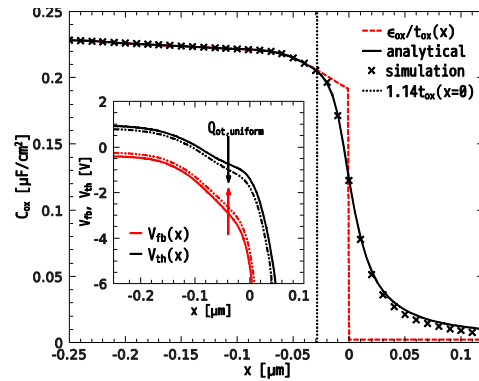
**Fig.1** The conformal transformation used to solve the gate/drain fringing problem. The complicated case of the corner gate form (red dashed line) was reduced just to a ray.



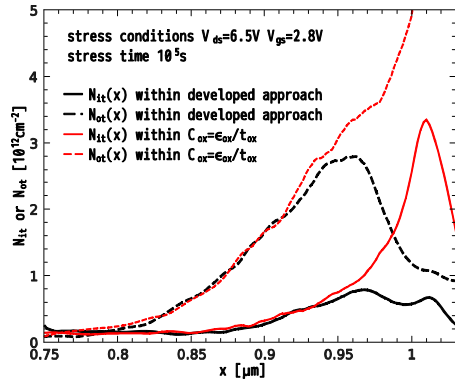
**Fig.2** The topology of n-MOSFET. Inset: the dependence of the oxide thickness vs. the lateral coordinate.



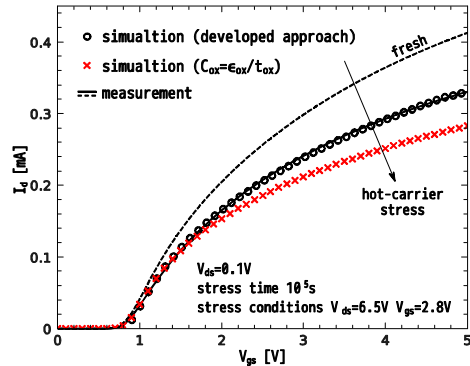
**Fig.3** The comparison of equipotential and field-lines as the analytical solution and simulated by means of device simulator MiniMOS-NT.



**Fig.4** The local oxide capacitance calculated within the approach [2] and compared with the analytical model (2). Inset: local threshold and flatband voltage distributions with uniform oxide charge profiles.



**Fig.5** Lateral distributions of  $N_{it}(x)$  and  $N_{ot}(x)$  calculated using (1) and developed expression (2) for  $C_{ox}(x)$ .



**Fig.6** The comparison of the experimental and simulated transfer characteristics for fresh and stressed devices.