

# Secondary generated holes as a crucial component for modeling of HC degradation in high-voltage n-MOSFET

Stanislav Tyaginov, Ivan Starkov,  
Oliver Triebel, Hajdin Ceric, Tibor Grasser  
Institute for Microelectronics,  
TU Wien, 1040 Vienna, Austria  
Email: tyaginov@iue.tuwien.ac.at  
Phone: +43-1-58801-36025

Hubert Enichlmair,  
Jong-Mun Park  
Austriamicrosystems AG,  
8141 Unterpremstaetten, Austria,  
Email: Jong-Mun.Park@  
austriamicrosystems.com

Christoph Jungemann  
Institute für Theoretische Elektrotechnik,  
RWTH Aachen, 52056 Aachen, Germany  
Email: Jungemann@ieee.org

**Abstract**—We propose a physics-based model for hot-carrier degradation (HCD), which is able to represent HCD observed in n-channel high-voltage MOSFETs with different channel length with a single set of physical parameters. Our approach considers not only damage produced by channel electrons but also by secondary generated channel holes. Although the contribution of the holes to the total defect creation is smaller compared to that of electrons, their impact on the linear drain current is comparable with the electronic one. The reason behind this trend is that hole-induced traps are shifted towards the source, thereby more severely affecting the device behavior.

**Index Terms**—hot-carrier degradation, Monte-Carlo, interface states, TCAD.

## I. INTRODUCTION

Hot-carrier degradation (HCD) is rather complicated to model because it includes three different but strongly connected aspects. In fact, carriers interacting with the Si/SiO<sub>2</sub> interface break Si-H bonds, thereby generating traps at/near this interface and thus the microscopic mechanisms for defect creation have to be properly described. The information on how efficiently these carriers trigger the bond dissociation process is provided by a thorough carrier transport treatment. Furthermore, these generated traps can capture carriers and thus distort the electrostatics of the transistor and degrade carrier mobility. Due to the complexity of this detrimental phenomenon, a comprehensive physics-based model is still missing and most existing HCD models are empirical [1], [2].

Recently, we have proposed a detailed HCD model which considers all these aforementioned aspects within the same framework [3], [4]. This model is able to successfully represent the linear drain current ( $I_{dlin}$ ) degradation in a wide range of stress/operating conditions in the case of a 5V n-MOSFET with a channel length of  $L_{ch} = 0.5 \mu\text{m}$  [3]. Unfortunately, the model completely fails while trying to capture  $I_{dlin}$  degradation in MOSFETs with different channel lengths with the same set of fitting parameters. In fact, for devices with  $L_{ch} = 1.2$  and  $2.0 \mu\text{m}$ , the relative change of  $I_{dlin}$  (i.e. the ratio between its absolute change and the value typical for a “fresh” device)

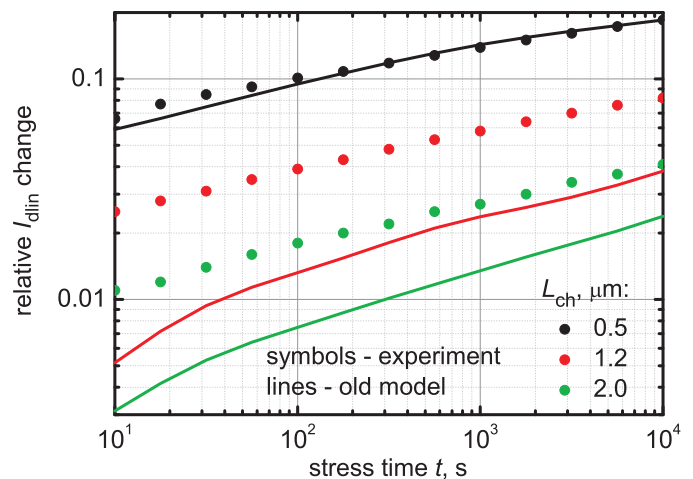


Fig. 1.  $I_{dlin}$  degradation predicted by the electron-only HCD model for different channel lengths.

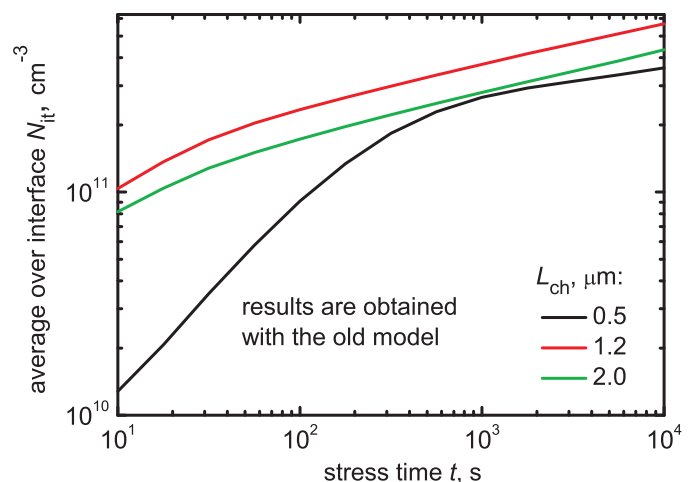


Fig. 2. The average (over the interface length) total degradation dose for different channel lengths.

predicted by the model is substantially less than that observed experimentally, see Fig. 1.

The reason is that the concentration of interface states  $N_{it}$  generated by electrons peaks outside the channel, thereby weakly affecting the device performance. Fig. 2, showing the average  $N_{it}$  (i.e. integrated over the interface and divided by the interface length), demonstrates that more severe degradation (Fig. 1) corresponds to a lower average concentration of interface states. Hence, longer devices are less sensitive to the electron-induced  $N_{it}$  and suggests that another mechanism leading to  $N_{it}$  created closer to the channel has to be responsible for this discrepancy. One may envisage that the missing contribution to the damage is triggered by secondary generated (by impact ionization) holes which are accelerated by the electric field and thus create interface states shifted towards the source. Therefore, the main purpose of this work is to refine the existing version of the model in order to make it suitable for representation of the degradation in transistors with different channel lengths within the same set of parameters.

## II. THE MODEL

The model includes three main modules: a carrier transport module, a module for modeling of microscopic mechanisms of defect creation and a module for simulation of characteristics of degraded devices [4]. The carrier transport module calculates a set of carrier energy distribution functions (DFs) at any position in the MOSFET for a particular device architecture and stress/operating conditions. For this purpose we employ the full-band Monte-Carlo device simulator MONJU [5]. Then the information about the carrier DF is used to generate  $N_{it}$  profiles. These profiles are then loaded to a circuit and device simulator MINIMOS-NT [6], which calculates the characteristics of the degraded device. We consider the superposition

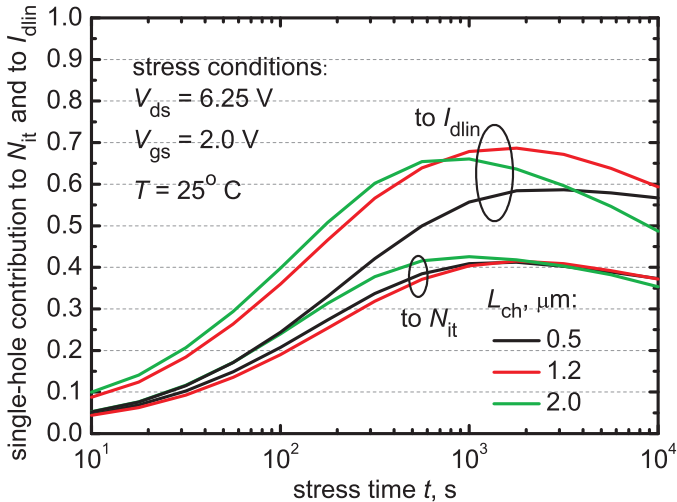


Fig. 3. The relative contribution provided by the single-hole component into the total  $I_{dlin}$  change and to the total  $N_{it}$ .

of single- and multiple-carrier mechanisms of Si-H bond-breakage (SC- and MC-processes) [3], [4]. Both mechanisms

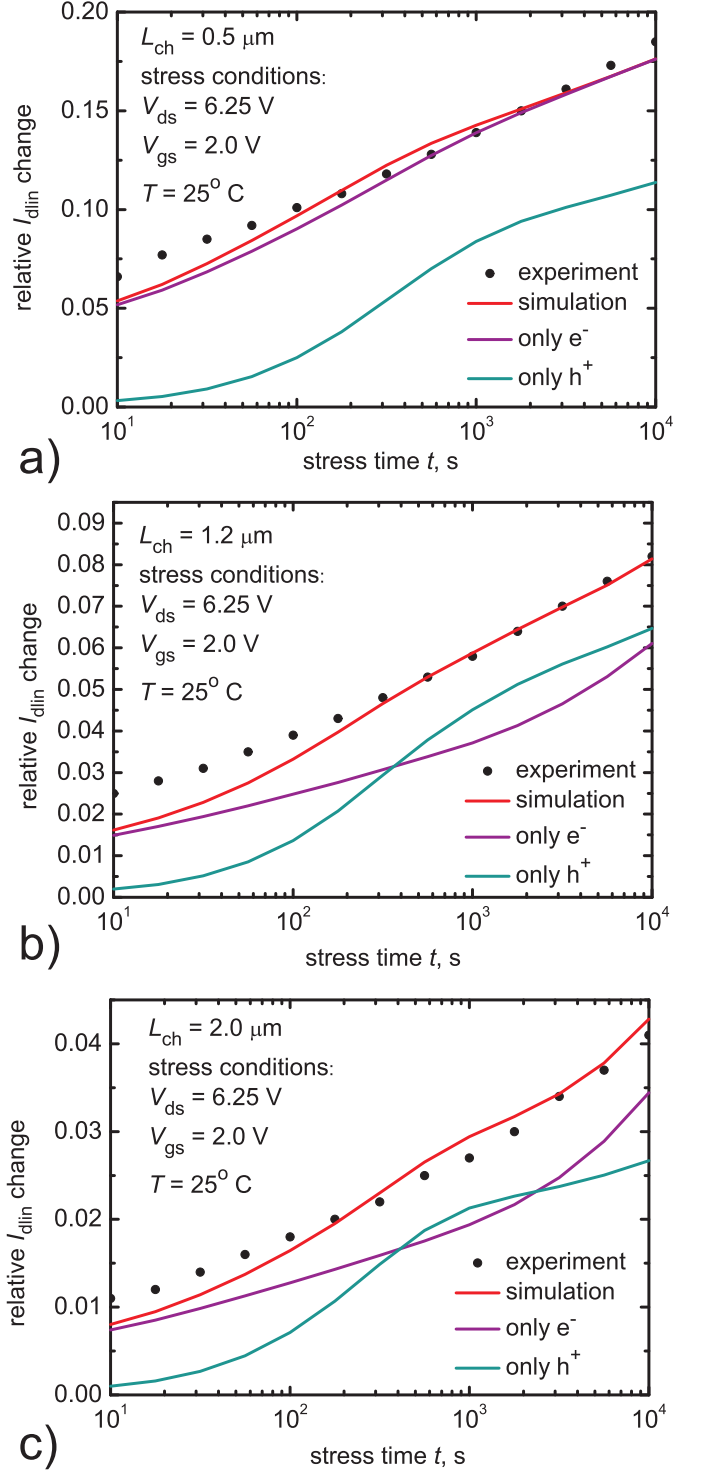


Fig. 4. The relative  $I_{dlin}$  change vs. time: experiment, simulations and contributions of electrons and holes separately for channel lengths of 0.5 (a), 1.2 (b) and 2.0  $\mu\text{m}$  (c).

are controlled by the carrier acceleration integral (AI):

$$I_{SC,e} = \nu_{SC,e} \int_{E_{th}}^{\infty} f(E)g(E)\sigma_{SC,e}(E)v(E)dE, \quad (1)$$

where  $f(E)$  is the carrier DF,  $g(E)$  the density-of-states,  $v(E)$  the carrier velocity and integration is performed over energy starting from the threshold for the Si-H bond dissociation reaction [3], [4]. Note that further in expressions (e.g. in (1)) we use acronyms SC-/MC- to distinguish two bond-breakage processes and 'e/h' to distinguish the carrier types. The previous version of our HCD model considers only electrons. In this work we also take the holes into consideration. These secondary holes are generated by impact ionization caused by the injection of hot electrons. These holes are then accelerated by the electric field towards the source, thereby creating interface states shifted with respect to the electron-induced ones. As a result, the  $N_{it}$  fraction induced by holes should be much less than their relative contribution to  $I_{dlin}$  change, Fig. 3.

For the SC-process we assume first-order kinetics to describe the SC-induced contribution to the total  $N_{it}$ :

$$N_{SC}(t) = N_0 \left[ 1 - e^{-(\nu_{SC,e} I_{SC,e} + \nu_{SC,h} I_{SC,h})t} \right], \quad (2)$$

where  $N_0$  is the concentration of "virgin" bonds and  $\nu_{SC,e/h}$  are prefactors related to electron/hole contributions.

The MC-induced portion of  $N_{it}$  is calculated:

$$N_{MC} = N_0 \left( \frac{\lambda_{emi}}{P_{pass}} \left( \frac{P_u}{P_d} \right)^{N_1} (1 - e^{\lambda_{MC} t}) \right)^{1/2}. \quad (3)$$

This expression is obtained considering the bond as a truncated harmonic oscillator (with the number of levels  $N_1$ ) characterized by phonon excitation and decay rates [1], [3], [7], [8]:  $P_u = I_{MC,e} + I_{MC,e} + \omega_e \exp(-\hbar\omega/k_B T_L)$ , and  $P_d = I_{MC,e} + I_{MC,e} + \omega_e$ . The bond-breakage process is associated with the hydrogen hopping from bonded to transport state (with the rate  $\lambda_{emi}$ ) with the backward reaction also taking place ( $P_{pass}$ ). As for the MC-process, we already showed in [3], [4] that even in the case of a high-voltage device the MC-component makes a significant contribution to the total damage. However, in this case the carrier flux is high enough, i.e.  $I_{MC,e} + I_{MC,e} \gg \omega_e$ . As a result, the prefactor  $P_u/P_d$  in (3) is equal to unity and  $N_{MC}$  is homogeneously distributed along the lateral coordinate  $x$ .

### III. RESULTS AND DISCUSSION

The model verification was performed using a series of three 5V n-MOSFETs with identical architecture differing only in channel lengths ( $L_{ch} = 0.5, 1.2, \text{ and } 2.0 \mu\text{m}$ ). Devices were fabricated on a standard  $0.35 \mu\text{m}$  technology and subjected to a hot-carrier stress at the gate voltage  $V_{gs} = 2.0$  and the drain voltage of  $V_{ds} = 6.25\text{V}$  (at  $25^\circ\text{C}$ ). The model was calibrated in a manner to represent the  $I_{dlin}$  degradation for all devices with a single set of fitting parameters and reveals a good agreement between experimental and theoretical results, see Fig. 4. AIs for electrons and holes plotted vs.  $x$  are depicted in Fig. 5.

In Fig. 6 showing the total  $N_{it}$  profile and the hole-related component of  $N_{it}$  calculated for 10 and  $10^4$  s one may explicitly see that the hole contribution is considerably shifted towards the source. The single-electron component generates

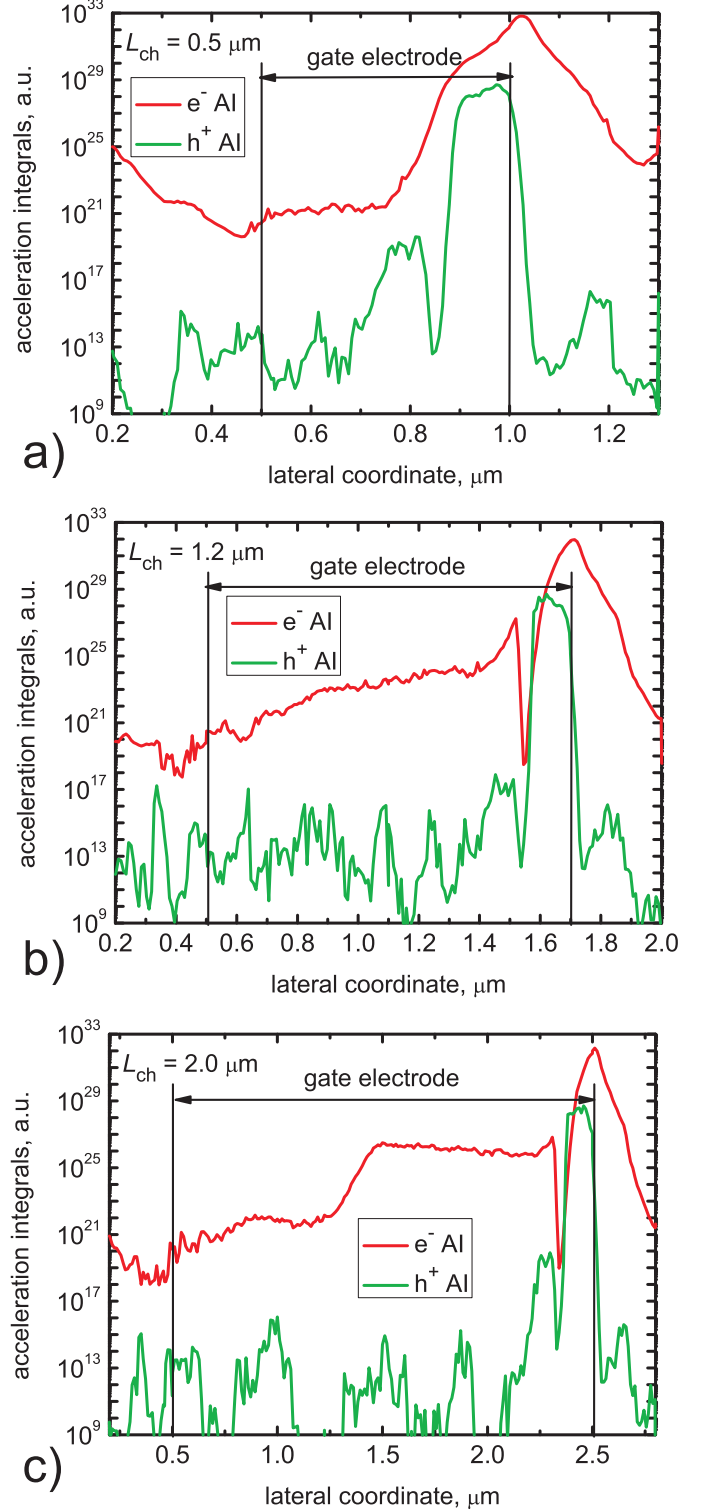


Fig. 5. The acceleration integrals for electrons and holes in the case of  $L_{ch} = 0.5, 1.2$  and  $2.0 \mu\text{m}$ .

traps situated outside the channel which explains why the hole-induced traps have stronger relative impact on  $I_{dlin}$ . While analyzing the relative contribution of holes we intentionally considered only the SC-component because for both types of

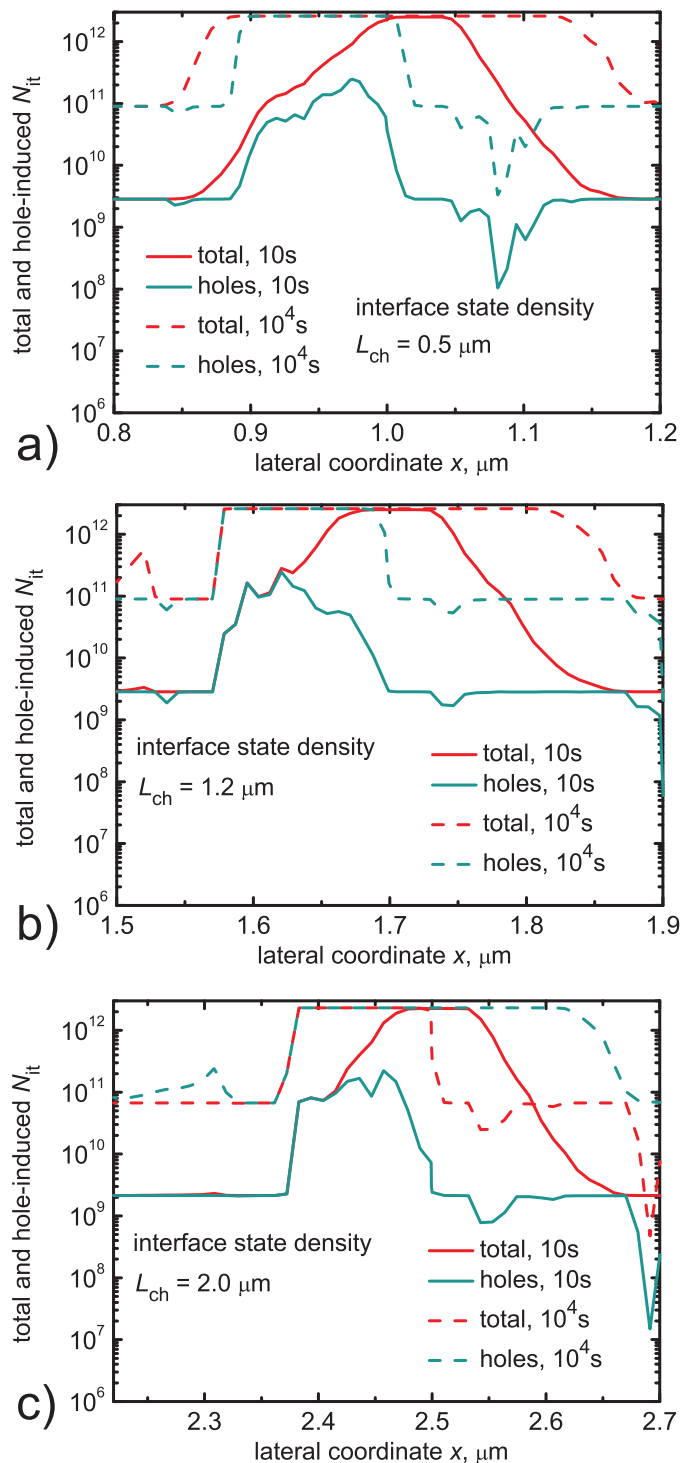


Fig. 6. The total  $N_{it}$  profile and that induced only by holes for 10 and  $10^4$  s and for three different channel lengths.

carriers the AI is already too high, thereby saturating the rate for this process. As a result, it is impossible to distinguish between multiple-electron and multiple-hole contributions. Additionally,  $N_{MC}$  is homogeneously distributed over  $x$  and speculations about position-dependent impact of  $N_{it}$  on the device performance are relevant only for the SC-component.

The contribution of hot holes to the total concentration  $N_{it}$  (Fig. 3) is much less than the corresponding fraction of  $I_{dlin}$  change. This trend becomes more pronounced for longer devices. Furthermore, such a behavior is also supported by Fig. 4 where the experimental  $I_{dlin}$  degradation is plotted against the theoretical one as well as the portion of  $I_{dlin}$  change induced by electrons and holes only. Note that in the case of  $L_{ch} = 0.5 \mu\text{m}$  the degradation may be represented employing only the electron-component, but this is impossible for longer devices.

#### IV. CONCLUSION

We have presented and verified a novel model for hot-carrier degradation. This model was verified by representing HCD in 5V n-MOSFETs with various channel lengths using a single set of fitting parameters. The model considers not only channel electrons but also secondary holes generated by impact ionization. We have shown that in spite of a less pronounced hole contribution to the total interface states density, the device behavior is more sensitive to the hole-induced trap generation as compared to the electron one. This is related to the fact that hole-induced  $N_{it}$  is situated closer to the channel, thereby affecting the drain current in a stronger fashion. Finally the model allowed us to properly describe the  $I_{dlin}$  degradation.

#### ACKNOWLEDGMENT

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#### REFERENCES

- [1] S. Rauch and G. L. Rosa, "CMOS hot carrier: From physics to end of life projections, and qualification," in *Proc. International Reliability Physics Symposium (IRPS), tutorial*, 2010.
- [2] A. Bravaix and V. Huard, "Hot-carrier degradation issues in advanced CMOS nodes," in *Proc. European Symposium on Reliability of Electron Devices Failure Physics and Analysis (ESREF), tutorial*, 2010.
- [3] S. Tyaginov, I. Starkov, O. Triebel, J. Cervenka, C. Jungemann, S. Carniello, J. Park, H. Enichlmair, C. Kernstock, E. Seebacher, R. Minixhofer, H. Ceric, and T. Grasser, "Interface traps density-of-states as a vital component for hot-carrier degradation modeling," *Microelectronics Reliability*, vol. 50, pp. 1267–1272, 2010.
- [4] I. Starkov, S. Tyaginov, H. Enichlmair, J. Cervenka, C. Jungemann, S. Carniello, J. Park, H. Ceric, and T. Grasser, "Hot-carrier degradation caused interface state profile - simulations vs. experiment," *Journal of Vacuum Science and Technology - B*, vol. 29, no. 1, pp. 01AB09–1–01AB09–8, 2011.
- [5] C. Jungemann and B. Meinerzhagen, *Hierarchical Device Simulation*. Springer Verlag Wien/New York, 2003.
- [6] *MiniMOS-NT Device and Circuit Simulator*, Institute for Microelectronics, TU Wien.
- [7] W. McMahon, K. Matsuda, J. Lee, K. Hess, and J. Lyding, "The effects of a multiple carrier model of interface states generation of lifetime extraction for MOSFETs," in *Proc. Int. Conf. Mod. Sim. Micro*, vol. 1, 2002, pp. 576–579.
- [8] A. Bravaix, C. Guerin, V. Huard, D. Roy, J. Roux, and E. Vincent, "Hot-carrier acceleration factors for low power management in DC-SC stressed 40nm nMOS node at high temperature," in *Proc. International Reliability Physics Symposium (IRPS)*, 2009, pp. 531–546.