Properties of Silicon Ballistic Spin Fin-Based Field-Effect Transistors

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The breathtaking increase of the performance of integrated circuits was made possible by the continuing size miniaturization of semiconductor devices' feature size. The 32nm MOSFET process technology [1] presently in manufacturing involves a sophisticated heavily strained silicon channel and a high-k dielectric/metal gate stack. Although alternative channel materials with a mobility higher than that in silicon were already investigated [2,3], silicon will still be the main channel material for MOSFETs at the 22nm technology node and very likely also beyond, thanks to new device architectures based on multi-gate structures with better electrostatic channel control and reduced short channel effects.

However, with scaling apparently approaching its fundamental limits, the semiconductor industry is facing critical challenges. New engineering solutions and innovative techniques are required to improve MOSFET performance for upcoming device generations.

Spin as a degree of freedom is promising for future nanoelectronic devices for both memory [4] and logic [5] applications. Silicon, the main element of microelectronics, possesses several properties attractive for spintronics: it is composed of nuclei with predominantly zero spin and is characterized by small spin-orbit coupling. In experiment coherent spin transport through an undoped silicon wafer of 350 μ m length was already demonstrated [6]. Spin coherent propagation at such long distances makes the fabrication of spin-based switching devices in the near future quite likely.

We investigate the properties of ballistic fin-structured silicon spin field-effect transistors. The original suggestion for the spin transistor by Datta and Das [7] employs the spin-orbit coupling to introduce the current modulation. The electric-field dependent spin-orbit coupling was assumed to be due to the geometry-induced inversion symmetry breaking, or of the Rashba type. However, as it was demonstrated recently [8], the major contribution to the spin-orbit interaction in thin silicon films is due to the interface-induced inversion asymmetry which is of the Dresselhaus type. The coefficient of the spin-orbit interaction is a linear function of the effective electric field which opens the way to modulate the current by applying the gate voltage.

The non-zero spin-orbit interaction leads to an increased spin relaxation. The D'yakonov-Perel' mechanism is the main spin relaxation mechanism in the systems with the degeneracy between the electron dispersion curves for the two spin projections lifted. In quasi-one-dimensional electron structures, however, the complete suppression of the spin relaxation was predicted [9].

In our studies the fins have a square cross-section with the (001) horizontal faces. The parabolic band approximation becomes insufficient in thin and narrow silicon fins, where an accurate description of the conduction band based on the **k·p** model [10] is necessary. This leads to the subband effective mass depending on the fin height and thickness (Fig.1).

To form the spin transistor we sandwich the silicon fin

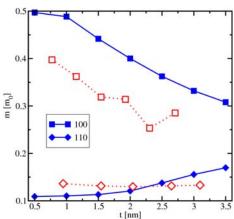


Fig.1: Effective masses vs. thickness for a square fin. Dotted lines are from [11].

between two ferromagnetic metallic contacts. The degree of the spin polarization in each contact is 0 < P < 1. The contacts can be in either parallel or anti-parallel configuration. The carriers in the contacts are characterized by the effective mass and the Fermi-energy. Following [12], delta-function barriers at the interfaces between the contacts and the channel are introduced. Contrary to [12], the spin-orbit interaction is taken in the Dresselhaus form [8]. We study the conductance through the system for the contacts being in parallel and anti-parallel configurations. Differences between the [100] and [110] orientated structures are investigated in detail for a large range of parameters.

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REFERENCES

- P. Packan; et al., High performance 32nm logic technology featuring 2nd generation high-k + metal gate transistors, IEDM 2009, pp.1-4.
- 2. M. Radosavljevic, *et al.*, Advanced high-K gate dielectric for high-performance short-channel In_{0.7}Ga_{0.3}As quantum well field effect transistors on silicon substrate for low power logic applications, IEDM 2009, pp.1-4.
- 3. D. Kuzum, *et al.*, Experimental demonstration of high mobility Ge NMOS, IEDM 2009, pp.1-4.
- S. Parkin, M. Hayashi, L.Thomas, Magnetic domain-wall racetrack memory, *Science* 320, 190 (2008).
- T. Marukame, T. Inokuchi, M. Ishikawa et al., Read/write operation of spin-based MOSFET using highly spinpolarized ferromagnet/MgO tunnel barrier for reconfigurable logic devices, IEDM 2009, pp.1-4.
- B. Huang, D.J. Monsma, I. Appelbaum, Coherent spin transport through a 350-micron-thick silicon wafer, *Phys. Rev. Lett.* 99, 177209 (2007).
- 7. S. Datta, B. Das, Electronic analog of the electro-optic modulator, *Appl.Phys.Lett.* 56, 665 (1990).
- M.O. Nestoklon, *et al.*, Electric field effect on electron spin splitting in SiGe/Si quantum wells, *Phys.Rev.B* 77, 155328 (2008); M. Prada, G. Klimeck, R. Joynt, Spin-orbit splittings in Si/SiGe quantum wells, cond-mat 0908.2417.
- 9. A. Bournel, *et al.*, Gate induced-spin precession in an In_{0.53}Ga_{0.47}As two dimensional electron gas, *The European Physical Journal Applied Physics* **4**, 1 (1998).
- 10. G.L. Bir , G.E. Pikus, Symmetry and Strain-Induced Effects in Semiconductors, J.Willey & Sons, NY, 1974.
- 11. H. Tsuchiya, *et al.*, Comparisons of performance potentials of silicon nanowire and grapheme nanoribbon MOSFETs considering first-principles bandstructure effects, *IEEE Transactions on Electron Devices* **57**, p.406 (2010).
- K.M. Jiang, et al., Tunneling magnetoresistance properties in ballistic spin field-effect transistors, *IEEE Transactions on Electron Devices* 57, p.2005 (2010).