Recent trends in CMOS reliability: from individual traps to circuit simulations

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In order to maintain the trend of ever-increasing performance, several directions have been pursued by the semiconductor industry in the past decade. i) Conventional Si and SiO_2 are being replaced by more exotic materials, from high-k gate dielectrics to metal gates and to high-mobility substrates, ii) new (3D) device architectures are being developed, iii) devices are downscaled toward atomic dimensions, while iv) supply voltages are not correspondingly reduced.

All of these developments constitute new challenges for CMOS reliability. With literally just a handful of defects in the gate oxide of each deeply scaled Field Effect Transistor (FET), statistical treatment, once confined to the breakdown of thin gate oxides, must be applied to other degradation mechanisms. Correctly interpreting these mechanisms relies on measuring and understanding the properties of individual defects and their individual impact on FET operation. At the microscopic level, parallels between effects such as Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI) can be found. When technological solutions start to be inadequate, reliability margin can be increased by considering the particular function of each device in the circuit. This leads to novel, “atomistic” approach to time-dependent variability in circuit simulations.