Superior NBTI Reliability of SiGe Channel pMOSFETs: Replacement Gate, FinFETs, and impact of Body Bias

J. Franco[1,*], B. Kaczer, G. Eneman[1,2], Ph.J. Roussel, T. Grasser[3], J. Mitard, L.-Å. Ragnarsson, M. Cho, L. Witters, T. Chiarella, M. Togo, W.-E Wang[4], A. Hikavyy, R. Loo, N. Horiguchi, and G. Groeseneken[1]

imec, Kapeldreef 75, 3001 Leuven – Belgium
[1] also ESAT Dept., Katholieke Universiteit Leuven - Belgium
[2] also FWO-Vlaanderen – Belgium
[3] Technische Universität Wien - Austria
[4]Assignee at imec
[*]Jacopo.Franco@imec.be

Abstract

In this paper we demonstrate superior NBTI reliability of SiGe pFETs with ultra-thin EOT in a Replacement Metal Gate (RMG) process flow, and in a SiGe channel bulk pFinFET architecture. Moreover, we investigate the Forward Body Bias (FBB) technique showing that it can very efficiently improve the SiGe device I_{ON} without compromising the NBTI reliability, or vice versa further improve the device reliability without compromising the I_{ON}. Based on the insights provided by the Body Bias experiments, we propose a model for the superior SiGe NBTI reliability which can explain all the experimental observations.

Introduction

Negative Bias Temperature Instability (NBTI) is considered the topmost reliability issue for scaled CMOS technologies (1). Due to the high oxide electric field (E_{ox}), the 10 year lifetime of sub-1nm EOT Si pFETs cannot be guaranteed (2) at the expected operating V_{DD} (3). We have recently shown that SiGe pFETs (4) offer superior NBTI reliability (5), and demonstrated a 6Å EOT $Si_{0.45}Ge_{0.55}$ pFET with a 10 year lifetime at operating conditions (V_{DD}=1V) in a Metal Inserted Poly-Silicon (MIPS) process flow (6). We have found that the key to achieve the improved NBTI reliability is the optimization of the Si cap thickness: as shown in Fig. 1, the reduction of this key process parameter consistently boosts the operating overdrive voltage for 10 year reliability.

In this paper we report the *superior SiGe pFET reliability* for the *Replacement Metal Gate* (RMG) process flow (7), as well as for SiGe *pFinFET* devices. We further show the *impact of Body Biasing (BB) on the NBTI reliability* (8,9) of SiGe pFETs. These experiments offer insights into the mechanism of NBTI and allow refinements to the physical model we proposed in (10), providing further its validation. Moreover, we propose *the Forward Body Bias (FBB) technique as a design solution for reducing NBTI* without compromising the device I_{ON} performance, or vice versa to boost the device performance without compromising the NBTI reliability. This technique is shown to be much more efficient for the SiGe channel, as explained by the model discussed here.

Replacement Metal Gate and FinFET

Recently we have shown (6) how a reliability-oriented optimization of the SiGe pFET gate-stack in a MIPS process flow can salvage the device lifetime even at ultra-thin EOT (i.e. aggressively reduced IL, (11)). Here we show that such optimization can be successfully implemented in a RMG process flow as well (Fig. 2). Moreover SiGe channel bulk pFinFETs (12) also show improved NBTI lifetime w.r.t. Si planar ref. when removing the Si cap (Fig. 3). These architecture-independent results suggest *the reduced NBTI as an intrinsic property of the SiGe structure*, further emphasizing the use of a SiGe channel as a promising candidate for future CMOS technology nodes. Additional insights into the physical mechanism behind this superior reliability are now developed through the use of the body biasing.

Impact of Body Bias

$Si_{0.45}Ge_{0.55}$ pFETs with three different Si caps (1.3, 1, and 0.65nm) were used for body bias experiments (Fig. 1, inset). Si channel pFETs with identical high-k/MG stack were used as a reference. Channel width and length were 10µm and 0.5µm respectively, while EOT was ~1nm.

A. Body Bias during NBTI stress only

Fig. 4 shows the V_{th} modulation by V_B for the Si ref. and for the SiGe devices. NBTI stress experiments were performed at 125°C for different BB, while keeping the overdrive stress voltage constant ($V_{ov}=|V_G-V_{th}(V_B)|=1.5V$). The measured NBTI V_{th} shifts are shown in Fig. 5a: SiGe devices with thin Si cap show dramatically lower V_{th} instability w.r.t Si ref. One can observe enhanced NBTI for the Reverse Body Bias (RBB) and reduced NBTI for the FBB (Fig. 5b) on both the Si ref. and the SiGe device, although the NBTI dependence on BB is much stronger for the SiGe device, showing up to 50% ΔV_{th} reduction at FBB. Such a reduction projects into ~100x longer device lifetime (inset of Fig. 5b), while no performance loss occurs since the same gate voltage overdrive is applied, i.e. the hole population in the inversion layer is kept constant. Conversely, NBTI stresses performed at different BB but the same V_G (i.e. higher $V_{ov} \rightarrow$ higher hole population → higher I_{ON} for the FBB case), show identical V_{th} instability (Fig. 6).

To explain these experimental results, E_{ox} experienced by the device during the NBTI stress for different BB was calculated with MEDICI (13). For a constant V_{ov}, the FBB reduces E_{ox}, while E_{ox} is independent of BB when stressing the devices at the same V_G (Fig. 7). The E_{ox}-modulation as a function of the BB V_{th}-modulation is found to be identical for the Si and the SiGe devices (Fig. 8). The measured NBTI shifts at fixed V_{ov} (Fig. 5a), rescaled as a function of the calculated E_{ox} (Fig. 9a) *show the same E_{ox} dependence* as the standard NBTI data (V_B=0V, Fig. 9b) for both Si and SiGe, confirming the NBTI dependence on the BB is solely related to its E_{ox} modulation. Fig. 9 also shows the stronger E_{ox} NBTI dependence of the SiGe devices, readily explaining why the BB technique is much more efficient for SiGe devices (Fig. 5b). This higher efficiency converts into a reduced power cost of the FBB technique for a given NBTI reduction w.r.t. Si (Fig. 10).

B. Body Bias during NBTI stress and relaxation

In the previous section BB was applied during the stress period while V_B=0V was applied during the sensing (relaxation) phase. In this section, a more circuit-realistic case with constant BB during *both* NBTI stress and relaxation is discussed. Fig. 11 shows an *even stronger NBTI reduction with the FBB, especially for the SiGe device with thinnest Si cap where the instability can be almost completely suppressed*. To understand this, we compare the NBTI relaxation traces measured with V_B=0V and with FBB: an accelerated relaxation is found in the latter case, with the SiGe device showing stronger acceleration (Fig. 12). A faster NBTI relaxation has been reported when applying a positive V_G (14) and ascribed to reduced E_{ox} enhancing hole de-trapping (15). As one can notice in Fig. 7b, the FBB reduces E_{ox} also at low biases, e.g. at the typical sensing bias $V_G \approx V_{th}$ (V_{ov}=0V); such an E_{ox} reduction is calculated in MEDICI to be equivalent to the application of a positive V_G=+0.65V on the SiGe devices during the NBTI relaxation. Fig. 13 shows that the application of this positive V_G accelerates the relaxation as much as observed for the FBB case (~4.5 dec., cf. Fig. 12b).

A Model for SiGe Superior NBTI Reliability

In the light of the bulk bias experimental results, we again invoke our recently proposed model (10) assuming the existence of a defect band in the dielectric centered below the Si valence band (16) to explain the superior reliability of the SiGe pFETs. As depicted in Fig.14a, the Fermi level in the channel determines which part of the defect band is accessible to channel holes. Modeling such a defect band as a simple Gaussian distribution over the dielectric energy bandgap (see eq. (1-3) in Fig. 14a), we can calculate the ratio of existing oxide defects which can be accessed as a function of E_{ox} from the SiGe channel (for different Si cap thicknesses) and for the Si ref., as shown in Fig. 14b. The simple model readily explains all effects observed in SiGe pFETs with a thin Si cap: i) *the reduced NBTI (Figs. 5a, and 9b);* ii) *the stronger field acceleration which enhances the NBTI reduction efficiency of the FBB technique (Figs. 5b, 9a, and 10);* iii) *the stronger acceleration of the NBTI relaxation at low E_{ox} (Figs. 11 and 12b).*

Conclusions

We have shown SiGe pFETs offer superior NBTI reliability at ultra-thin EOT in a Replacement Metal Gate (RMG) process flow. The same promising reliability improvement was shown also in a SiGe channel bulk pFinFET architecture. Moreover, we have shown that the Forward Body Bias (FBB) technique can very efficiently improve the reliability without compromising the I_{ON} or vice versa, improve the SiGe device I_{ON} without compromising the reliability. The Body Bias experiments also provided further support for our model explaining the superior SiGe pFET NBTI reliability.

Acknowledgments

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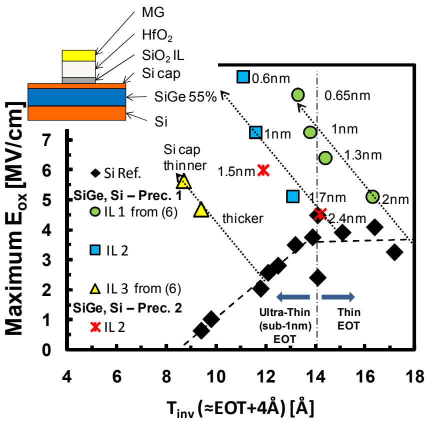


Fig. 1: A boost of the operating E_{ox} (i.e., ≈ operating overdrive voltage / T_{inv}) for 10 year reliability when reducing the Si cap thickness (reported values "as-grown") is observed consistently for several SiO_2 interfacial layer (IL) thicknesses and for different Si precursors and epi-growths ('Prec. 1' and 'Prec. 2'). The inset shows a gate-stack sketch of a SiGe pFET.

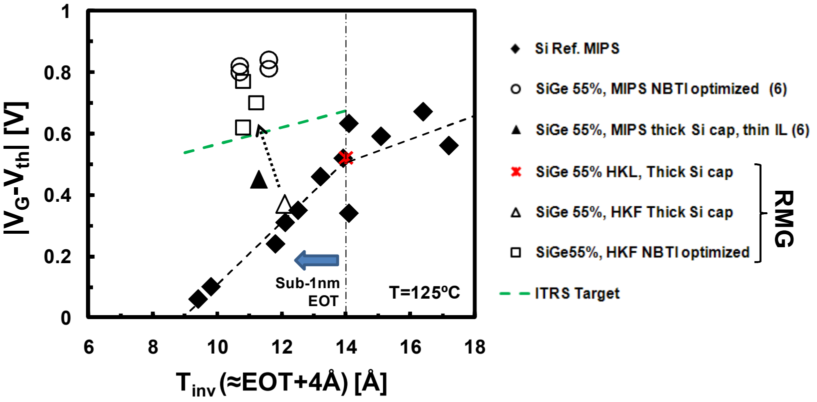


Fig. 2: A high Ge fraction (55%) in a 6.5nm thick SiGe quantum well, combined with a thin Si cap (0.8nm) boost NBTI lifetime to meet the target V_{DD} at ultra-thin EOT in a MIPS process flow (6). Such optimization is successfully implemented also in the RMG process flow.

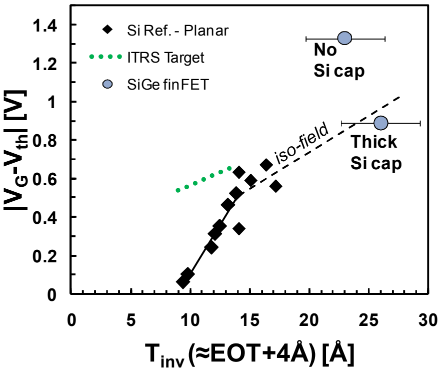


Fig. 3: SiGe channel bulk pFinFETs without the Si cap show improved NBTI reliability w.r.t. to the same devices with a thick Si cap and w.r.t Si planar pFETs. The dashed trendline for T_{inv}>14Å demarcates planar Si pFET constant field scaling (*"iso-field"*). Uncertainty in T_{inv} is related to the finFET dimensions.

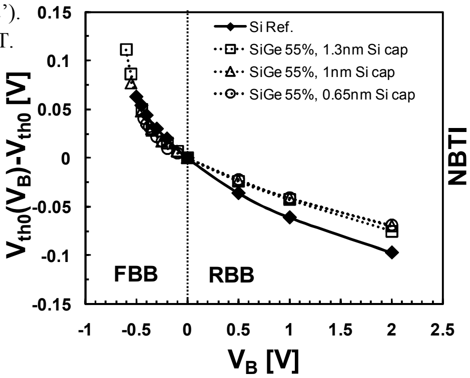


Fig. 4: A very similar V_{th} modulation by V_B is observed for the Si ref. and for the SiGe devices.

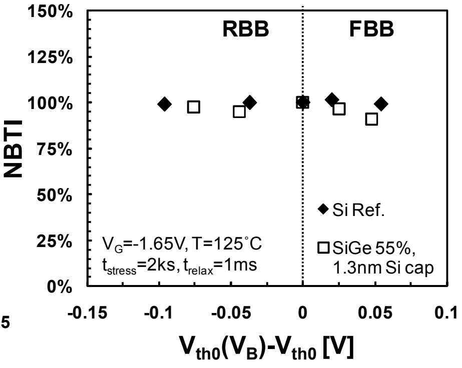


Fig. 6: NBTI stresses for different BB at constant V_G=-1.65V, show the same V_{th} instability (ΔV_{th} is normalized w.r.t. the standard case V_B=0V). FBB technique can be therefore used to enhance the device performance without compromising the NBTI reliability (i.e. higher V_{ov} → higher hole population → higher I_{ON} for the FBB case).

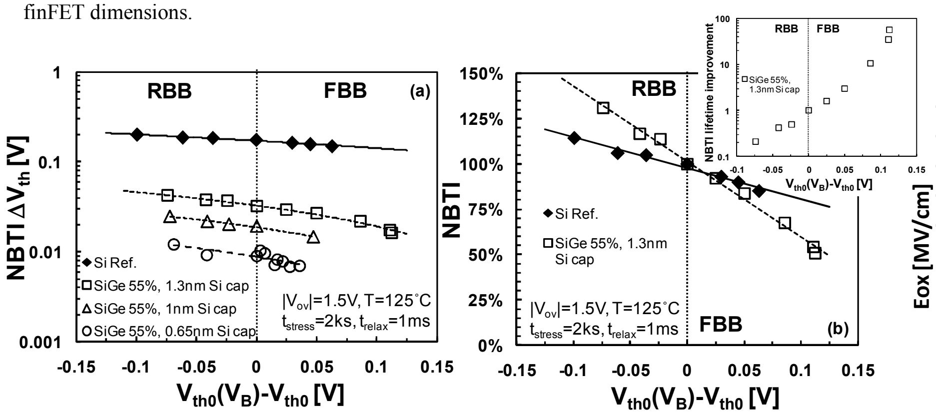


Fig. 5: NBTI stress experiments performed at 125°C for different BB, with fixed stress V_{ov}=|V_G-$V_{th}(V_B)$|=1.5V (i.e., same I_{ON}). **(a)** SiGe devices with thin Si cap show dramatically lower V_{th} instability w.r.t. Si ref. **(b)** When normalizing the NBTI shifts measured with BB w.r.t. the V_B=0V case, enhanced NBTI for the RBB and reduced NBTI for the FBB are found. The NBTI dependence on BB is much stronger for SiGe devices, showing up to 50% ΔV_{th} reduction in the FBB condition, which converts into ~100x longer device lifetime (inset).

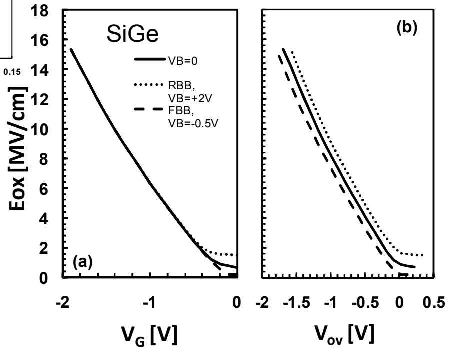


Fig. 7: E_{ox} as calculated with MEDICI for different BB. **(a)** E_{ox} is independent of V_B when stressing the devices at the same V_G, while **(b)** for a constant V_{ov}, the FBB reduces E_{ox} due to reduced depletion charge (see the band diagram in Fig. 8 inset).

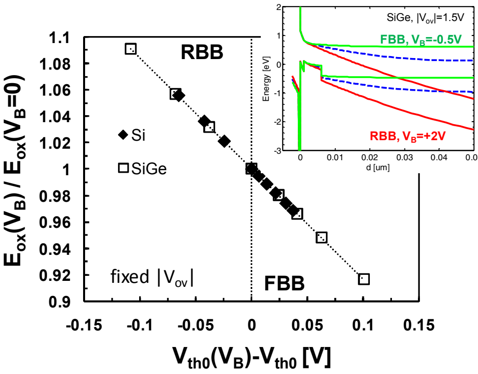


Fig. 8: Calculated E_{ox} modulation at fixed V_{ov} as a function of the BB V_{th} modulation is identical for both the Si ref. and the SiGe devices (Si cap thickness 1nm). The inset shows the simulated band diagrams of the SiGe devices.

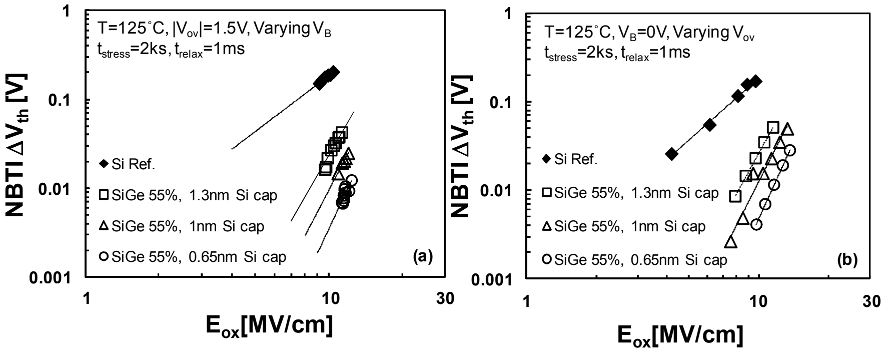


Fig. 9: **(a)** The measured NBTI shifts for different BB at fixed V_{ov} are rescaled as a function of the actual E_{ox} (as calculated with MEDICI, see Fig. 8). The same NBTI field dependence is found as for **(b)** standard NBTI stressing (V_B=0V). The field dependence is found to be stronger for the SiGe devices, explaining the stronger NBTI reduction at a given FBB.

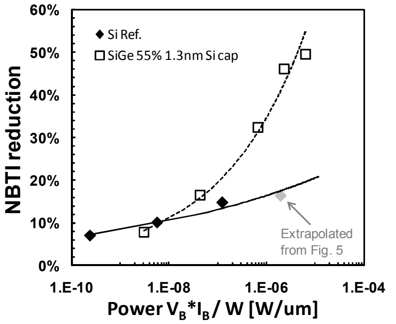


Fig. 10: The stronger field dependence for SiGe, converts into a reduced power cost of the FBB technique for SiGe for a given NBTI reduction w.r.t. the Si ref.

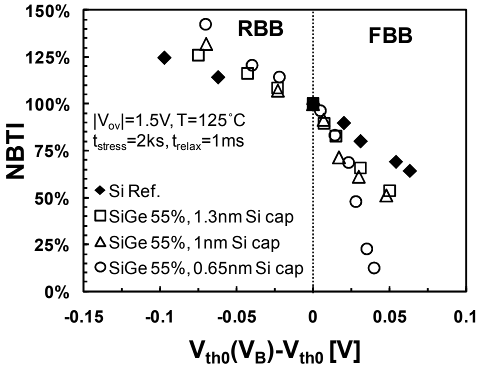


Fig. 11: NBTI experiments with BB during *both* stress and relaxation. A much stronger NBTI reduction with the FBB is found, especially for the SiGe device with the thinnest Si cap.

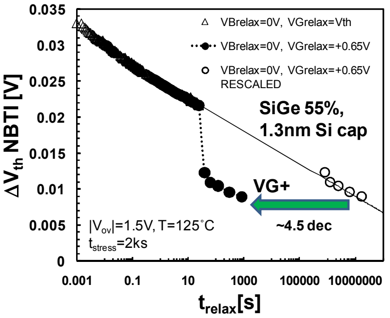


Fig. 13: The FBB-related E_{ox} reduction at the relaxation bias V_G=V_{th} is calculated with MEDICI to be equivalent to the application of a positive V_G=+0.65V for the SiGe devices (at V_B=0V). This positive V_G accelerates the NBTI relaxation as much as observed for the FBB case (~4.5 dec., cf. Fig. 12b) confirming the field reduction accelerates hole de-trapping.

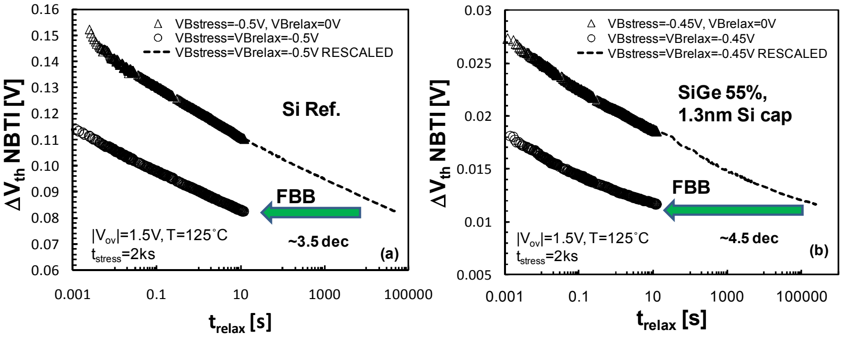
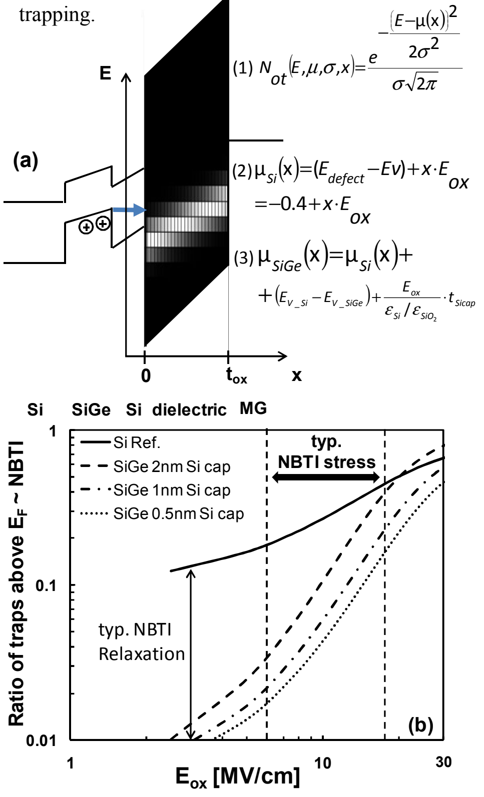


Fig. 12: **(a)** NBTI relaxation traces measured with V_B=0V and with FBB on a Si ref. pFET: the FBB accelerates the relaxation (~3.5 decades). **(b)** SiGe pFETs show more accelerated relaxation (~4.5 decades). This faster relaxation is ascribed to reduced E_{ox} at V_{th} for the FBB cases (see Fig. 7b).



$$(1)\ N_{ot}(E,\mu,\sigma,x)=\frac{e^{-\frac{(E-\mu(x))^2}{2\sigma^2}}}{\sigma\sqrt{2\pi}}$$

$$(2)\ \mu_{Si}(x)=(E_{defect}-Ev)+x\cdot E_{ox} =-0.4+x\cdot E_{ox}$$

$$(3)\ \mu_{SiGe}(x)=\mu_{Si}(x)+ +(E_{V\_Si}-E_{V\_SiGe})+\frac{E_{ox}}{\varepsilon_{Si}/\varepsilon_{SiO_2}}\cdot t_{Sicap}$$

Fig. 14 (right): **(a)** A model including a defect band in the dielectric centered at -0.4eV below the Si valence band as observed in (16). The Fermi level in the channel determines which part of the defect band is accessible to channel holes. The defect band is modeled as a Gaussian distribution over energy (eq. 1), with its mean modulated by the E_{ox} (eq. 2) and by the valence band offset between the SiGe and the Si, and the Si cap thickness (eq. 3). **(b)** The ratio of accessible oxide defects can be calculated as a function of the E_{ox} for the SiGe channel (with different Si cap) and for the Si ref. This simple model explains the reduced NBTI for SiGe pFETs with a thin Si cap, and the stronger field acceleration which enhances the NBTI reduction efficiency of the FBB technique. *The calculation favorably compares with the experimental data* in Fig. 9. Finally, at the low E_{ox} (V_G≈V_{th}) typically used to measure the NBTI relaxation, a higher ratio of defects is pushed below the SiGe Fermi level, explaining the enhanced hole de-trapping (cf. Fig. 12).