

Normally-Off InAlN/GaN HEMTs with n⁺⁺ GaN Cap Layer: A Simulation Study

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The ongoing interest in the development of GaN-based enhancement-mode high electron mobility transistors (EHMTs) resulted in several different approaches being proposed, one of them employing a reduction of the gate-to-channel distance. In order to facilitate gate recessing, a technique using a n⁺⁺ cap layer was suggested by Kuzmik *et al.* [1], who also analyzed the contribution of the cap layer to current conduction and on the mechanism of the off-state breakdown. In this work we complement the experimental results with two-dimensional device simulation using Minimos-NT [2]. We have employed it previously for the optimization studies of a whole generation of AlGaIn/GaN HEMTs [3], but also for high-temperature simulations [4].

The simulated devices are adopted from [1]. The positive charges (introduced by polarization effects) at the channel/barrier interface is compensated by a commensurate negative surface charge at the barrier/cap interface. The polarization charge density is $2.8 \times 10^{13} \text{ cm}^{-3}$. Fig. 1 shows the electron concentration in a vertical cut as determined by the C-V measurements, which are in good agreement with the simulation results, especially for the two-dimensional electron gas (2DEG) concentration.

Fig. 2 shows measured and simulated data for the transfer characteristics, which exhibit an excellent agreement too. We further focus on carrier transport in the GaN cap and the 2DEG. Fig. 3 shows the current density in the region close to the gate. The simulated device is biased to on-state at $V_{GS}=1.5 \text{ V}$ and $V_{DS}=8.0 \text{ V}$. The highly conductive 2DEG is clearly distinguished. In the InAlN barrier the electron concentration is very low (Fig. 1), therefore there is no current observed except for a narrow “channel” under the edge of the n⁺⁺ GaN cap. In the latter, however the current is two to three orders of magnitude lower than in the 2DEG. This is confirmed in Fig. 4, which shows the current density in a vertical cut in the gate-drain region (same position as the cut in Fig. 1). Thus, the simulations confirm the experimental results [1], that the n⁺⁺ cap layer does not significantly contribute to the current transport. It should be also mentioned, that while the drain side of the cap indeed does exhibit some minimal current, in the source side there is no current at all. The electric field distribution is further investigated under the off-state bias condition ($V_{GS}=0.0 \text{ V}$, $V_{DS}=8.0 \text{ V}$). The electric field has its peak at the drain side of the gate region (see Fig. 5) so there are carriers with high enough energy to overcome the potential barrier of the InAlN layer. On the source side of the gate the electric field is overall lower, which results in a minimal current density in the n⁺⁺ cap layer. Fig. 6 shows again a cut of the current density in the gate-drain region, however in the off-state bias. The difference with magnitude of seven orders in the current density of the 2DEG channel region and the cap layer is seen. It should be noted that the drain leakage current is provided mostly by the buffer layer under the off-state conditions, which explains the experimental results [1].

In summary, we study current transport effects in the recessed n⁺⁺ GaN cap layer in InAlN/GaN normally-off HEMTs. Our simulations confirm that the cap layer does not have a significant contribution to the on-state drain current. We also observe that it does not provide additional mechanism for gate-to-drain leakage under the off-state bias.

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References

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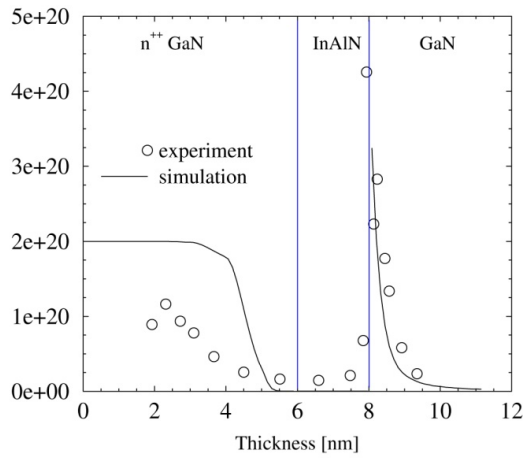


Fig. 1: Electron concentration in a vertical cut ($V_{GS}=1.5$ V, $V_{DS}=8.0$ V).

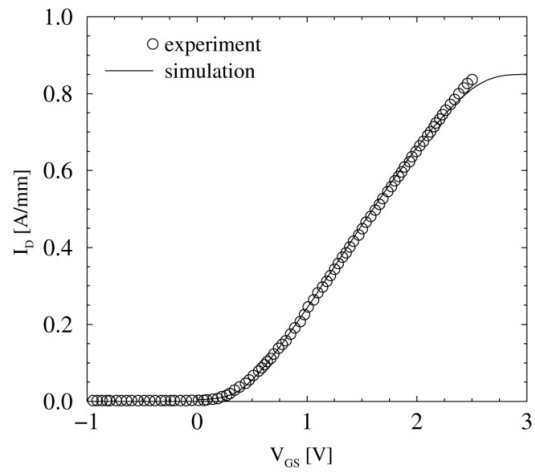


Fig. 2: Simulated and measured transfer device characteristics.

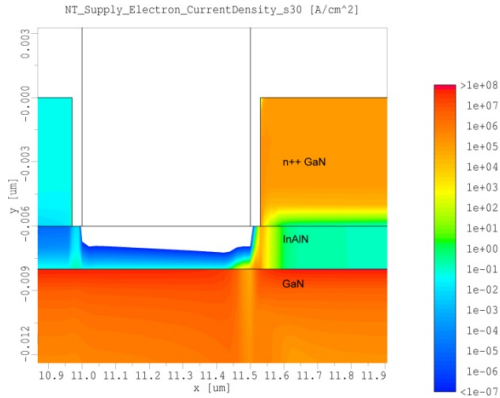


Fig. 3: Electron current density in the gate region in the on-state ($V_{GS}=1.5$ V, $V_{DS}=8.0$ V).

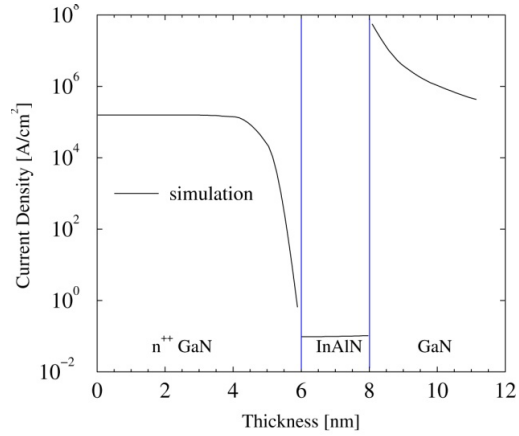


Fig. 4: Electron current density in a vertical cut in the on-state ($V_{GS}=1.5$ V, $V_{DS}=8.0$ V).

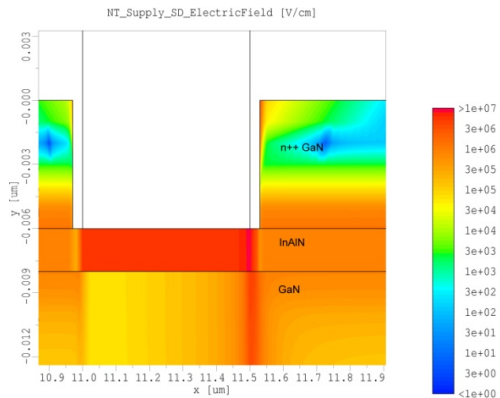


Fig. 5: Electric field distribution in the gate region in the off-state ($V_{GS}=0.0$ V, $V_{DS}=8.0$ V).

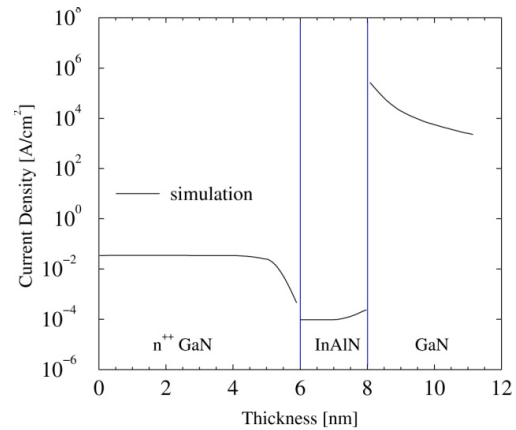


Fig. 6: Electron current density in a vertical cut in the off-state ($V_{GS}=0.0$ V, $V_{DS}=8.0$ V).