Hierarchical Simulation of Process Variations and Their Impact on Circuits and Systems: Results

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***Abstract*—Process variations increasingly challenge the manufacturability of advanced devices and the yield of integrated circuits. Technology computer-aided design (TCAD) has the potential to make key contributions to minimize this problem, by assessing the impact of certain variations on the device, circuit, and system. In this way, TCAD can provide the information necessary to decide on investments in the processing level or the adoption of a more variation tolerant process flow, device architecture, or design on circuit or chip level. Five Fraunhofer institutes joined forces to address these issues. Their own software tools, e.g., for lithography/topography simulation, mixed-mode device simulation, compact model extraction, and behavioral modeling, have been combined with commercial tools to establish a hierarchical system of simulators in order to analyze process variations from their source, e.g., in a lithography step, through device fabrication up to the circuit and system levels.**

***Index Terms*—Circuit simulation, manufacturability, process modeling, semiconductor device modeling, sensitivity, yield.**

I. Introduction

AS DISCUSSED in the preceding paper [1] also published in this Special Issue, process variations are increasingly affecting the performance, the reliability, and the manufacturability of advanced semiconductor devices. Simulation is the only realistic possibility for a holistic investigation of the impact of the large manifold of relevant process variations on circuits and systems. A hierarchical approach is required to investigate process variations from their sources, which are largely at the equipment level, to their impact on devices, circuits, and systems. Simulation tools are needed, which accurately predict not only nominal values but also their variability, both along the chain of technological processes and at all levels.

Based on the assessment of process variability and the state of the art summarized in [1], in the following relevant application results obtained in the "HIErarchische Simulation von PArameterschwankungen in NAnoelektronischen Systemen" (HIESPANA) project at Fraunhofer are presented.

II. HIESPANA Project

In the HIESPANA project [2], five Fraunhofer institutes, i.e., the Institute for Integrated Systems and Device Technology (IISB), the Division Design Automation of the Institute for Integrated Circuits (IIS/EAS), the Institute for Microelectronic Circuits and Systems (IMS), the Institute for Industrial Mathematics (ITWM), and the Institute for Algorithms and Scientific Computing (SCAI), have joined forces to develop a software system that allows simulating the impact of process variations. Further contributions have been made by the Vienna University of Technology and the University of Cologne. Own software tools have been combined with third-party tools from software houses and academic sites to establish a hierarchical system of simulators to analyze process variations from their source, e.g., in a lithography process, through device fabrication up to circuit and system levels. Aside from software integration issues, the activities have particularly focused on extension of the lithography (*Dr.LiTHO* [3], [4]), deposition, and etching simulation tools from IISB; commercial circuit simulators by IIS/EAS to allow for the appropriate simulation of variations; and the behavioral modeling tool *Analog Insydes* [5] of ITWM to treat variations with statistical reduction methods. SCAI has focused on the improvement and the use of advanced tools for efficiently solving systems of sparse equations (*SAMGp* [6]), mixed-level device/circuit simulation *MECS* [7], and *PRO-CHAIN* [8]. The project software has been evaluated with a demonstrator chip fabricated by IMS. Some examples for the application of these programs for the hierarchical simulation of the impact of variations are given in the following section.

Manuscript received November 16, 2010; revised February 23, 2011; accepted March 31, 2011. Date of publication June 16, 2011; date of current version July 22, 2011. This work was supported by the Fraunhofer Internal Programs under Grant MAVO 817 759. The review of this paper was arranged by Editor A. Asenov.

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Digital Object Identifier 10.1109/TED.2011.2150226

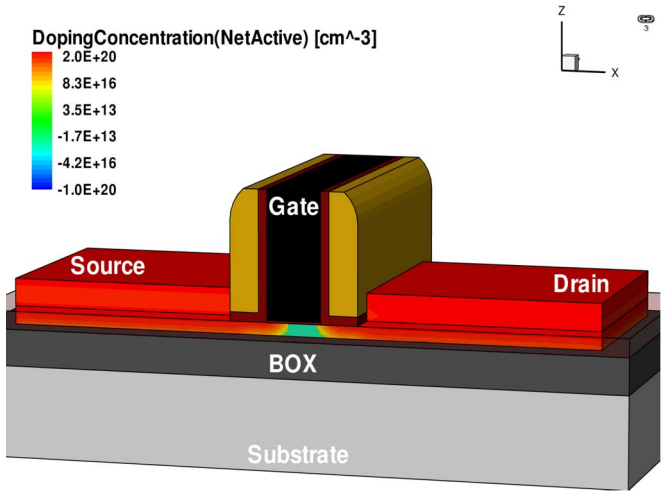

Fig. 1. Geometry and doping concentration of a 32-nm nominal FD SOI transistor, simulated with *Sentaurus Process*.

III. Results

Planar fully depleted silicon-on-insulator (FD SOI) transistors are among the most promising device architectures for scaling beyond the 22-nm node. For the single-gate (SG) FD SOI transistor shown in Fig. 1, the geometry has been generated with the solid modeling feature of *Sentaurus Process* [9]. Doping and electrical properties of the nominal device have been simulated with *Sentaurus Process* and *Sentaurus Device* [9], respectively.

The first example deals with the impact of focus and dose variations in optical lithography on the threshold voltage of 32-nm transistors with different architectures. 32-nm bulk, SG and double-gate (DG) FD SOI devices were investigated. A basic difference in the impact of these variations on bulk and the SOI transistors is shown in this example. Using *Dr.LiTHO*, the lithography process window analysis [allowing up to 10% critical dimension (CD) variation] for the 193-nm water immersion process employed yielded a depth of focus of 52 nm and a "threshold latitude" of 8.5% (see the drawn rectangle in [1, Fig. 1]). In order to study the impact of process variations not only under best conditions, the variation range has been increased to ± 40 nm around best focus and to a threshold range of 0.25–0.4 (broken-line rectangle in [1, Fig. 1]). A fixed etch bias of 13 nm was assumed. The inherent nature of the lithography process, as discussed in [1, Sec. II], yields the highly asymmetric probability distribution function (pdf) of the CD, as shown in Fig. 2. Process and device simulations using *Sentaurus*—assuming the gate length distribution from lithography as previously explained—then predict only for the bulk metal–oxide–semiconductor (MOS) field-effect transistor a symmetric threshold-voltage distribution because of the dominating role of the pockets.

For both SOI devices, quite similar highly asymmetric generalized-extreme-value (GEV) distributions result. The pdf's for the bulk and the FD SOI n-channel MOS (NMOS) transistors are shown in Fig. 3. More details on the setup of this simulation, the interpretation, and the additional results are presented in [10].

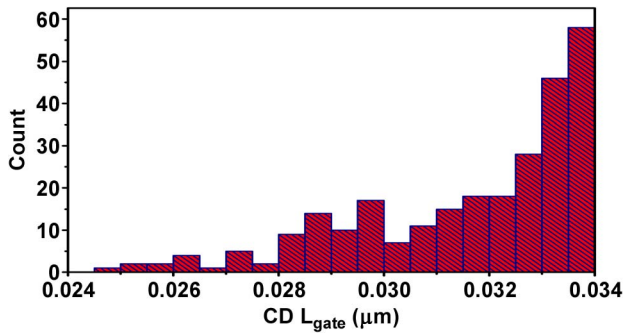

Fig. 2. Pdf of the transistor gate length subject to variations of focus and dose in optical lithography.

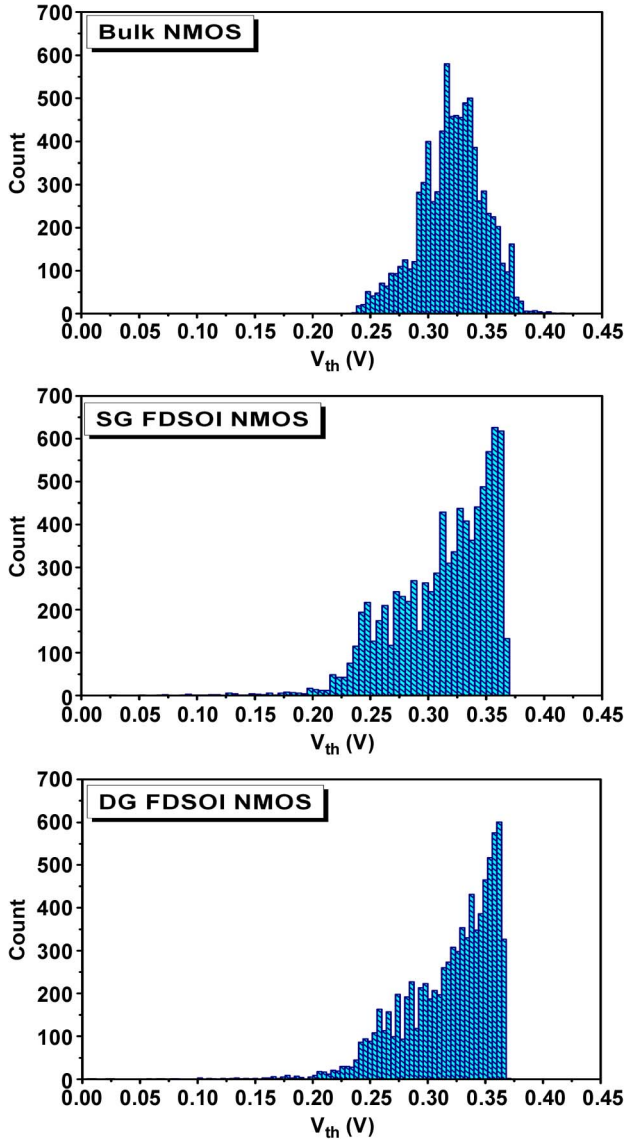

Fig. 3. Pdf of the threshold voltage for different transistor architectures. Bulk NMOS transistor—(top) normal distribution and (middle) SG and (bottom) DG FD SOI NMOSs—both GEV distributed.

In other simulation studies, the impact of across-wafer inhomogeneities in etching [11], silicon thickness variations of SOI wafers [12], and variations in the peak temperature of millisecond anneals [13] has been investigated. Furthermore, a method

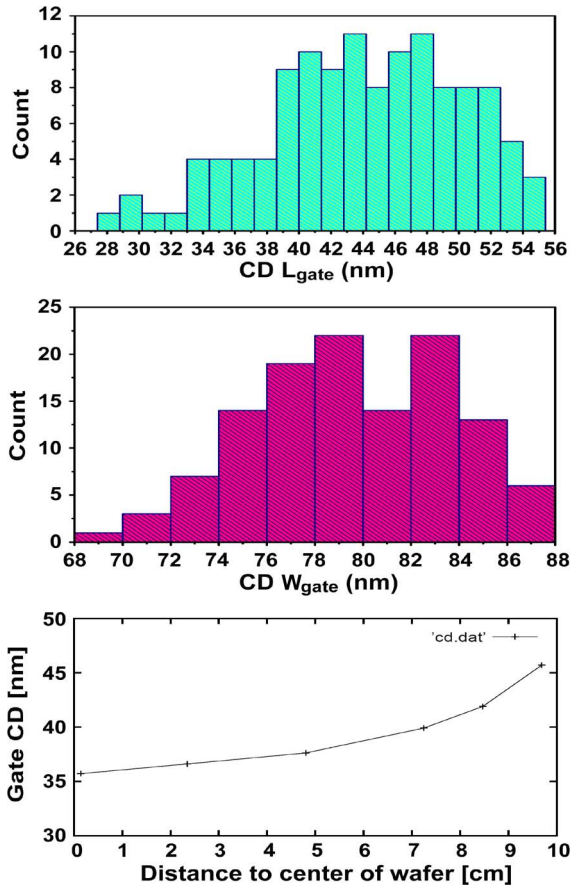

Fig. 4. Variations of gate (top) length and (middle) width due to defocus and dose variations in optical lithography. (Bottom) Variations of gate CD due to variations of etch bias across the wafer, assuming nominal CD after lithography.

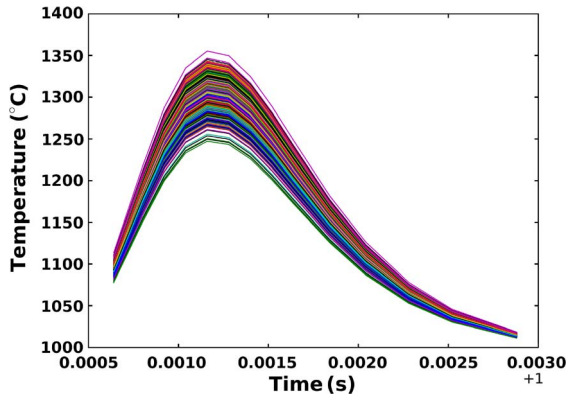

Fig. 5. Variation of temperature profile during millisecond annealing.

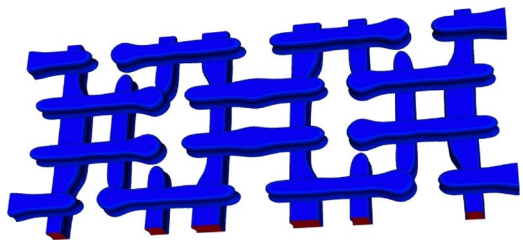

Fig. 6. Resist profiles of (vertical) the active n+/p+ layers and (horizontal) the poly layer of four 6T SRAM cells investigated, for fixed values of dose and defocus. The simulated area is 1.764 μm $\times$ 0.754 μm. The pattern sizes are 45, 55, 65, and 105 nm. Due to periodic boundary conditions in the etching simulations, four cells had to be simulated.

to derive variation-aware compact models was shown [12]. In the following, a comprehensive study is presented, which includes all these effects and methods, including the treatment of correlations as outlined in [1, Sec. IV]. The fabrication of SOI transistors has been simulated, using *Dr.LiTHO* linked to *Sentaurus Process* and *Sentaurus Device*. The impact of focus and dose variations in lithography was included, affecting both the gate width and length (see Fig. 4). The apparent double peak, particularly in the pdf of the gate width, results from the overlay of the highly asymmetric pdf's due to focus variations [10] and a linear pdf due to dose variations. Absolute CD variations are comparable for the gate length and width. However, because a nominal width twice as large as the gate length was used, relative variations are smaller for the width than for the length. The variation of the etch bias was simulated using equipment simulation with the *CFD-ACE* [14] tool coupled with the 3-D etching simulator *ANETCH* [11] from IISB (see Fig. 4). For the variation of temperature profiles during millisecond anneal, an approximation already used before [13] was applied (see Fig. 5) and fed into the simulation of annealing with *Sentaurus Process*.

Similar to the first example, 193-nm water immersion lithography has been used. The focus was varied between -80 and 10 nm, and the dose was varied between 21.7 and 24.7 mJ/cm^2. Two relevant layers (active n+/p+ and polygate) of a standard six-transistor static random-access memory (6T SRAM) cell were simulated with rigorous mask simulation (solving Maxwell's equations), full vectorial image simulation, and a full resists model, after applying simple optical proximity correction to the attenuated phase-shift mask used. The simulated resist layers are shown in Fig. 6. An etch bias with variations as previously outlined was used. Doping processes were simulated with *Sentaurus Process*, assuming two implantations for source/drain (S/D) extensions and contact formation after the formation of the elevated S/D, respectively. Doses and energies used were low enough to avoid damage concentrations above 10^{21} cm^{-3}. Combined spike (nominal peak of 1070 °C) and Flash annealing (1280 °C) was used, as discussed in [12].

Simulation splits were performed as follows: 11 equally distributed values each for both defocus variables and both dose values; 11 equally distributed positions along the wafer radius for the determination of the etch bias; and 11 values for the peak temperature in the Flash annealing, equally distributed between 1230 °C and 1330 °C. Standard BSIM3SOI [15] parameters were extracted from three dimensional (3-D) process and device simulations using *Sentaurus*, including the length and width variations previously mentioned. As demonstrated before [12], temperature variations only affect contact resistances and were therefore only considered as resistance variations in the SRAM cell, together with the width and length variations.

In total, 11^6 variations were simulated with the compact model as previously described. The six transistors in the cell were subject to identical variations, however partly starting from different nominal values due to the layout in lithography. A python interface was used to transfer the process variations that resulted from lithography, etching, and annealing to the

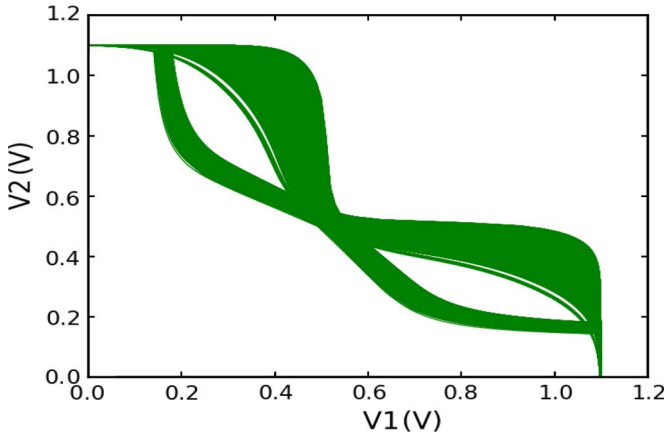

Fig. 7. Classical butterfly characteristic in the READ operation mode of the 6T SRAM cell under the influence of the six statistically independent process variations.

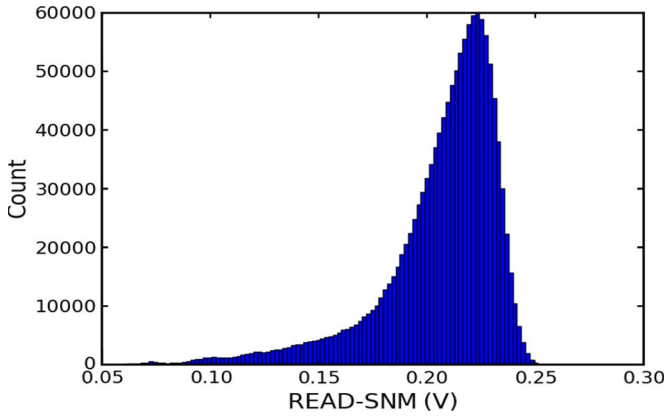

Fig. 8. Variation of the READ SNM of the 6T SRAM cell due to the six statistically independent process variations.

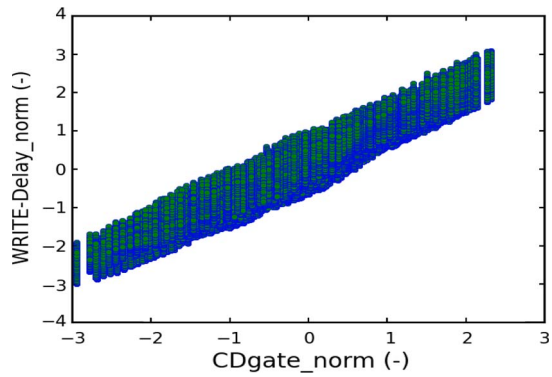

Fig. 9. Correlation between the normalized WRITE delay of the 6T SRAM cell and the normalized transistor gate CD. The values are given as deviation of the varying quantity (e.g., CD) from its mean value normalized to the standard deviation of the varying quantity.

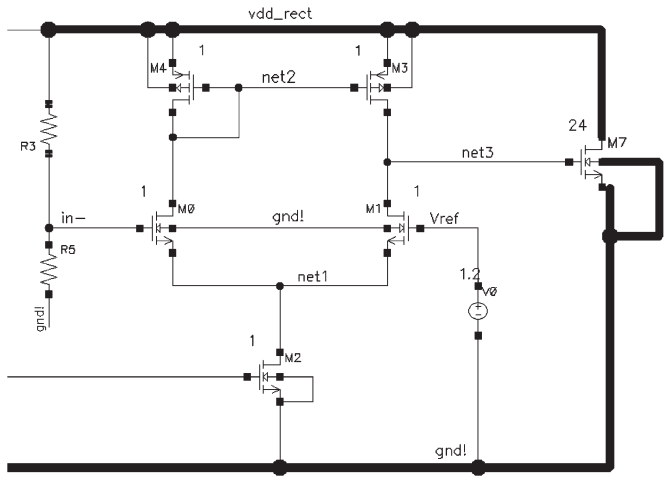

Fig. 10. Voltage-limiter circuit subject to local and global process variations.

SPICE level. Using this interface, the values of the gate length and width were first included in the SPICE netlist and second used to recalculate the contact resistances of the SRAM cell in combination with the annealing peak temperature, using a compact model extracted before from the 3-D process and device simulations. This procedure was repeated after each simulation step until each combination of process variations was simulated. The computational effort amounted to about 20 days on three conventional 2.5-GHz central processing unit cores.

In the following, some key results are presented. Fig. 7 shows the static behavior of the SRAM cell in the READ state, indicating a large spread of the static noise margin (SNM). Fig. 8 shows the pdf of the SNM of the SRAM cell. In both figures, a large variability is visible. As an example for the treatment of the correlations, Fig. 9 shows the strong correlation between the normalized WRITE delay and the normalized variation of the gate length. The spread of the WRITE delay at the fixed gate length indicates the impact of the other variations. Although the nominal values for the gate length differ in the SRAM cell from transistor to transistor, due to proximity effects in lithography, the normalized length variations were identical.

A further detailed discussion of the various correlations and conditional distributions is just a straight-forward postprocessing of the data obtained.

In the next example, the simulation of the impact of local and global process variations on the circuit level is presented for a voltage-limiter circuit, as shown in Fig. 10. This analog building block is used in larger mixed-signal applications, where full-chip verification requires replacement by an equivalent behavioral model. The block model needs to represent the statistical characteristics of the circuit including correlations. The divided voltage at node "in−" is compared with reference V_{ref}, which, in effect, opens transistor M7 accordingly until the target value for the voltage at node vdd_rect is reached.

Fig. 11 shows assumed local and global variations of the threshold voltage V_{th}, which can be readily obtained from coupled equipment, process, and device simulations. Here, it is important to note that not only the sources of variations previously discussed can be considered but also others that may be important for the device or the circuit in question, e.g., dopant fluctuations in the case of transistors with doped channels.

Starting from a SPICE model of the voltage-limiter circuit, the threshold voltages of the respective transistors are changed according to these pdf's. For the local variations, the transistors are independently treated of each other, whereas global variations affect all transistors in the same way. In this example, we examine the variations of the settling time at node vdd_rect when a voltage ramp is applied.

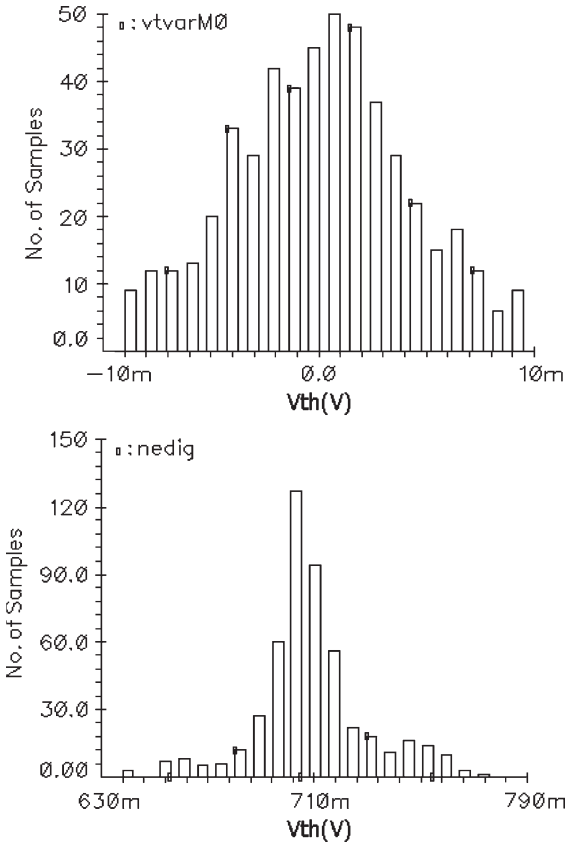

Fig. 11. Assumed threshold-voltage variations as combination of (bottom) global variations for all NMOS devices and (top) local variations for device M0 in the differential pair of the voltage-limiter circuit.

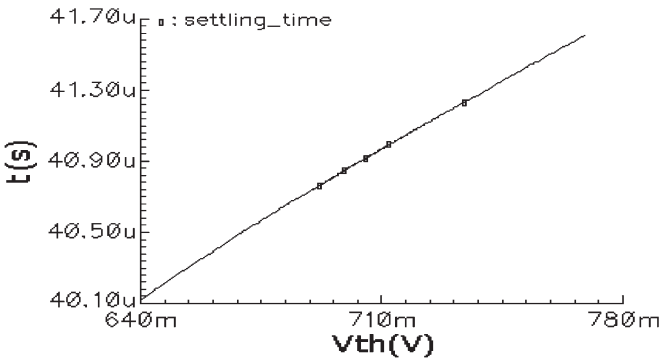

Fig. 12. Observed relation between the threshold voltage and the settling time for the voltage-limiter circuit.

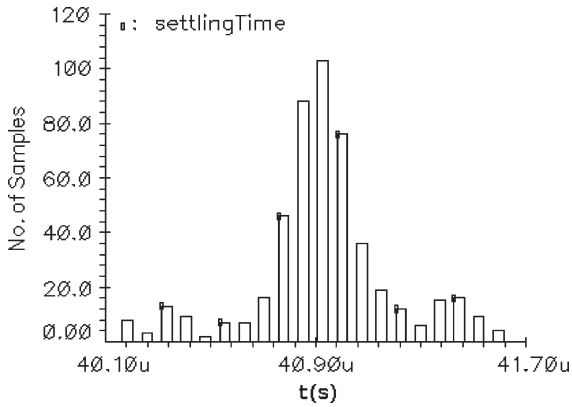

Fig. 13. Simulated frequency distribution of the characteristic settling time when local and global variations of the threshold voltage are present.

We obtained the influence of the $V_{\rm th}$ variations on the settling time separately for local and global variations. This yields two new random variables for the locally and globally induced settling-time variations, respectively.

Now, it is possible to parameterize multiple instances of that block correctly in a hierarchical manner. Again, variations of the locally induced settling time are independently treated, whereas global variations affect all blocks simultaneously. This enables the variation analysis of complex circuits where only a simulation with behavioral models is feasible.

This separated propagation of local and global variations is only possible in the case of linear block behavior. Fig. 12 depicts the nearly linear relation between the threshold voltage and the settling time. Therefore, both distinct distributions yield the same result as the combined distribution that is shown in Fig. 13. Further refinements of the simulations are straightforward, using the approach described in [1, Sec. IV].

For larger circuits or systems, behavioral models, as discussed in [1, Sec. III-G], can be used. In the next step, behavioral models have been extracted using the program *Analog Insydes* from Fraunhofer ITWM [16], [17]. Due to the symbolic modeling of analog circuits in this tool, it is possible to calculate the sensitivities of output parameters y_i (here: the output voltage) on input parameters p_j in an analytical way. Starting with a static behavioral model $f(x,p)=0$, where

$$f : R^n \times R^m \to R^n \tag{1}$$

sensitivities S are calculated by

$$S = \left.\frac{dy}{dp}\right|_{(x_0,y_0)} \in R^{q\times m} \tag{2}$$

which is the solution of the equation system

$$\left.\frac{df}{dp}(x,p)\right|_{(x_0,p_0)} = 0 \tag{3}$$

where $x \in R^n$ denotes the state vector, $p \in R^m$ is the vector of distributed parameters, $x_0 \in R^n$ is the operating point, and $p_0 \in R^m$ is the nominal design point. The system output vector $y \in R^q$ is a subvector of state x. Then

$$y|_p \approx y|_{p_0} + S \cdot (p - p_0) \tag{4}$$

is a first-order approximation of the system output.

The sensitivities in (x_0, p_0) yield information about the output change depending on parameter variations. Using this approach, the importance of the accuracy of parameters in the production of a circuit can be estimated.

Table I shows the normalized sensitivity $S \cdot y/p$ of the output voltage of the voltage-limiter circuit to various parameters such as resistances R3 and R5, and the transistor gate width W, length L, oxide thickness $T_{\rm ox}$, and threshold voltage $V_{\rm th}$, with the frames referring to those in Fig. 14. Obviously, variations of the parameters of the dashed block, i.e., the matching resistors,

TABLE I
SENSITIVITY OF THE OUTPUT VOLTAGE OF THE VOLTAGE-LIMITER CIRCUIT WITH RESPECT TO VARIOUS DEVICE PARAMETERS

normalized sensitivity	parameters
~ 0.65	R3, R5
~ 0.56 – 0.72	Tox, Toxm
~ 0.51 – 0.53	Vth0
~ 0.039 – 0.045	NLX
~ 0.035 – 0.037	U0
~ 0.02 – 0.03	W, L
~ 0.005	Tox, Toxm, Vth0, NLX, U0, W, L
~ 0.003	Tox, Toxm, Vth0, NLX, U0, W, L

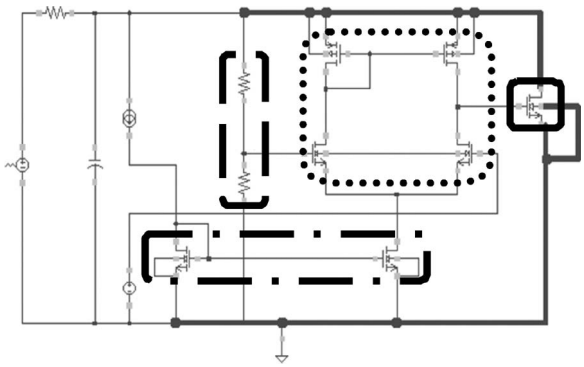

Fig. 14. Voltage-limiter circuit. Some blocks are marked, which have different sensitivity with respect to variations.

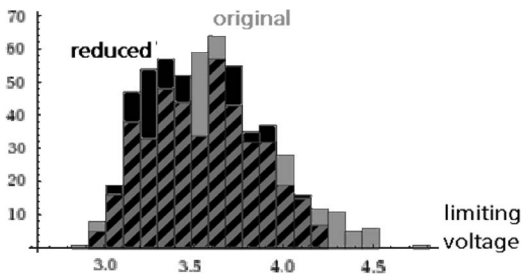

Fig. 15. Pdf of the output voltage of the current-limiter circuit for the original and reduced behavioral models.

and of some parameters of the dotted block have the largest impact on the output voltage.

Furthermore, symbolic statistical order reduction, including treatment of the variations, has been implemented in *Analog Insydes*. This allows for the minimization of the number of equations in the behavioral model (1), largely maintaining accuracy while reducing simulation time. An example is given in Fig. 15, where the pdf of the output voltage is compared between the original and reduced models, yielding good agreement. Table II characterizes the reduced model in terms of the order reduction and the simulation time.

TABLE II
COMPARISON OF MODEL ORDERS AND SIMULATION TIME FOR THE ORIGINAL AND REDUCED BEHAVIORAL MODELS

	model order	simulation time [s]
original	353	18.96
reduced	157 (44.5%)	3.14 (16.5%)

As a promising approach for enhancing the splitting process to obtain the R^k vectors (see [1, Sec. IV]), as well as for controlling computational and data complexity, the *PRO-CHAIN* strategy [8], [18] has been recently transferred to the process-to-device/circuit simulation chains. *PRO-CHAIN* has been originally developed for the forming-to-crash and casting-to-crash chains arising in the automotive industry. Corresponding mathematical software modules have been integrated into the *DesParO* software [19] for parameter sensitivity analysis, interpolation, and robust multiobjective optimization. The main steps of the current *PRO-CHAIN* version for the process-to-device/circuit simulation chain are:

1) at the process level
   a) input: parameters, along with ranges, distribution functions (determined or assumed), and correlations;
   b) iterative analysis by means of *DesParO*: process simulations performed based on a first experimental design [design of experiment (DoE)] followed by a sensitivity analysis of results (functionals on discretization grids; DF-ISE format [9]) and an interpolation and a compression of these functionals and statistical measures for the overall parameter range; principal component analysis combined with interpolation based on radial basis functions and polynomial detrending is used here; *DesParO* sets up an extended DoE and requests another analysis if the current DoE does not allow for a sufficient interpolation; etc.;
   c) output: database (compressed) describing simulation results, along with interpolated statistics on, e.g., the final grid of the nominal simulation (without variations);
2) at the device level or the coupled circuit and device level [*Multiphysical Electric Circuit Simulator (MECS)*]
   a) input: database from the process level, mapped to the grid for device simulation if necessary;
   b) iterative analysis by means of *DesParO* for results (functionals on grids and/or device characteristics);
   c) output: database (compressed) including statistics; and
3) at the circuit level
   a) input: mapped database from the device level or parameters, along with variations and correlations;
   b) iterative analysis by means of *DesParO*.

In particular *PRO-CHAIN* together with the mixed-level simulator *MECS* allows for a deep analysis of the impact of

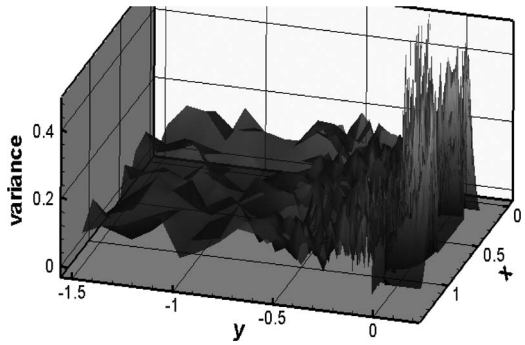

Fig. 16. Variance of the potential for the p-channel MOS (PMOS) based on a DoE with 17 experiments for variations of the gate length and the channel implantation. On the x- and y-axes, spatial coordinates are shown in micrometers. The nitride spacers and the oxide areas are located on the right-hand side.

parameter variations on the process level to the circuit level if, at least for some devices, compact modeling shall be avoided and replaced by a tightly coupled circuit and device simulation.

The exemplary output of the statistical analysis of the process-to-device simulation chain for the HIESPANA demonstrator is shown in Fig. 16. The gate length and the channel implantation have been simultaneously varied for a PMOS and an NMOS in an inverter by means of a DoE with 17 experiments in total. *Sentaurus Process* and *MinimosNT* have been used. The results of the device simulations have been mapped (interpolated) to the resulting grid of the nominal device simulation. Variances are substantial, particularly in and/or around nitride and oxide.

IV. Conclusion

Hierarchical coupled equipment, process, device, circuit, and system simulation is a valuable approach to assess the impact of variations and to decide about the best equipment, process, and device architectures options and the best tradeoffs to be taken. Technologies with normal distributions of process parameters can lead to highly asymmetric parameter distributions at the device level. A cooptimization of the nominal performance of devices, circuits, and systems and of their variability is of paramount importance because these targets may compete against each other.

Acknowledgment

The authors want to acknowledge the contributions from their colleagues at Fraunhofer A. Burenkov, T. Fühner, D. Kunder (IISB), T. Klick, C. Sohrmann (IIS/EAS), T. Feldengut, S. Kolnsberg, A. Strack, J. Wang (IMS), T. Halfmann, M. Hauser, P. Lang, O. Schmidt (ITWM), C. Hettkamp, B. Klaassen, N. Männig. P. Thum, L. Torgovitski (SCAI), and of J. Cervenka (TU Vienna), C. Tischendorf, M. Selva Soto (Univ. Köln).

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