New Trends in Microelectronics: Towards an Ultimate Memory Concept

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***Abstract*—In this paper we briefly discuss different memory technologies based on new storage information principles, highlight the most promising candidates for future universal memory, make an overview of the current state-of-the-art of these technologies, and outline future trends and possible challenges.**

Keywords-ZRAM, non-volatile memory, STT-MRAM, RRAM

I. INTRODUCTION

For many decades charge based storage memory technologies (DRAM, flash memory, and other) have been successfully scaled down to achieve higher speed and increased density of memory chips at lower bit cost. However, memories based on this storage principle are gradually approaching the physical limits of scalability. Although a new cell structure for DRAM has been developed by industry to overcome the scaling challenges at 30nm, future size reduction below 20nm is facing physical limitations and the required process complexity results in high manufacturing costs [1].

This is the reason that new types of memories based on a different storage principle are gaining momentum.

Apart from good scalability, a new type of memory must also exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, and a simple structure [2].

From new technologies two of the most promising candidates for future universal memory are spin transfer torque RAM (STT-MRAM) and resistive RAM (RRAM). Currently, STT-MRAM and RRAM have been demonstrated on 64 Mb [3] and 4Mb [4] test chips, respectively. These technologies could be manufacturable within 5–10 years [5].

First we briefly review the nearest future of DRAM technology, including ZRAM as a potential replacement of DRAM. Then we outline the possibility of creating a universal non-volatile memory based on resistance change and spin, the current state of these technologies, trends and challenges, and demonstrate modeling approaches.

II. ZERO-CAPACITANCE RAM

DRAM with vertical gate type transistors was introduced in order to resolve the critical scaling problems, but it is not easy to reduce the size of the cell capacitance for the 20nm technology node [1].

A DRAM memory cell based on a transistor alone technology could solve this problem. The concept of a 1T/0C DRAM was introduced already a decade ago [6]. The functionality of the first generation ZRAM is based on the possibility to store majority carriers in the floating body. The carriers are generated by impact ionization caused by the minority carriers close to the drain. The threshold voltage is modified because of the charge accumulated in the body, thus guaranteeing the two states of a MOSFET channel, open and close, for a gate voltage chosen between the two thresholds.

The idea of the second generation ZRAM is to exploit the properties of the bipolar transistor [7], allowing to expand the ZRAM applicability to such advanced non-planar devices as FinFETs, multi-gate FETs, and gate-all-around FETs. Contrary to the first generation, the current is flowing through the body of the structure. Thereby the value of current is increased by roughly the ratio of the fin radius to the surface layer thickness. The majority carriers are generated due to impact ionization. They are stored under the gate at the silicon/silicon dioxide interface. The stored charge provides good control over the bipolar current, in contrast to the first generation ZRAM, where the charge is stored in the area close to the buried oxide.

In [8] it is demonstrated that the programming window, which is formed by the two current values and the two gate voltage values when switching appears, is sufficiently large for stable ZRAM operation on double-gate transistors with an only 11nm thin silicon body (Fig.1).

The use of vertical gate-all-around transistors extends the ZRAM roadmap to future generations. One disadvantage of the ZRAM cell is the relatively high operating voltage needed to ignite impact ionization. To reduce the operating voltage, a new concept of a 1T/0C cell was recently proposed [9].

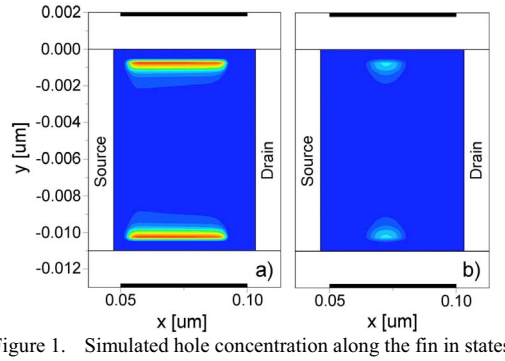

Figure 1. Simulated hole concentration along the fin in states "1" (a) and "0" (b) for a 11nm thin ZRAM device [8].

III. MAGNETIC MEMORY TECHNOLOGY

The basic element of an MRAM is a magnetic tunnel junction (MTJ), a sandwich of two magnetic layers separated by a thin non-magnetic spacer. While the magnetization of the pinned layer is fixed due to the fabrication process, the magnetization direction of the free layer can be switched between the two states parallel and anti-parallel to the fixed magnetization direction. Switching in MRAM is performed by applying a magnetic field. In contrast to field-driven MRAM, STT-RAM does not require an external magnetic field. Switching between the two states occurs due to the spin-polarized current flowing through the MTJ. The spin-polarized current is only a fraction of the total charge current. Therefore, high current densities are required to switch the magnetization direction of the free layer.

The reduction of the current density required for switching and/or the increase of the switching speed are the most important challenges in this area [10].

Measurements [11] showed a decrease in the critical current density for a penta-layer MTJ with the two pinned magnetic layers in the anti-parallel configuration (Fig. 2, left) compared to the three-layer MTJ. Theoretical predictions showed a decrease of the switching time in penta-layer structures with an increase of the out-of-plane component of the magnetostatic field [12]. An even more pronounced decrease of the switching time and current density were recently reported in a penta-layer structure with a composite free layer (Fig.2, right) [13]. Fig.3 demonstrates a substantial decrease of the switching time in the penta-layer structure with the composite free layer. The magnetostatic field h_{ms} causes the magnetization to tilt out of the x–y plane. The non-zero angle between the fixed magnetization and the magnetization in the free layer results in an enhanced spin transfer torque, when the current starts flowing. In the case

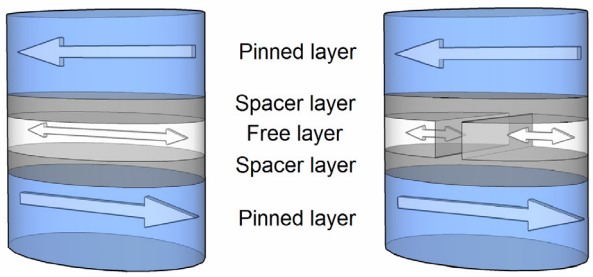

Figure 2. Schematic illustration of penta-layer MTJs with monolithic (left) and composite free layer (right).

of the monolithic structure, however, the torque remains marginal in the central region, where the magnetization is along the x-axis. As the amplitude of the end domains precession increases, the central region experiences almost no spin torque and preserves its initial orientation along the x-axis, thus preventing the whole layer from alternating its magnetization orientation. This is, however, not the case, when the central region is removed in the composite structure and the end domains become virtually independent.

A reduction of the switching current is also observed in MTJs with perpendicular magnetization [14].

STT-RAM based on CoFeB-MgO MTJs with interfacial anisotropy is already close to overcome the scalability limit of charge based storage memories. However, such devices still require reducing damping and increasing thermal stability [15]. For device with its dimension smaller than 30nm, it is necessary to use materials with higher anisotropy such as Co/Pt multilayers or a FePt system. However, radically new approaches are required to write data on such layers without sacrificing speed [16].

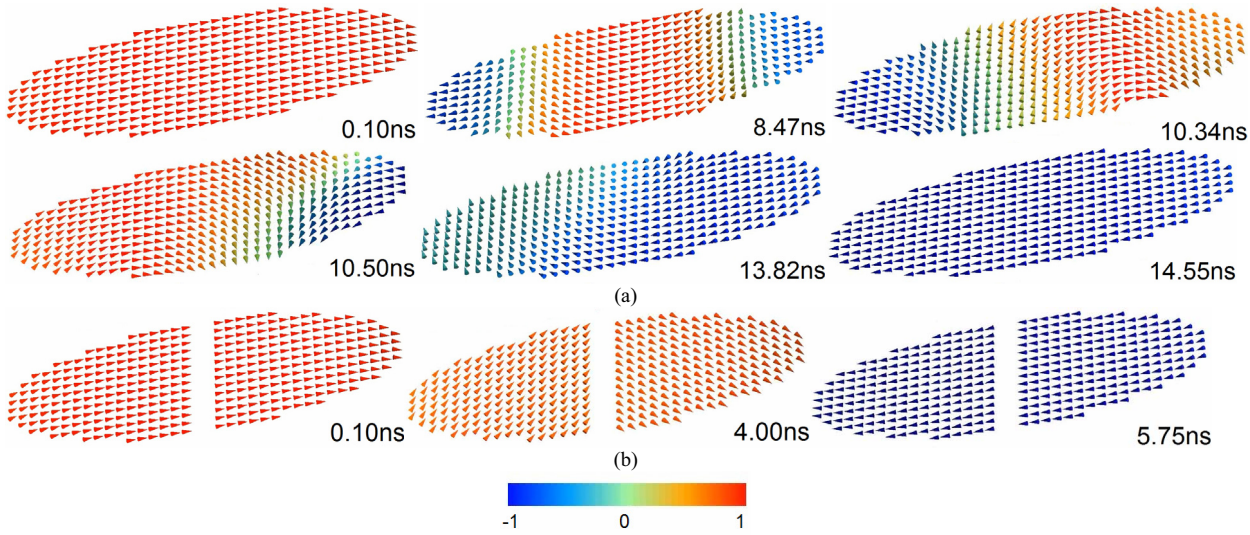

Figure 3. Snapshots of the switching process for a MTJ with (a) monolithic and (b) composite free layer. The direction of the magnetization is shown as the unit vectors, color indicates the x-component of the magnetization, the x-axis is directed along the long axis of the ellipse.

IV. RESISTANCE CHANGE MEMORY TECHNOLOGY

Resistance change memory possesses the simplest structure in the form of a metal–insulator–metal (MIM) sandwich. The electrical conductance of the insulator can be set at different levels by the application of an electric field, and this phenomenon can be used in memory devices. The resistive switching phenomenon is observed in different types of insulators, such as metal oxides, perovskite oxides, chalcogenide materials, and others. Three memory technologies, CBRAM, PCRAM, and RRAM, are based on the resistive switching.

The concepts of RRAM shown by NDL [17] and Samsung [18] have already surpassed the scaling limit of charge based storage memories [19]. Despite this, a proper fundamental understanding of the RRAM switching mechanism is still missing, hindering further development of this type of memory. First and foremost, one needs a better understanding and control of the physics of the SET/RESET processes through development of accurate models [5].

In the literature several physical mechanisms/models based on either electron or ion based switching have been suggested for the explanation of resistive switching in perovskite oxides [20–24], in metal oxides with bipolar [23,25–28] and unipolar behavior [29], and metal oxides heterostructures [30].

In [26, 27] the resistive switching behavior is associated with the formation and rupture of a conductive filament (CF). The CF is formed by localized oxygen vacancies V_o and the conduction is due to electron hopping between these V_o. Rupture of a CF is caused by a redox reaction in the oxide layer under a voltage bias (Fig. 4).

In [27] for modeling the resistive switching by Monte Carlo techniques the dynamics of oxygen ions (O^{2-}) and electrons in an oxide layer was described as follows:

- formation of V_o by O^{2-} moving to an interstitial position;
- annihilation of V_o by moving O^{2-} to V_o;
- an electron hop into V_o from an electrode;
- an electron hop from V_o to an electrode;
- an electron hop between two V_o.

Results of simulations obtained with the model [27] are shown in Fig.5 and Fig.6. Fig.5 shows the RESET process for a single CF, which is in good agreement with the measurements from [26].

Fig.6 shows the RRAM switching hysteresis cycle. The simulated cycle is in agreement with the experimental cycle from [31] shown in the inset of Fig. 6. The interpretation of the RRAM hysteresis cycle obtained from the stochastic model is as follows. If a positive voltage is applied, the formation of a CF begins, when the voltage reaches a critical value sufficient to create V_o by moving O^{2-} to an interstitial position. The formation of the CF leads to a sharp increase in the current (Fig.6, Segment 1) signifying a transition to a state with low resistance. When a reverse negative voltage is then applied, the current increases linearly, until the applied voltage reaches the value at which an annihilation of V_o is triggered by means of moving O^{2-} to V_o. The CF is ruptured and the current decreases (Fig.6, Segment 3). This is the transition to a state with high resistance.

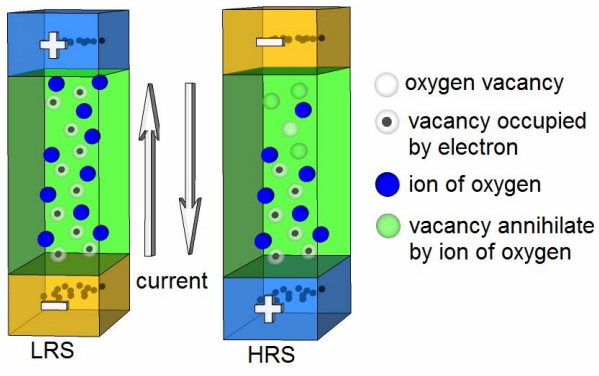

Figure 4. Schematic illustration of the conducting filament in the low resistance state (LRS) and hight resistance state (HRS).

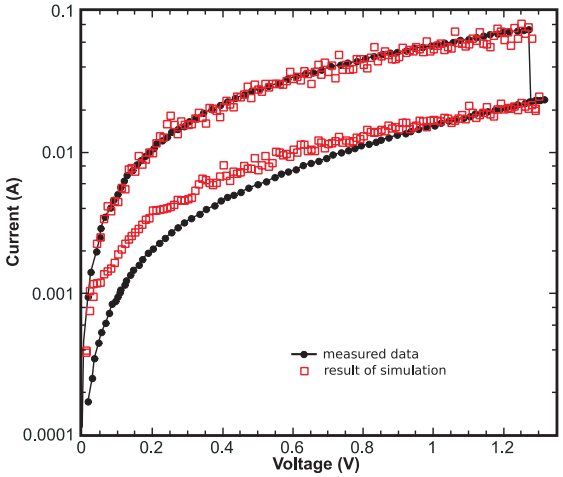

Figure 5. Current-voltage curves during the reset process. The lines are measured result from [26]. The symbols are obtained from the model [27].

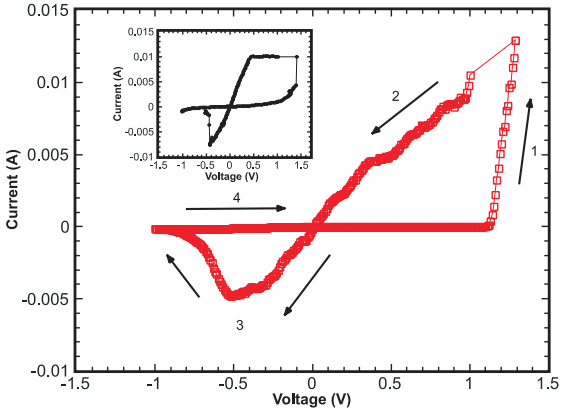

Figure 6. I-V characteristics showing the hysteresis cycle obtained from the model [27]. The inset shows the hysteresis cycle for M-ZnO-M from [31].

V. CONCLUSIONS

A DRAM memory cell based on a transistor alone helps to resolve the critical scaling problems. The use of vertical gate-all-around transistors extends the 1T/0C DRAM roadmap to future generations. However, this technology is still volatile and can not be used for universal memory. Therefore and because of the fact that charge based memory scaling will be at risk as technology scales down to 20nm, conceptually new types of memories based on a different storage principle are gaining momentum. One of the most promising candidates for future universal memory is the STT-RAM. STT-RAM based on CoFeB-MgO MTJs with interfacial anisotropy is close to overcome the scalability limit of charge based storage memories. However, such devices still require reducing damping and increasing thermal stability. Another candidate for future universal memory with good potential is RRAM. In particular, RRAM cells have already surpassed the scaling limits of charge based storage memories. However, a better understanding and control of the physics of the SET/RESET processes through development of accurate models is urgently needed. Material and structure optimization through accurate modeling and simulations is a key ingredient in successful designing of future memory cells with low power consumption.

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