Recent Results Concerning the Influence of Hydrogen on the Bias Temperature Instability

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***Abstract*—Alongside the intensive debate concerning the influence of hydrogen on NBTI we present several details which have received little or no attention in the past. We show experimental evidence that hydrogen does not only passivate interface traps but also positive oxide charges or border traps. Besides passivation, hydrogen increases the overall drift capability of a device under NBTS, thereby increasing the sum of both precursors and activated defects. Furthermore hydrogen passivation has a positive effect on PBTI, presumably through the passivation of pre-existing oxide traps.**

I. INTRODUCTION

Recent scientific progress identified switching oxide traps as the main contributors to the negative bias temperature instability (NBTI) [1, 2]. The temperature and time dependent recovery of these oxide traps following a switch of the gate bias from stress level back to the V_{TH} allows for very detailed and elaborate analysis of those defects [3]. As we understand more and more about the behavior of the oxide traps we loose the connection to the creation of interface traps (namely P_b centers) through the dissociation of silicon–hydrogen (Si–H) bonds.

The precise role of hydrogen (H) in the NBTI experiences an intensive debate. Some groups attribute the diffusion of H away from the interface during stress as the limiting process which leads to the well-known power law-like degradation behavior of NBTI [4, 5]. Other groups argue that H may get trapped in charged oxide traps and leads to fixed positive oxide charges and interface traps [6, 7].

In this study the influence of H on N- and PBTI is studied by comparing virgin characteristics and stress experiments on devices with different H concentrations at the silicon–silicon dioxide ($\mathrm{Si{-}SiO_2}$) interface.

II. EXPERIMENTAL DETAILS

We use $100\,\mu\mathrm{m} \times 6\,\mu\mathrm{m}$ width times length p- and nMOSFETs with either $30\,\mathrm{nm}$ or $3.7\,\mathrm{nm}$ $\mathrm{SiO_2}$ gate oxides. Throughout our study we observed consistent results independent of the actual gate oxide thickness. We performed a split experiment on a number of wafers where we varied the thickness of the titanium–titanium nitride (Ti–TiN) barrier in the metallization stack. Titanium is known to gather H, thereby decreasing H diffusion from upper metal stacks toward the gate oxide [8]. We have verified with time of flight secondary ion mass spectroscopy (TOF-SIMS) and charge-pumping (CP) measurements that the Ti–TiN barrier thickness changes the passivation degree of the $\mathrm{Si{-}SiO_2}$ interface of the device [9]. In particular a thinner Ti–TiN barrier leads to an accumulation of H near the $\mathrm{Si{-}SiO_2}$ interface in TOF-SIMS and reduces the density of interface traps measured by charge pumping.

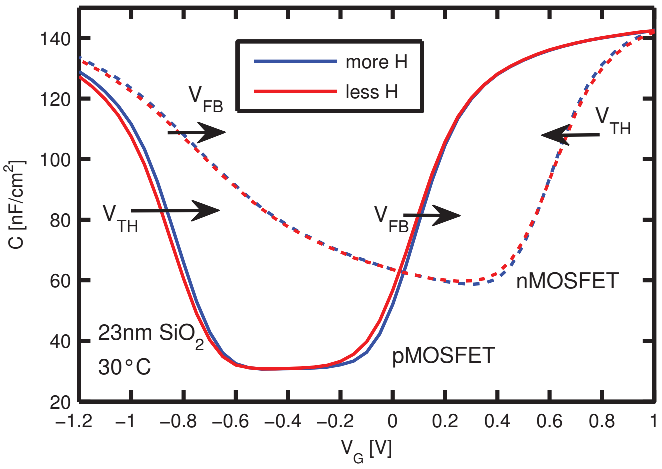

Figure 1. Comparison of MOSFET CV measurements of n- and pMOSFETs on two wafers with more H at the interface (thin Ti–TiN) and less H at the interface (thick Ti–TiN). H reduces positive charge ($\approx 1 \times 10^{10}\,\mathrm{cm}^{-2}$), both at the V_{TH} as well as at the V_{FB} for the pMOSFET and at the V_{FB} of the nMOSFET. The reduction is smaller at V_{FB} of the pMOSFET because of the passivation of amphotheric traps (the P_b center), which are negatively charged when the Fermi level is close to the Si conduction band edge. For the nMOSFET at the V_{TH} the number of interface traps exceeds the number of positive charges which results in net negative charge. Nevertheless also for the nMOSFET positive charges are passivated with H.

III. RESULTS AND DISCUSSION

Fig. 1 shows a comparison of the MOSFET capacitance–voltage (CV) characteristics of virgin devices with thick Ti–TiN layer (less H) against thin Ti–TiN layer (more H). The more H CV characteristics are slightly shifted toward positive infinity over most of the voltage range, except for the nMOSFET around the threshold voltage (V_{TH}). The shift towards positive infinity through passivation with H can be interpreted as creation of negative charge or loss of positive charge. To identify which of those two options is appropriate we have to add information from literature.

Ab-initio calculations have shown that the positive charge

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state H^+ is the only stable state of H in SiO_2 [10]. If interstitial H accounts for the difference in the CV characteristics of Fig. 1 the more H CV characteristic would need to be shifted toward negative infinity, which is the opposite of our experimental result. We therefore rule out interstitially incorporated H near the interface and conclude that all H resides in atomic bindings with other atoms of the solid.

Hydrogen can in principal form a bond with boron (B) doping atoms in the bulk of the Si [11]. This passivates the B acceptor which leads to a decreased doping concentration [11]. A decrease of the doping level decreases the value of the minimal capacitance in a CV measurement. We did not observe any significant decrease of the minimal capacitance of the nMOS CV curve in Fig. 1. We also performed NBTI experiments on devices with and without a surface B implantation of about $1 \times 10^{11}\,\mathrm{cm}^{-2}$ ionized atoms (not shown) and did not observe any differences. We consequently discard the idea that our results are due an interaction of H with doping atoms in Si.

One rather common approach to understand the differences in the virgin CV curves for devices with more or less H at the interface is based on the amphoteric nature of interface traps. We know that H passivates silicon dangling bonds at the Si–SiO_2 interface (P_b centers, interface traps) [4, 7]. These traps are amphoteric, meaning that they are charged positively when the Fermi level is close to the silicon valence band edge and charged negatively when the Fermi level is close to the conduction band edge [12]. If H would passivate only amphoteric P_b centers we would expect positive charge passivation at negative gate voltages and negative charge passivation at positive gate voltages (assuming $V_\mathrm{G}(E_i) \approx 0\,\mathrm{V}$). Since we observe positive charge passivation for a large voltage range we have to conclude that not only amphoteric traps, but also positive charges are passivated through H. Such an effect has already been reported in literature [13, 14]. The actual direction of the shift depends then on the relative quantity of the passivated defects. We therefore suggest that for the nMOS in Fig. 1 the number of passivated amphoteric traps is larger than the number of passivated positive traps.

In order to analyze the electrical properties of the passivated defects, we performed CP measurements with varying frequency f on the two differently passivated devices as depicted in Fig. 2. The device with more H at the interface has a smaller CP current (I_CP) than the device with less H, consistent with earlier results [9]. By analyzing the number of charges pumped per cycle $N_\mathrm{CP} = I_\mathrm{CP}/(qfA)$, which is independent of f for ideal interface traps [15], we observe a strong increase of I_CP with decreasing f for the device with less H at the interface. As opposed to SRH-like interface defects, the frequency dependent increase of the CP current is commonly attributed to the charging and discharging of border traps during the high- and low-time of the CP pulse. The result of Fig. 2 therefore shows that the increased H passivation reduces not only the number of interface traps but also the number of border traps.

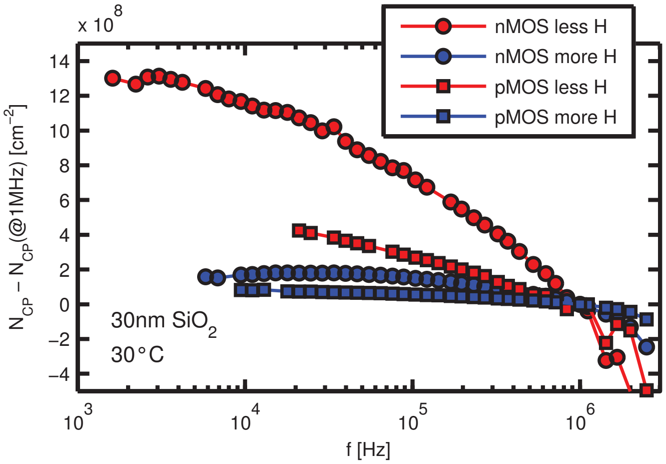

Figure 2. In a frequency dependent charge-pumping experiment the number of charges pumped per cycle N_CP is supposed to stay constant over f if considering interface traps only. Usually, an increase of N_CP with decreasing frequency is observed due to border traps with larger time constants. The characteristics are subtracted with the I_CP value at 1MHz to account for the large difference in virgin interface trap density of the devices (less H: $D_\mathrm{IT} \approx 1 \times 10^{10}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$, more H: $D_\mathrm{IT} \approx 1 \times 10^{9}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$). We observe a large number of border traps on the devices with less H at the interface. This is interpreted in that way that H can also passivate border traps, not only interface states.

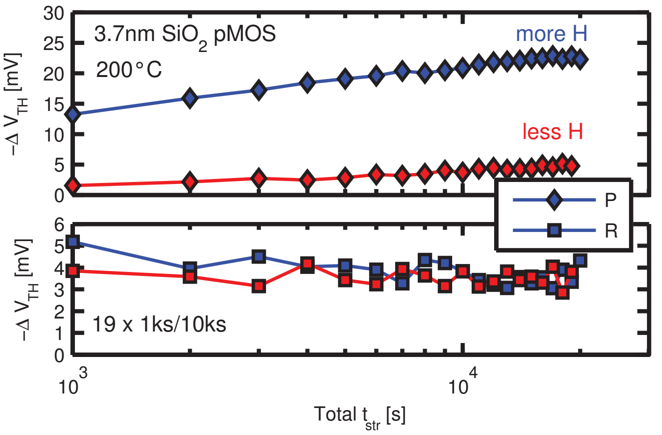

Figure 3. We performed an ultra-low frequency drift experiment where we repeated 1 ks of stress and 10 ks of recovery 19 times (90.9 μHz) without bringing the device a single time into accumulation. We define an estimate for the permanent component as $P = \Delta V_\mathrm{TH}(t_\mathrm{rec} = 10\,\mathrm{ks})$ and an estimate for the recoverable component as $R = \Delta V_\mathrm{TH}(t_\mathrm{rec} = 1.5\,\mathrm{ms}) - P$ arbitrarily based on the defect emission time constants [16, 17]. The experiment reveals that P (defects with emission time constants $\tau_\mathrm{e} > 10\,\mathrm{ks}$) is strongly influenced by H, while R (defects with emission time constants $1.5\,\mathrm{ms} < \tau_\mathrm{e} < 10\,\mathrm{ks}$) is largely unaffected by the H content in the interfacial region. In particular no large loss in recoverable defects is observed.

IV. NEGATIVE BTI

On the pMOSFETs with more/less H we performed an ultra-low frequency NBTI test [16] as depicted in Fig. 3. When we plot the evolution of the recoverable R and the permanent component P (as defined in the caption of Fig. 3) over the cumulative stress time we observe consistent with earlier results [7, 9], that a better H passivated interface experiences much more drift in P and that R is independent of the H budget at the interface. We do not observe a significant decrease of R for the more H wafer, as might be expected when considering models which suggest the lock-in of switching oxide traps [18–20] by the transition of a H atom from a dissociated Si–H bond [6, 7]. We remark that a small decrease of R may be not resolvable considering that only a fraction of the degradation during NBTS is due to Si–H dissociation and the lock-in would happen only for another small fraction of oxide defects. An alternative interpretation of the H independence of R would be that R and P are totally uncorrelated, as recently also stated by Ho et. al. [7, 17].

One might expect that the device with more H at the interface will drift more since it has a larger number of passivated defects which make up the difference to the device with less H at the interface. If H transforms existing defects at the interface to precursors, one single maximum degradation level ($\Delta V_{\mathrm{TH}}^{\max}$) for both device with more or less H is expected. The measurement of $\Delta V_{\mathrm{TH}}^{\max}$ remains unachievable up to date because of rare observations of a decrease in the power law coefficient for NBTI [21, 22]. However, an estimate of $\Delta V_{\mathrm{TH}}^{\max}$ can be given when accelerating the stress with very high stress temperatures, which was shown to considerably reduce the time constants of all defects constituting to NBTI [22]. In Fig. 4 the result of an NBTI test at 400 °C stress temperature is depicted. The high stress temperature is achieved using the poly-heater, a polycrystallin, in situ, local heating structure in the vicinty of the device [23]. The V_{TH} of the device with more H at the interface exceeds the value of the device with less H already after one second of stress at 400 °C. The maximum drift potential of the device with more H at the interface is much larger compared to the device with less H. Hydrogen passivation therefore increases the precursor density for NBTI [8, 9, 14, 24]. The root cause of this effect might lie in the transition reported by Tsetseris et al. based on first-principle calculations [25]: If H breaks up at the Si–$\mathrm{SiO_2}$ interface to passivate a P_b center, the remaining H atom enters a neighboring Si–Si bond, leading to a H bridge in Si. The questions why a hydrogen bridge in Si may be activated through bias temperature stress or if the hydrogen bridge is formed in the $\mathrm{SiO_2}$ and not not in the Si bulk remains unanswered.

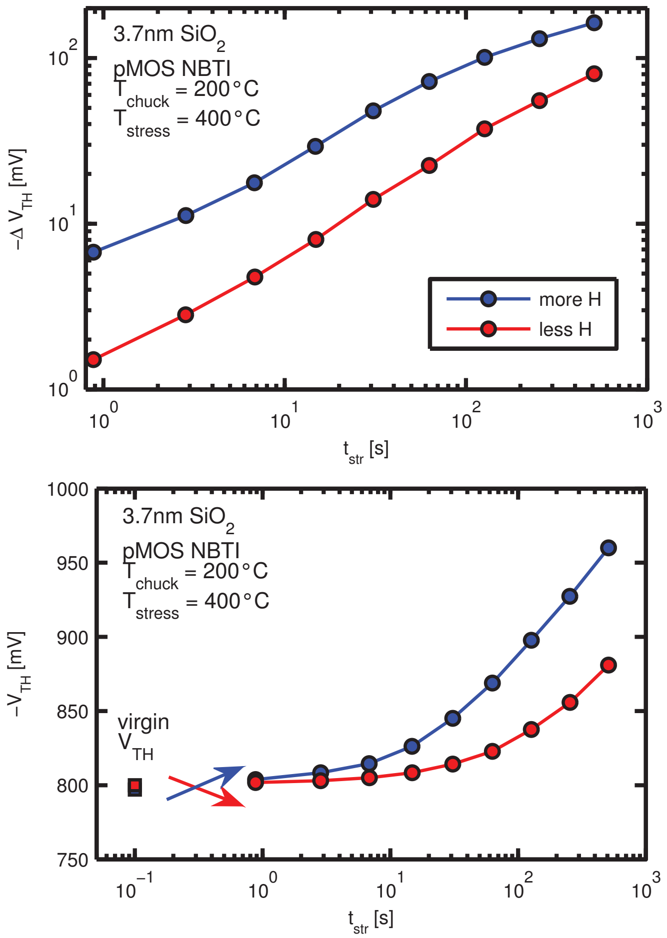

Figure 4. Change of the threshold voltage (top) and the value of the threshold voltage itself (bottom) over the duration of an extreme stress at 400 °C for devices with more or less H at the interface. The top figure shows that a device with a well passivated interface drifts roughly three times more compared to a device with a badly passivated interface. The bottom figure highlights that the drift exceeds the virgin difference in V_{TH} already after roughly one second of stress. This justifies that the H passivation increases the total number of available precursor (and thus the maximum possible drift $\Delta V_{\mathrm{TH}}^{\max}$) for NBTI [24]. The increase is, however, totally due to defects with large time constants, namely P.

V. POSITIVE BTI

We perform our PBTI experiments on nMOSFET devices with an n^{++} doped poly-gate in order achieve a stress situation without any holes on both sides of the gate oxide. Holes may tunnel from a p^{++} doped poly gate toward the Si–$\mathrm{SiO_2}$ interface during PBTS and may cause NBTI-like degradation (creation of donor-like traps) [26, 27], which is undesirable for a PBTI investigation. PBTI in n^{++} gated devices creates acceptor-like traps in both n- and pMOSFETs, which are visible in the ΔV_{TH} only for the nMOSFET [26].

Fig. 5 shows the impact of the H budget on the PBTI drift of nMOSFET devices. The H passivation has the opposite impact on the PBTI compared to NBTI, as we observe less degradation after PBTS for devices on the more H wafer. When we analyze MOS capacitor CV measurements before and after PBTS for more and less H (c.f. Fig. 6) we find that PBTS shifts the flat-band voltage V_{FB} toward the work-function difference value for both groups of wafers. The theoretical value considering only the work function difference is not exceeded, which means that H reduces the number of precursors for PBTI, as in stark contrast to NBTI where the precursor density is increased. We attribute the decrease in PBTI to the passivation of border traps with H. We further argue that we do not create negative charges but passivate existing positive charges through PTBS (c.f. Fig. 7). Due to the decrease in the border trap density with H there are less border traps left which can be neutralized at positive gate bias.

Furthermore, we observe an increase of the CP current

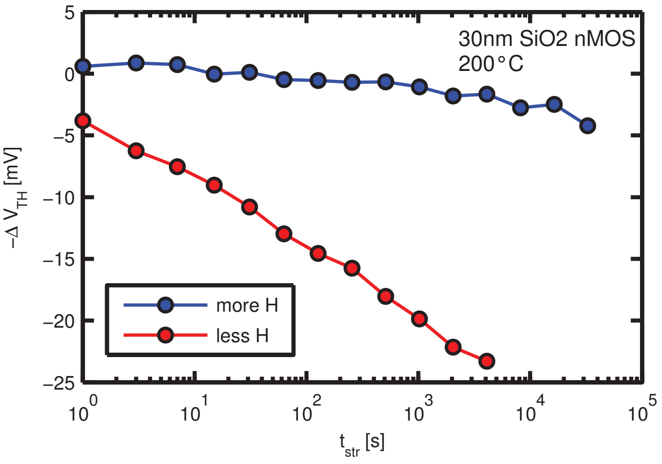

Figure 5. The H passivation degree decreases PBTI. The better the interface is passivated, the better the PBTI behavior of the device. We speculate that the negative charging of a device after PBTI is in fact the loss of positive charges (transforming from positive to neutral state). If H passivates not only interface traps but also positive charges, it becomes clear that a well passivated device can loose less positive charges than a badly passivated device.

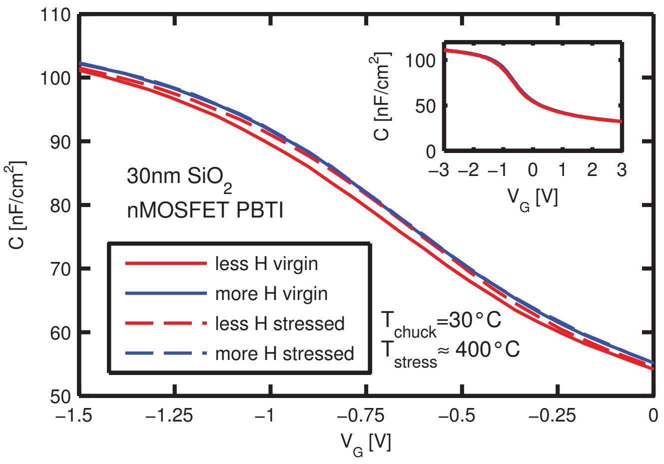

Figure 6. Comparison of CV measurements for nMOSFETs with more/less H at the interface before and after PBTS (full characteristics are depicted in the inset). The unstressed weakly H passivated device has a large number of positive charges and therefore a CV characteristic which resides more towards negative infinity. Those charges may be either be neutralized by H passivation (characteristic of the virgin device with more H) or through PBTS. In both cases we experience roughly the same CV characteristic, with a flat-band voltage very close to the theoretical V_{FB} when considering only the work function difference.

through PBTS [26]. This can be consistently explained with a defect model with 4 different states as depicted in Fig. 8 [1]. PTBS would favor the defects to transfer from the positive stable to the neutral metastable state. In the neutral metastable state charge exchange with the substrate may proceed easily which gives rise to a CP current.

VI. Conclusions

By varying the thickness of Ti–TiN layers during the back end of line processing, we changed the H budget at the Si–SiO$_2$ interface of n- and pMOSFETs. We found that H also

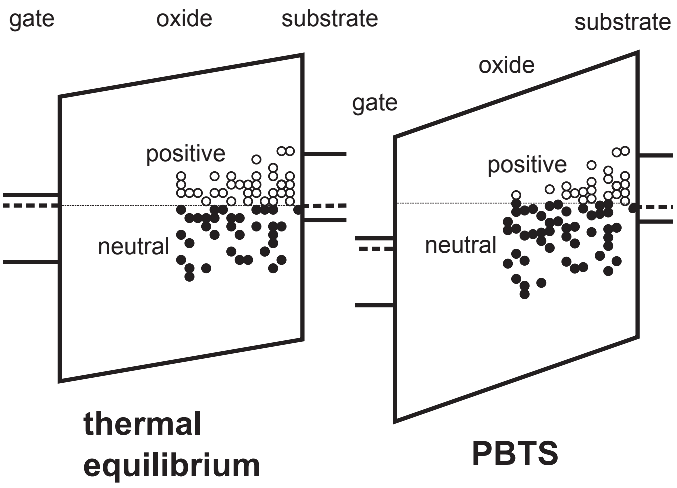

Figure 7. Band diagram of an nMOSFET at thermal equilibrium without any voltage applied to the gate and during positive bias temperature stress. The PBTS fills the positive charge (empty circles) above the equilibrium Fermi level with an electron, which effectively neutralizes the defect (filled circles). The neutralization of the positive charges acts as an apparent negative charge increase for the device.

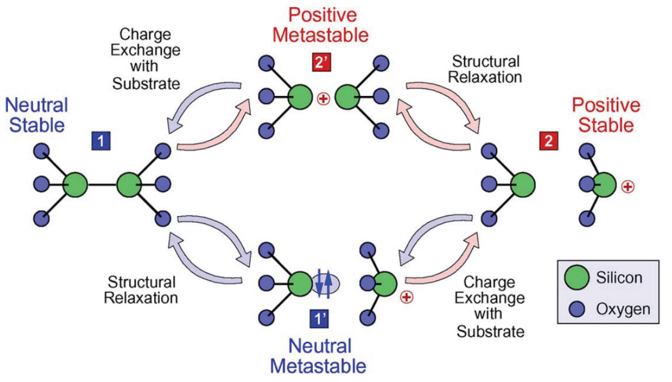

Figure 8. Four state defect model for the switching oxide traps for NBTI after [1]. PBTS increases the charge-pumping current of both n- and pMOSFETs [26] (not shown). This can be consistently explained if we assume that PBTS brings the border traps from the state 2 to the state 1'. In this state the trap can easily exchange charge with the substrate which gives rise to an increased CP current. Recovery is then attributed as the final return of the defect back to the positive stable state 2.

passivates positive oxide (border) traps and not only interface traps.

We studied the influence of H on NBTI and found other indications that H influences mainly the permanent part of NBTI degradation. By performing a high temperature stress, we showed that the H passivation increases the overall drift capability of the device, thus H is creating additional defect precursors at the interface. For PBTI the influence of the H budget is the opposite, i.e. less H at the interface leads to increased PBTI. We attribute this effect to unpassivated positive border traps which are neutralized during PBTS and act as apparent negative charge increase.

ACKNOWLEDGMENT

This work was jointly funded by the Austrian Research Promotion Agency (FFG, Project No. 831163) and the Carinthian Economic Promotion Fund (KWF, contract KWF-1521|22741|34186).

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