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BTI reliability of ultra-thin EOT MOSFETs for sub-threshold logic

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ABSTRACT

A first study of the BTI reliability of a 6 Å EOT CMOS process for potential application in sub-threshold logic is presented. Considerable threshold voltage shifts are observed also for sub-threshold operation. The observed shifts convert to a remarkable current reduction due to the exponential dependence of current on V_{th} in this operating regime. Moreover, the pMOS is observed to degrade significantly more w.r.t. the nMOS device, inducing a detrimental V_{th}-imbalance. A proper device failure criterion is proposed, based on simulation of the DC robustness of an inverter logic circuit.

1. Introduction

One of the most effective methods to enhance the CMOS device performance is by means of scaling the gate oxide thickness. This results in a higher oxide capacitance (C_{ox}) which allows for better electrostatic control and enhanced current drive. Several groups have already demonstrated functional devices with Ultra-Thin Equivalent Oxide Thickness (UT-EOT) down to ~5 Å [1,2]. However, due to the ever increasing oxide electric field (E_{ox}), the reliability issue is becoming a show stopper. In particular, due to Bias Temperature Instability (BTI) [3], a 10 year device lifetime cannot be guaranteed anymore for the ITRS-expected supply voltage (V_{DD}) for standard high-performance logic [4,5].

In the meanwhile, Ultra-Low Power (ULP) operation of digital integrated circuits is receiving a growing interest. This is because ULP has paved the way for many new applications such as wireless sensor networks, biomedical and implantable devices/networks, ambient intelligence, wearable computing, etc.

From a circuit level perspective, ultra-low power operation is enabled by very aggressive supply voltage scaling, down to the threshold voltage and below [6,7]. However, operation in sub-threshold poses many challenges. In general, ultra-low voltage operation limits the DC robustness (i.e. logic noise margin), causes a strong performance penalty and provides no energy gain below a certain voltage. These issues set the limits to the practical voltages that can be employed. For ULP design, a better scalability can be obtained by using devices that are more amenable for aggressive voltage scaling. As already mentioned, in the case of sub-threshold operation, scalability can be improved through a better control of the channel charge. Therefore UT-EOT devices, providing a steeper sub-threshold swing thanks to the tighter electrostatic control, are particularly suitable for sub-threshold operation of ULP applications.

In addition, the reduced operating V_{DD} for ULP design is expected to significantly relieve the reliability issue previously observed for UT-EOT devices. However, a specific device reliability study is needed for the sub-threshold operating regime, due to the atypical reliability specifications imposed by certain ULP applications. In particular, biomedical application will require extended device lifetime (i.e. 100 years for medical implants) but at relatively low operating temperatures (e.g. 55 °C).

Here we present a first study of the BTI reliability of a 6 Å EOT CMOS process for sub-threshold logic. Considerable threshold voltage shifts (ΔV_{th}) are observed even at low V_{GS}, which convert to remarkable current reductions. A BTI induced V_{th}-imbalance is highlighted, being particularly detrimental for sub-threshold logic. A proper device failure criterion is proposed, based on simulated static transfer characteristics of an inverter circuit.

2. Experimental

6 Å EOT pMOS and nMOS devices were used in this work. The gate stack consisted of a thin SiO_2 interfacial oxide layer (IL), a 1.8 nm HfO_2 high-k dielectric layer and a TiN metal gate. The EOT was aggressively scaled by means of IL reduction through an oxygen-scavenging technique. Further details on the process can be found elsewhere [1].

For the BTI assessments, an On-the-Fly (OTF) measurement technique [8], consisting of hysteresis-like traces, was used (see Fig. 1). I_D–V_G traces were recorded up to a stress voltage ($V_{Gstress}$) which was consequently held for a given stress time (t_{stress}) while monitoring the drain current. Finally another I_D–V_G trace was recorded while sweeping back V_G toward 0 V. The initial I_D–V_G

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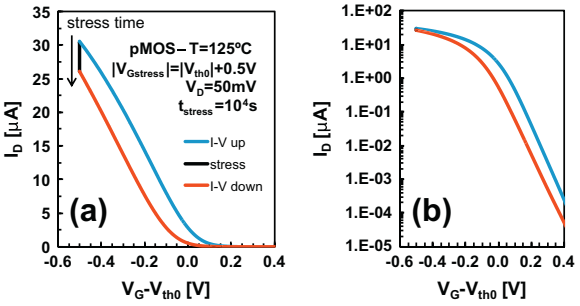

Fig. 1. (a) Hysteresis-like OTF measurement used for BTI assessment. (b) Initial and final I_D–V_G traces shown on a logarithmic I_D axis.

trace was used to convert the drain current reduction during stress to a threshold voltage shift (ΔV_{th}). This conversion, relying on the initial I_D–V_G trace measured on the fresh device, neglects any mobility degradation due to BTI. However, as discussed in [8], this effect can be neglected for low stress voltages as the ones used in this work; on the other hand, this OTF technique is known to introduce an artefact in the measured parameter at short t_{stress} due to unaccounted device pre-stress during the initial V_G ramp up to $V_{Gstress}$. As a consequence, the measured ΔV_{th} deviates significantly from the typically observed BTI power-law-like behavior for short stress time (see Fig. 2). This issue is minimized by increasing the stress time (up to 0.3–1 $\times$ 10^4 s in this work) in order to be able to capture the power-law dependence.

3. Experimental results

In Fig. 3, BTI ΔV_{th} trends measured on pMOS and nMOS devices are shown for two typical $V_{Gstress}$, corresponding to super-threshold and sub-threshold operating regimes. Two main experimental observations can be made. On devices with such aggressively scaled oxide thickness, a significant ΔV_{th} is observed already at the very low gate stress voltage here considered (0.1 V below the fresh device threshold voltage, V_{th0}). Moreover, the pMOS degradation (NBTI) is observed to be $\sim$3$\times$ higher than the one observed for the nMOS (PBTI). This known unbalanced degradation [5] is observed here to be independent of the stress voltage down to sub-threshold operating V_G, as further documented in Fig. 4. Such imbalance is expected to be particularly detrimental for sub-threshold circuit operation, which strongly relies on the n-/p-MOS balance, as discussed in Section 5.

With BTI being a temperature-activated mechanism, the measurements were repeated at three different temperatures (Fig. 5). Interestingly, in the sub-threshold $V_{Gstress}$ regime a very weak temperature dependence was found (estimated ΔV_{th} activation energy

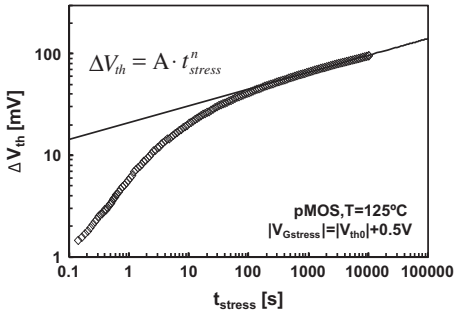

Fig. 2. Typical BTI ΔV_{th} trend measured with the OTF technique. A typical power-law dependence of ΔV_{th} on the t_{stress} is observed for sufficiently long stress times.

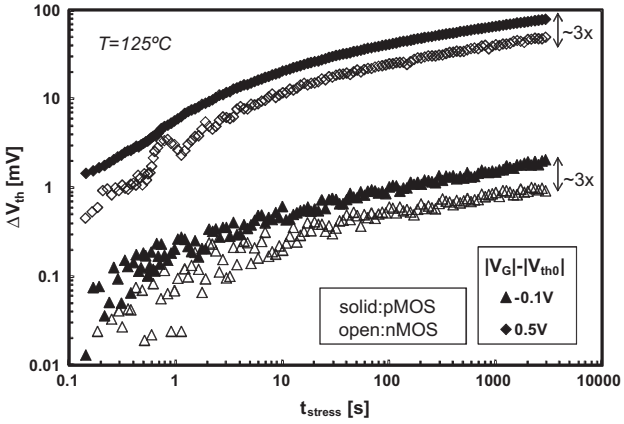

Fig. 3. Measured NBTI and PBTI ΔV_{th} trends for two $V_{Gstress}$ values, above and below the device V_{th0}. A considerable ΔV_{th} is observed also for the sub-threshold stress voltage. In both regimes the pMOS degradation is observed to be $\sim$3$\times$ higher than that of the nMOS.

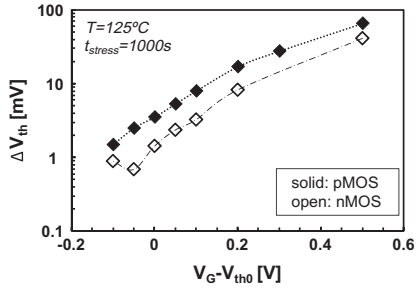

Fig. 4. Measured NBTI and PBTI ΔV_{th} after a fixed stress time. The $\sim$3$\times$ higher NBTI degradation w.r.t. PBTI is consistently observed for the whole $V_{Gstress}$ range considered here.

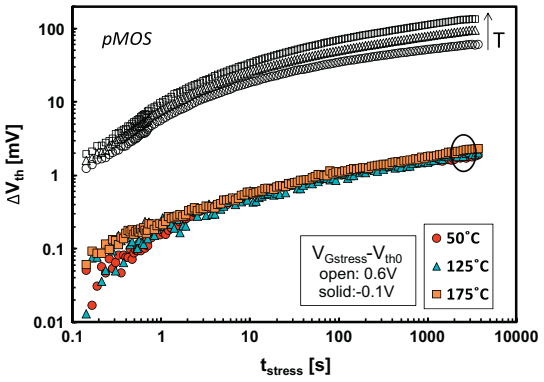

Fig. 5. Measured NBTI ΔV_{th} trends for different operating temperatures. Conversely to the super-threshold $V_{Gstress}$ regime, a very weak T-dependence is observed for sub-threshold $V_{Gstress}$.

$E_A \sim 20$ meV), conversely to the standard super-threshold stress regime where a typical temperature dependence is observed (estimated ΔV_{th} $E_A \sim 80$ meV). We speculate this may be caused by the total degradation being constituted by two different components with different temperature activations, with the dominant component for UT-EOT devices stressed at very low gate voltage having the lowest E_A. It is worth noting that this reduced temperature dependence projects to a weaker reliability relief for ULP applications with reduced operating temperature (e.g. biomedical applications).

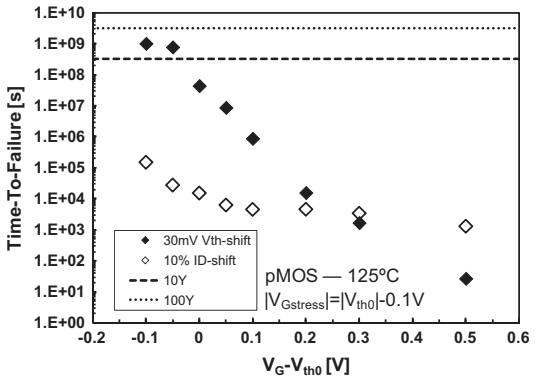

Fig. 6. NBTI time-to-failure projections. Depending on the considered failure criterion (e.g. ΔV_{th} = 30 mV or ΔI_D% = 10%), a significant discrepancy arises for sub-threshold $V_{Gstress}$.

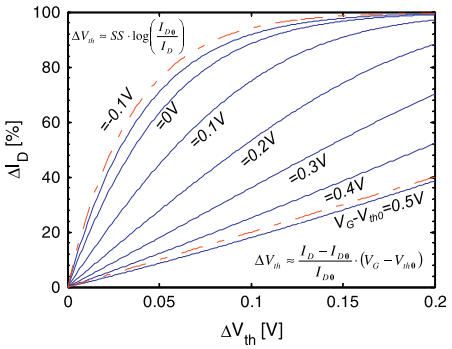

Fig. 7. Correct conversion from ΔV_{th} to ΔI_D% for different operation regime, based on the pristine I_D–V_G trace. The dependence can be modeled with simple equations for the extreme cases (sub-threshold or linear operation, red dash-dotted lines), while it is more complex for the near-threshold operating regime.

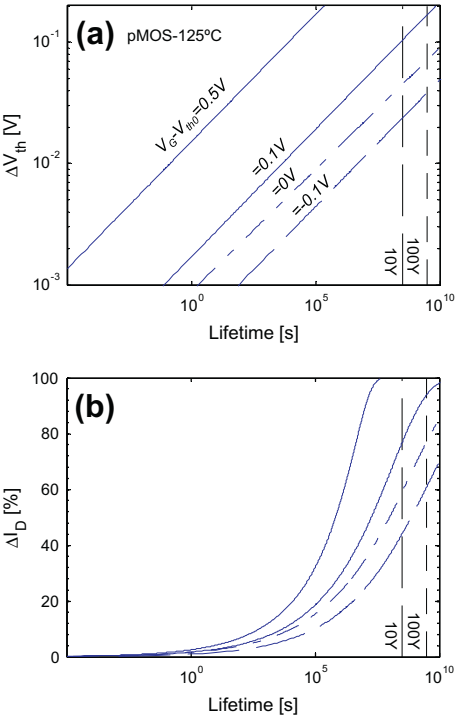

Fig. 8. (a) NBTI power-law extrapolated ΔV_{th} trends vs. the device lifetime, for different operating regimes. (b) Same trends with ΔV_{th} properly converted to ΔI_D% (see Fig. 7). These plots can be used to estimate the device time-to-failure based on application specific failure criteria.

4. Lifetime projections: which failure criterion for sub-threshold logic?

Typically, two failure criteria are alternatively used for BTI assessment: a fixed (e.g. 30 mV) shift of the device threshold voltage or a fixed (e.g. 10%) reduction of the device drive current. Fig. 6 shows the pMOS time-to-failure projections for the two different failure criteria. As one can notice, a significant discrepancy of several orders of magnitude arises for the two failure criteria, particularly in the reduced gate voltage regime. This can be ascribed to the different dependence of the drive current on the device threshold voltage for super- and sub-threshold operating regimes, namely linear and exponential respectively. In Fig. 7 the ΔV_{th} to ΔI_D% conversion is calculated for different operating gate voltages using a measured I_D–V_G curve as a conversion table. While for the two extreme cases the dependence can be easily approximated with simple equations (i.e. Super-threshold: $\Delta V_{th} \approx (V_G - V_{th0})\cdot(I_{D0}-I_D)/I_{D0}$; Sub-threshold: $\Delta V_{th} \approx SS\cdot\log(I_{D0}/I_D)$; red[1] dash-dotted lines in Fig. 7), for near-threshold operating regimes (typically of interest for ULP applications) the dependence is more complex.

As observed above, for the gate voltage regimes of interest for ULP applications, the choice of the failure criterion strongly affects the extrapolated time-to-failure. Therefore we propose that an application-specific failure criterion be chosen based on simulation at the circuit level, as discussed in the next section. It is useful then to plot the expected degradation in terms of both ΔV_{th} and ΔI_D% as a function of the device lifetime. This is done in Fig. 8, converting the measured ΔV_{th} power-laws on stress time to ΔI_D% evolutions through the above described procedure (see Fig. 7). In such a way the shift of these two important device electrical parameters is readily readable as a function of the device lifetime.

While the ΔV_{th} information can be used for DC robustness considerations (i.e. logic circuit noise margins, see next section), the ΔI_D% can be used for delay considerations (i.e. logic gate rise/fall times).

5. Static characteristics of a CMOS inverter operated in sub-threshold: BTI impact on noise margins

The numerical approach described in [9] was used here to calculate the static input–output characteristic of a CMOS inverter operated with a $V_{DD} = V_{th0} - 0.1$ V. A complete experimental $I_D(V_{GS}, V_{DS})$ characterization of fresh pMOS and nMOS devices with L = 70 nm and W = 90 nm from the same UT-EOT wafer was used in order to derive the inverter static characteristics. The V_{th0} of pMOS and nMOS were numerically matched in order to have a perfect p-/n-MOS balance at time-zero. Then, a range of V_{th}-imbalance values were introduced in order to compute the static characteristic degradation caused by BTI. The results are shown in Fig. 9. For increasing p-/n-MOS V_{th} imbalance values, the characteristic is shifted to the left. This effect is readily quantified in the Noise Margin figure of merit [10], shown in Fig. 10 for different degradation levels. The low noise margin (NM_L) is reduced for increasing V_{th}-imbalance while the high noise margin (NM_H) improves. A hard BTI failure criterion can be then set at NM_L = 0, i.e. for a p-/n-MOS V_{th}-imbalance of ~95 mV. Recalling the ~3× factor experimentally observed for NBTI ΔV_{th} w.r.t. PBTI ΔV_{th} (see Figs. 3 and 4), the failure criterion can be converted to $\Delta V_{th\_pMOS} \approx 143$ mV. This failure criterion, based on the DC robustness of a CMOS

[1] For interpretation of color in Fig. 7 the reader is referred to the web version of this article.

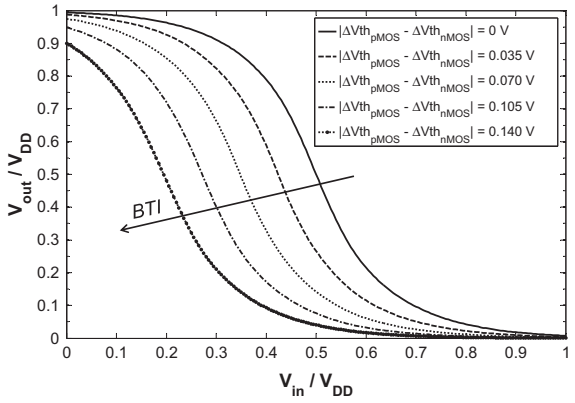

Fig. 9. Static characteristics of an inverter operated in sub-threshold ($V_{DD} = V_{th0} - 0.1$ V). The initial characteristic is computed from an extensive set of measured p-/n-MOS $I_D(V_{GS}, V_{DS})$ curves. A perfect match of the initial V_{th0}s is assumed; then an increasing p-/n-MOS V_{th}-imbalance is introduced in order to evaluate the degradation of the static characteristic due to BTI.

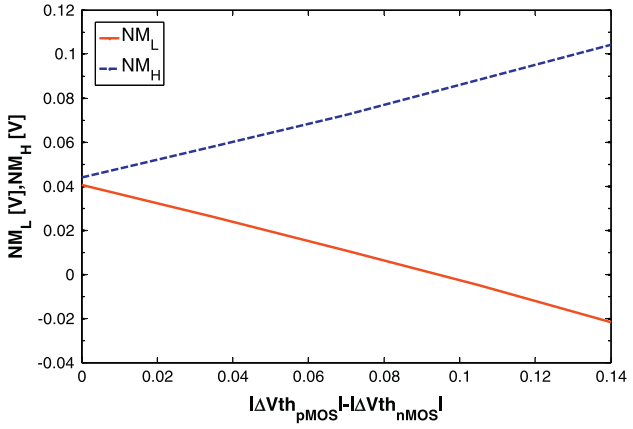

Fig. 10. Computed inverter static noise margin for increasing p-/n-MOS V_{th}-imbalance. Due to stronger NBTI, the low-to-high noise margin is expected to reduce. As a first approximation (neglecting device-to-device variability), a hard failure criterion can be set for the ΔV_{th} which causes $NM_L = 0$.

inverter, can be used in order to assess from Fig. 8a the UT-EOT device time-to-failure for sub-threshold operation. As one can see the 6 Å EOT device meets a 100 year lifetime for near $-V_{th0} \times V_{DD}$.

However, it is worth noting that such failure criterion does not take into account safety margins necessary to account for device-to-device variability in nanoscaled technologies. A proper safety margin could be set assuming a pre-existing p-/n-MOS V_{th}-imbalance, e.g. equal to two times the sum of the standard deviations of the n- and pMOS V_{th0}-distributions [$=2(\sigma_n + \sigma_n)$]: in such way, assuming uncorrelated V_{th0}-variabilities, the unlucky probability of having a pMOS with V_{th0} higher than the average plus two sigmas (=2.275%) and simultaneously a nMOS with V_{th0} lower than the average minus two sigmas (=2.275%) is safely limited to ~0.05%. Hence the actual aging ΔV_{th} failure criterion will be significantly reduced.

Finally, we note a similar approach can be used in order to determine an alternative ΔI_D% failure criterion (see Fig. 8b) based on delay considerations from time-based circuit simulations.

6. Conclusions

A study of the BTI reliability of a 6 Å EOT CMOS process for sub-threshold logic was presented. Considerable ΔV_{th} was observed, which also converts to considerable ΔI_D% for this operating regime. The BTI-induced V_{th}-imbalance was highlighted, being particularly detrimental for sub-threshold logic. An application-specific device failure criterion was proposed, based on simulated static transfer characteristics of an inverter.

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