

Local Oxide Capacitance as a Crucial Parameter for Characterization of Hot-Carrier Degradation in High-Voltage n-MOSFET

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Hot-carrier degradation (HCD) is associated with the build-up of interface states and oxide trapped charges (with densities N_{it} and N_{ot}) of an MOS transistor. Therefore, quantitative information on the defect spatial distributions is essential to reveal and understand the physical mechanisms of the HCD phenomenon. For this purpose, the charge-pumping (CP) technique is widely used [1]. Most methods for extraction of the lateral defect profiles from CP data employ a constant transistor oxide capacitance, namely $C_{ox} = \epsilon_{ox}/t_{ox,0}$, where $t_{ox,0}$ is the oxide thickness at the center of the device and ϵ_{ox} is the dielectric permittivity (e.g. [2]). In such an approach the MOS structure is considered as an ideal infinite parallel-plate capacitor or, in other words, the oxide electric field is assumed uniform. However, accounting of the fringing effect is of great importance for the characterization of the defect spatial distributions after hot-carrier stress because the $N_{it}(x)$ peak is located near the drain end of the gate [1]. In literature we were able to find consideration of the oxide capacitance coordinate dependence only in the work of Lee *et al.* [3]. This approach is based on the simulation of the local threshold voltage shift induced by the given uniform oxide charge distribution and requires adequate computational resources. Thus, an compact analytical model for simplification of the defect profile extraction technique is of great importance even nowadays. For the solution of this problem we use the conformal-mapping method which is most helpful for fringing the electric field in simple 2D boundary conditions [4]. Following the standard calculation procedure [4], the $C_{ox}(x)$ can be then defined as

$$\left. \begin{aligned} x &= t_{ox,1}(x)(\varphi + \exp(\varphi))/\pi \\ C_{ox}(x) &= \epsilon_{ox}/(t_{ox,1}(x) + t_{ox,1}(x)\exp(\varphi)) \end{aligned} \right\} \quad (1)$$

Oxide thickness of transistor is interpreted as $t_{ox,1}(x) = t_{ox,0} + \Delta t_{ox}(x)$, where $\Delta t_{ox}(x)$ is the thickness gradient component, which increases closer to the end of the gate contact. For validation of the developed analytical approach we use two 5V n-MOSFETs with identical architecture differing only in channel lengths ($L_{ch} = 0.5$ and $2.0 \mu\text{m}$). The drain-sided gate edge is the origin of the x -axis for both devices. Transistors were fabricated on a standard $0.35 \mu\text{m}$ technology and subjected to a hot-carrier stress at the gate voltage $V_{gs} = 2.0\text{V}$ and the drain voltage of $V_{ds} = 6.25\text{V}$ up to 10^5s . For charge-pumping current measurements we use an experimental scheme suggested in [5].

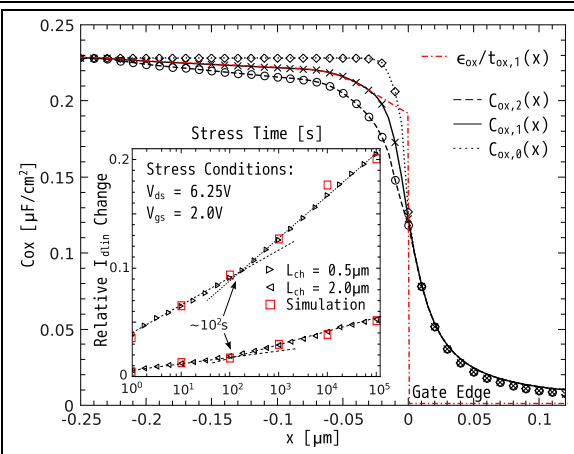


Fig.1. The $C_{ox,\{0,1,2\}}(x)$ (indexes correspond to the considered oxide thicknesses) calculated using the approach of [3] (symbols), compared with the developed analytical model (lines) in the case of $L_{ch} = 0.5 \mu\text{m}$. Inset: the relative I_{dlin} change vs. stress time - experiment and simulation results for $L_{ch} = 0.5$ and $2.0 \mu\text{m}$.

Additionally, to ensure that the device geometrical peculiarities are taken into account, a parametric system (1) was examined on the two artificial devices with $L_{ch} = 0.5 \mu\text{m}$ but with different oxide thicknesses of $t_{ox,0}(x) = t_{ox,0}$ and $t_{ox,2}(x) = t_{ox,0} + 2\Delta t_{ox}(x)$. A comparison of the simulation approach [3] and model (1) for $t_{ox,\{0,1,2\}}$ shows a good agreement in Fig.1.

For characterization of the $N_{it}(x)$ evolution with the stress time we employed the analytical $C_{ox}(x)$ distributions incorporated into the scheme described in [5]. One can see in Fig.2 that the extracted defect profiles features two peaks starting from $\sim 10^2\text{s}$. Moreover, Fig.2 demonstrates that these peaks just correspond to the maxima of the electron and hole acceleration integrals [6]. This result is confirmed by the findings of our HCD model [6] which shows that these peaks are related to the contributions induced by primary channel electrons and secondary generated holes. The obtained defect profiles were subjected to further validation as input parameters to simulate the I_{dlin} degradation. Comparison of simulated and experimental curves once again confirms the applicability of the developed model (see Fig.1, inset). It should be noted that the change of the I_{dlin} degradation slope appearing at $\sim 10^2\text{s}$ for both devices can be linked to the contribution of the hole N_{it} peak to the total defect density.

We have shown that the accurate consideration of the oxide capacitance dependence on the lateral coordinate is essential for the proper extraction of the defect profiles from CP data. Presented analytical model for $C_{ox}(x)$ was verified by representing I_{dlin} degradation in 5V n-MOSFETs with various channel lengths. Obtained results demonstrate a good agreement with our physics-based HCD model.

References

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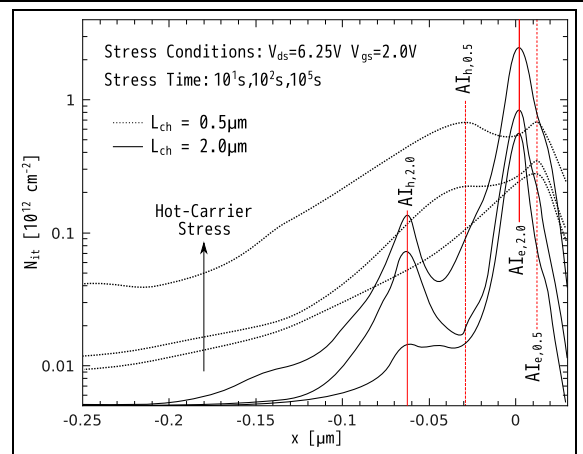


Fig.2. The evolution of interface state density profiles with stress time for $L_{ch} = 0.5$ and $2.0 \mu\text{m}$. Peaks of $N_{it}(x)$ correspond to the maxima of electron ($AI_{e,\{0.5,2.0\}}$) and hole acceleration integrals ($AI_{h,\{0.5,2.0\}}$) [6].