Superior Reliability and Reduced Time-Dependent Variability in High-Mobility SiGe Channel pMOSFETs for VLSI Logic Applications

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***Abstract*—With a significantly reduced Negative Bias Temperature Instability, SiGe channel pMOSFETs promise to virtually eliminate this reliability issue for ultra-thin EOT devices. The intrinsically superior NBTI robustness is understood in terms of a favorable energy decoupling between the SiGe channel and the gate dielectric defects. Thanks to this effect, a significantly reduced time-dependent variability of nanoscaled devices is also observed. Other reliability mechanisms, such as Channel Hot Carriers, Time-Dependent Dielectric Breakdown and Low-Frequency noise are demonstrated not to be showstoppers. Finally the performance improvement promised by the SiGe technology is discussed from the perspective of VLSI logic circuits.**

Keywords-NBTI, pMOSFET, Reliability, High-Mobility Channels, SiGe, Ge, Time-Dependent Variability, Aggressive Voltage Scaling, VLSI.

I. INTRODUCTION

Due to the ever increasing electric fields in scaled CMOS devices, reliability is becoming a showstopper for further scaled technology nodes [1]. Although several groups have already demonstrated functional devices with aggressively scaled EOT down to ~5Å [2,3], a 10 year device lifetime at operating conditions cannot be guaranteed anymore. Meanwhile, the use of high-mobility channels is being considered for further CMOS performance enhancement [4]. The SiGe channel quantum well (QW) technology (Fig. 1) in particular is considered for yielding enhanced mobility and pMOS threshold voltage tuning [5].

We show that this technology also offers a significant intrinsic reliability improvement and we ascribe to a reduced interaction between channel carriers and oxide defects. Furthermore, it also considerably alleviates the time-dependent variability [6], which arises as devices scale toward atomistic dimensions [7]. Finally, we explore the potential of this technology from a VLSI logic circuit perspective, noting that its speed advantage will be further accentuated at reduced supply voltages [8]. All these aspects make the SiGe technology a very promising successor to Si.

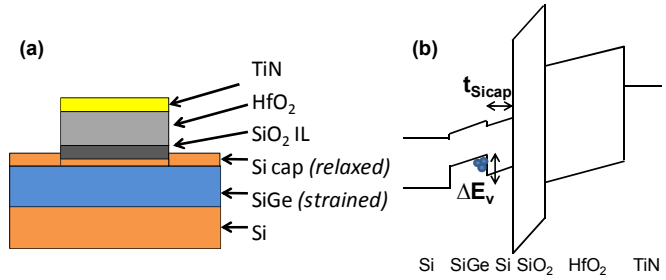

Fig. 1. (a) Gate-stack sketch of the SiGe devices used in this work. (b) Band diagram in inversion. Channel holes are confined into the SiGe QW thanks to the valence band offset (ΔE_v) between the SiGe channel and the Si cap. The Si cap thickness (t_{Sicap}) therefore contributes to the T_{inv} of the gate stack.

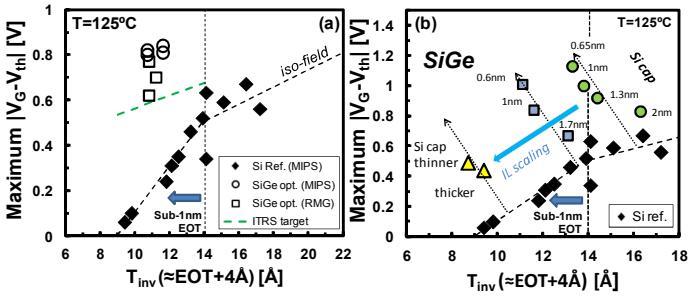

Fig. 2. (a) Due to severe NBTI, ultra-thin EOT Si channel pMOSFETs do not allow for a 10 year lifetime at the ITRS specified operating voltage. Conversely, optimized ultra-thin EOT SiGe channel pMOSFETs show significantly reduced NBTI, clearly exceeding the operating voltage target. The reliability improvement is consistently reproduced for different process thermal budgets and for both a Metal Inserted Poly-Si (gate-first) and a Replacement Metal Gate (gate-last) process flows. (b) A reduced Si cap thickness was consistently observed to consistently yield improved NBTI robustness over a wide range of EOT, obtained by means of SiO_2 interfacial layer (IL) scaling.

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II. NEGATIVE BIAS TEMPERATURE INSTABILITY

Negative Bias Temperature Instability (NBTI) is considered as the most severe reliability issue for scaled CMOS technologies [9]. It affects pMOSFETs during operation, causing significant shifts of the device electrical parameters (e.g., threshold voltage shift ΔV_{th}) due to oxide defect charging and interface state creation. The quasi-constant supply voltage scaling proposed by the International Technology Road Map [10] for the recent technology nodes enhances NBTI due to the ever increasing oxide electric field (E_{ox}). As a consequence, a 10 year lifetime at operating conditions cannot be guaranteed anymore for Si channel pMOSFETs with ultra-thin (UT-) EOT (Fig. 2 diamonds).

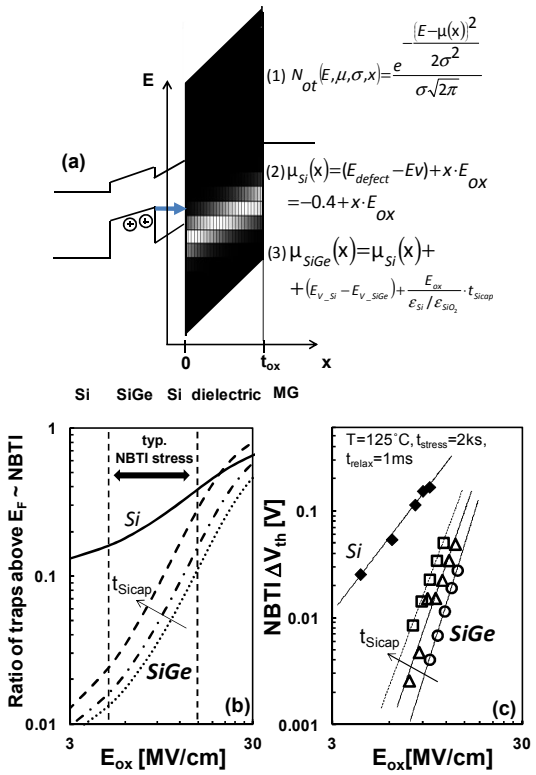

Fig. 3. (a) A model including a defect band in the dielectric centered at -0.4eV below the Si valence band as observed in [15]. The Fermi level in the channel determines which part of the defect band is energetically favorable for trapping channel holes. The defect band is modeled as a Gaussian distribution over energy (eq. 1), with its mean modulated by the E_{ox} (eq. 2), by the valence band offset between the SiGe and the Si, and by the Si cap thickness (eq. 3). (b) The ratio of accessible oxide defects can then be calculated as a function of the E_{ox} for the SiGe channel (with different Si cap) and for the Si ref. devices. *The calculation favorably compares with (c) the experimental data for SiGe devices with varying Si cap thickness.*

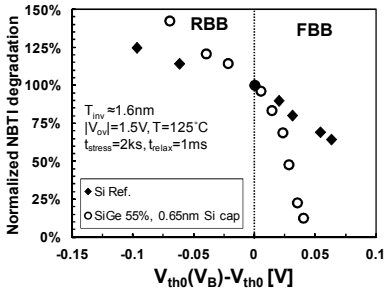

Fig. 4. The Body-Bias (BB) technique is used to modulate the device V_{th} for high-performance or low-power applications. By modulating the space charge region, it also modulates the oxide electric field (E_{ox}) at a constant gate overdrive voltage [16]. Due to the stronger NBTI-electric field dependence observed in SiGe pMOSFETs, a stronger NBTI modulation by BB is also observed. In particular a Forward Body Bias (FBB) significantly reduces NBTI, while a Reverse Body Bias (RBB) enhances the device degradation. Note: measured NBTI V_{th}-shifts were normalized to the respective V_B=0V cases and plotted vs. the BB V_{th0}-modulation.

Already in 2009 [11], we reported that the Ge-based technology promises a significantly improved NBTI robustness. To benefit from this property, the SiGe QW gate-stack was optimized for enhanced reliability, including a high Ge fraction (55%) in the channel, a sufficiently thick QW (6.5nm) and a Si passivation layer of reduced thickness (0.8nm) [12,13]. By means of such optimization, we demonstrated sufficiently reliable ultra-thin EOT SiGe pMOSFETs with a 10 year lifetime at operating conditions in both gate-first and gate-last process flows (Fig. 2a) [14]. The main gate-stack parameter affecting the NBTI robustness was found to be the Si passivation layer thickness, with thinner Si caps consistently observed to yield a significant boost of the device reliability also at UT-EOT (Fig. 2b). Furthermore, the reliability improvement was observed to be process- and architecture- independent, proving to be an intrinsic property of the Ge-based technology, and therefore readily transferable to various device architectures such as pure Ge-channel pMOSFETs and SiGe pFinFETs [14].

We have ascribed this intrinsic reliability improvement to a reduced interaction between channel carriers and defects in the gate dielectric. In particular, assuming the existence of a defect band in the dielectric centered below the Si valence band (as observed e.g. in [15]), fewer defects are energetically favored for trapping holes from the SiGe channel, thanks to the higher Fermi energy of holes in the small-bandgap SiGe QW (Fig. 3a). This simple model readily explains all the experimental observations, including the impact of different Ge fractions, QW thickness, and Si cap thickness on the device NBTI reliability (Fig. 3b&c).

Finally, it is worth noting that the stronger NBTI dependence on the oxide electric field observed in SiGe devices (Fig. 3 b&c), has further benefits for NBTI alleviation. In particular, the Forward Body Bias technique can be used very efficiently to further reduce NBTI on SiGe devices without compromising the device performance (i.e. fixed gate overdrive voltage), Fig. 4 [14].

III. TIME-DEPENDENT VARIABILITY

With the ever decreasing device size, the number of dopant atoms, but also the number of defects, in each device reduces to numerable levels [7]. This results in increased time-zero (i.e., as-fabricated) variability, but also considerable time-dependent variability (i.e., reduced reliability) [6]. We and others have recently shown that the properties of individual charged gate oxide defects can be observed in the NBTI ΔV_{th} relaxation transients [6,17]. A representative set of typical NBTI relaxation transients recorded on nanoscaled SiGe devices is shown in Fig. 5a. Several observations can be made: 1) the total ΔV_{th} observed after the same NBTI stress strongly varies from device to device; 2) single discharge events are visible, each causing a different ΔV_{th} step; 3) each device shows a different number of charging/discharging events (i.e. a different

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number of *active* oxide defects); 4) the ΔV_{th} step heights appear to be approx. exponentially distributed (Fig. 5b), with single charged oxide defects easily causing gigantic ΔV_{th} due to the percolative nature of the channel current associated with Random Dopant Distribution (RDD) in the nanoscaled devices.

SiGe pFETs with a reduced Si cap thickness showed a ~10× reduced average number of charge/discharge events per device (i.e. a reduced average number of *active* defects, $<N_T>$) and a ~2× reduced average ΔV_{th} step height (η) w.r.t. their Si counterparts (Fig. 6). These two experimental observations are readily explained with the model already discussed in the previous Section (see Fig. 3): fewer oxide defects are energetically favorable for SiGe channel holes, with the accessible defects located on the gate side of the dielectric, thus yielding a reduced ΔV_{th} [17].

Thanks to the reduced $<N_T>$ and η, the optimized SiGe channel technology promises a significantly enhanced reliability when considering a realistic population of billions of nanoscaled devices, as illustrated in Fig. 7 [18].

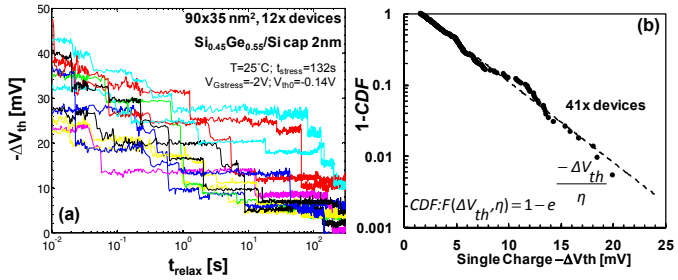

Fig. 5. (a) NBTI relaxation transients recorded on nanoscaled SiGe devices, with abrupt, single discharge events visible. (b) The single charge ΔV_{th} step heights appear to be exponentially distributed, with an average ΔV_{th} step height η≈3.4mV.

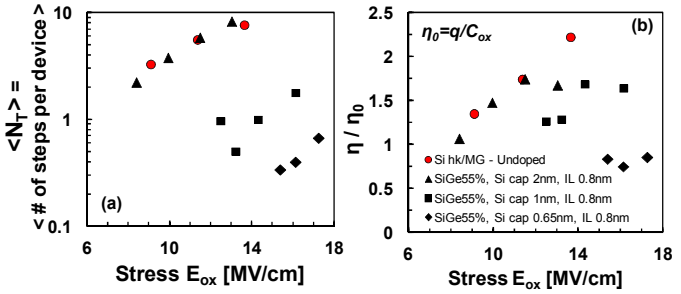

Fig. 6. (a) Nanoscaled SiGe channel pMOSFETs with a reduced thickness of the Si passivation layer show a significantly reduced (~10×) average number of active oxide defects w.r.t. their Si counterparts. (b) SiGe devices also show a reduced (~2×) average ΔV_{th} step height per charged oxide defect (η). Note: the experimentally observed η values were normalized over the simple electrostatic charge sheet expectation $\eta_0=q/C_{ox}$.

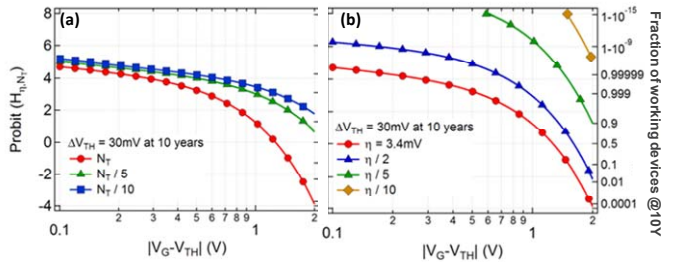

Fig. 7. Calculated fractions of working nanoscaled devices (failure criterion: ΔV_{th}=30mV) after 10 year operation as a function of the operating overdrive [18]. Showing a ~10× reduced $<N_T>$ and a ~2× reduced η, SiGe devices promise a significantly improved lifetime distribution.

IV. Other Reliability Mechanisms

A. Channel Hot Carriers (CHC)

The use of a small bandgap semiconductor favors electron-hole pair generation in the channel by means of impact ionization. This effect is expected to enhance hot carrier degradation. As a consequence, poor hot carrier robustness has been reported for pure Ge-channel devices [19]. However, during a typical CHC stress (V_G=V_D=V_{stress}) a significant fraction of the total degradation in pMOS devices is related to the residual NBTI effect at the source side of the channel [20]. The enhanced NBTI robustness of the optimized SiGe devices significantly reduces also the total degradation caused by CHC stress. As we reported in [13], CHC do not constitute a showstopper for the optimized SiGe devices reliability.

B. Low-frequency noise

Similarly to BTI, 1/f noise is ascribed to trapping and de-trapping of channel carrier into oxide defects with widely distributed characteristic time constants. The reduced interaction between carriers and oxide defects observed for SiGe devices—thanks to the energy decoupling (see Fig. 3)—also yields a reduced 1/f noise, as we showed in [13].

C. Time-Dependent Dielectric Breakdown (TDDB)

As already noted for Ge devices in [11], no significant difference in the TDDB characteristic of SiGe devices w.r.t. their Si counterparts was observed [13]. Although a few soft breakdown events could be expected (<100cm^{-2} in 10 years for a 6Å EOT technology at nominal V_{DD}), TDDB is not considered a showstopper for UT-EOT devices [21].

V. Speed Potential of VLSI Circuits With SiGe pMOSFETs Under Aggressive Voltage Scaling

For an early performance evaluation of a novel technology the I_{ON}=I_D($|V_{GS}|$=$|V_{DS}|$=$V_{DD\_nominal}$) figure of merit is widely used in the electron device community. However, during the real operation of a logic circuit, the devices may operate with several combinations of $|V_{GS}|$ and $|V_{DS}|$ (e.g., low-to-high transition of an inverter output). In addition to this, dynamic voltage scaling techniques are widely used in VLSI circuits to reduce the power consumption. Consequently, evaluating the performance of a technology only at the nominal supply voltage might be too simplistic.

In this section we discuss the evaluation of the performance improvement of a logic inverter gate when the Si pMOSFETs is replaced by a SiGe channel device. The analysis is based on wafer-level I-V measurements of individual transistors, according to the methodology described in [8]. The logic gate output load was assumed to be dominated by the gate capacitance of the next stage (i.e., the considered logic gate is driving adjacent cells). The comparison was performed equalizing the threshold voltage and the supply voltage for both SiGe and Si technologies.

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The speed benefit brought by the SiGe pMOSFET can be intuitively grasped by inspecting Fig. 8, where the ratio I_D/C_G between the on-current and the gate capacitance of SiGe normalized to the Si counterpart is plotted as a function of V_{SD} and V_{SG}-$|V_{th}|$ voltages. From this figure the largest speed improvement (up to 1.91×) is observed at low V_{SD}, whereas a significantly smaller improvement (down to 1.28×) is observed at high V_{SD} where I_{ON} is normally evaluated.

This superior performance at low V_{SD} can be proficiently exploited for aggressive V_{DD} scaling (see Fig. 9). Moreover, the higher speed improvement at low V_{SD} is expected to considerably enhance other important figures of merit of logic gates which include transient device biasing at varying V_{SD} (i.e. dynamic operation). This can be noted in Fig. 9 by looking at the gate delay (defined as the time need to pull-up the inverter output voltage from 0V to $V_{DD}/2$) or the gate rise time (defined as the time need to pull-up the inverter output voltage from 10% to 90% of V_{DD}) figures of merit.

VI. Conclusions

With a superior NBTI robustness, a reduced time-dependent variability, and yielding a significant performance enhancement of VLSI logic circuits at reduced V_{DD}, SiGe channel technology is a very promising alternative to Si pMOSFETs for the next generations of VLSI systems.

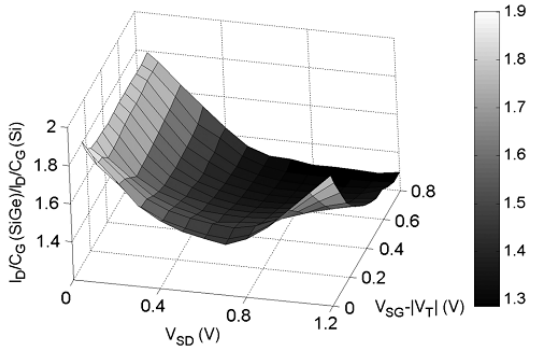

Fig. 8. Ratio of I_D/C_G between SiGe and Si pMOSFETs as a function of the bias voltages, V_{SD} and V_{SG}-$|V_{th}|$. The normalization of the drain current for the gate capacitance (I_D/C_G) has been obtained by multiplying the drain current by the capacitance-equivalent thickness in inversion (I_DT_{inv}). The large speed improvement observed at low V_{SD} (up to 1.91×) is strongly reduced at high V_{SD} (down to 1.28×). Note: the speed improvement observed at low V_{SG}-$|V_{th}|$ and high V_{SD} is due to differences in the DIBL behaviors.

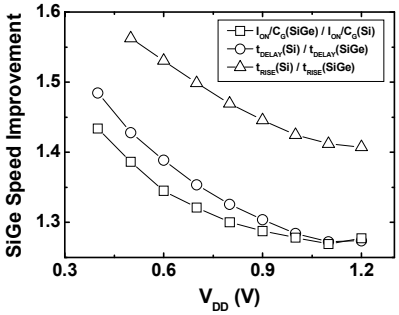

Fig. 9. Speed advantage of SiGe pMOSFET w.r.t. Si for an inverter logic gate in terms of ON-current, delay time, and rise time, as a function of V_{DD}. The speed improvement of SiGe significantly increases with V_{DD} scaling.

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