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METROLOGY REQUIREMENTS FOR MANUFACTURING 3D INTEGRATED CIRCUITS

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ABSTRACT

Three-dimensional integrated circuits (3D ICs) introduce wafer bonding and Through Silicon Vias (TSVs) as new modules, thus extending manufacturing requirements beyond CMOS. A 3D IC with a photosensor is taken as an example to further analyze the resulting new metrology requirements for mass production. For the wafer bond module, data on defects before and after bonding, bond interface adhesion strength, and the module, thickness control for deposited layers and defect metrology including the trench sidewall and bottom are identified as key requirements. Mass production requires non-destructive inline metrology in all cases. This has been achieved for electrical parameters, bond void (Scanning Acoustic Microscopy), and TSV depth monitoring (optical methods). Other parameters such as bond strength, as well as layer thickness or defect metrology inside TSVs, demand further R&D.

INTRODUCTION

Recently there has been a strong trend from classical packaging using bond-wires towards Wafer Level Packaging (WLP) using bumps. This is mainly driven by form factor and cost reduction. Additional Through Silicon Via (TSV) technology has enabled a conductive path connecting wafer front side and back side. This allows the placement of electrically functional structures on both sides of a chip as well as the stacking of chips to form 3D ICs. Open TSVs with Cu or W liner and Cu or W filled TSVs have emerged as the two main concepts [1], [2]. Likewise high density "TSV middle" [3] for memory or processor stacking and lower density "TSV last" [4] e.g. for sensor integration have emerged as the two main process integration schemes. The general metrology requirements are, however, very similar for all of these concepts because of the identical TSV and bond interface topography.

3D INTEGRATED CIRCUIT

BASIC STRUCTURE AND PROCESS FLOW

As an example for manufacturing requirements, a 3D integrated photosensor connected to an IC via an open TSV (Fig.1, [5]) has been chosen.

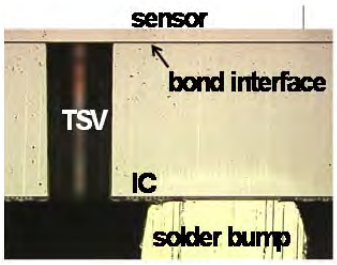

FIGURE 1. Cross-section of a 3D IC and a photosensor connected by an open TSV.

Key non-CMOS process modules are wafer to wafer (W2W) bonding and TSV formation (Figure 2, [5]).

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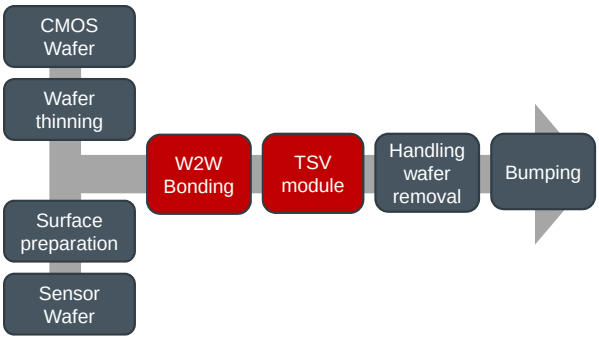

FIGURE 2. Schematic process flow for the 3D IC with photosensor and TSV from Figure 1.

ELECTRICAL CHARACTERIZATION

Important parameters are the TSV resistance, the leakage current to the Si bulk, and the TSV breakdown voltage [6]. The TSV resistance is routinely measured in a production environment.

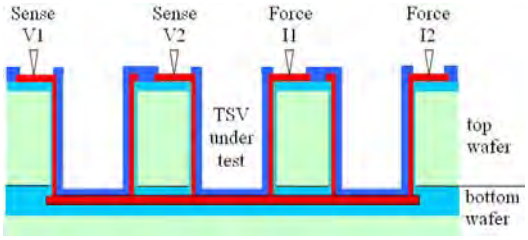

FIGURE 3. 4-point measurement enables precise contact resistance measurement on TSVs [6].

Two additional TSVs are used for forcing a current on the one hand and measuring the potential on the other hand (Fig. 3). Thus a high precision resistance measurement can be established. Figure 4 shows the TSV resistance distribution of 11.000 TSVs.

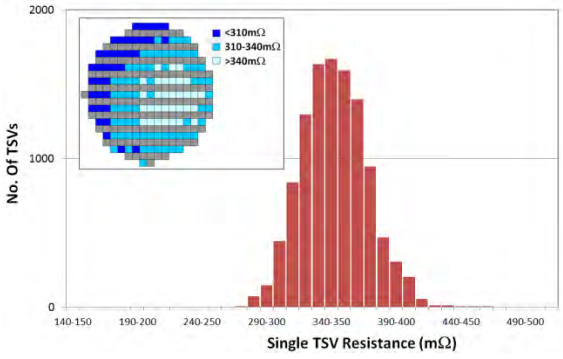

FIGURE 4. TSV resistance distribution [6].

The measured TSV resistance of 350mOhm aligns well with theoretical calculations for the materials used. Reliability investigations comprising thermal cycling, environmental stress, and thermal aging did not show any degradation.

IN-LINE METROLOGY

WAFER BONDING

Different bonding methods for CMOS compatible processing have recently been developed [7]. Temporary handling wafers, for example, may be attached to a CMOS wafer via adhesive wafer bonding. Due to the relatively thick polymer layer the requirements relating to surface topography and particle density are not very high. The demand on bond quality is considerably higher, if the bond interface remains part of the final product, such as in the case of direct wafer to wafer bonding (Fig.1) or metal bonding (e.g. Cu-Cu bonding). Control of bond quality is mandatory in such cases. Non-bonded areas (bond voids) must be minimized and the bond strength must be maximized close to the level of monolithic material. Bond defects smaller than 100x100µm^2 can be detected by C-mode Scanning Acoustic Microscopy (C-SAM, Fig. 5).

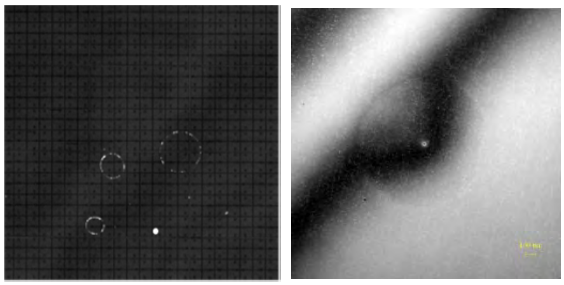

FIGURE 5. C-SAM image of bond defects: drying residues (left), particle in the bond interface (right).

While bond voids can be measured in-line, no non-destructive technique exists for determining the bond strength. Instead the tests rely on mechanically separating the bonded parts. While several methods exist, the only one satisfying the demand for robust measurements is the micro chevron test [8], [9]. Chevron structures are formed by patterning the bond oxide (Fig. 6 (left)). After bonding, external forces are applied. The maximum load needed to break the micro chevron structure is then recorded as a measure for the bond strength.

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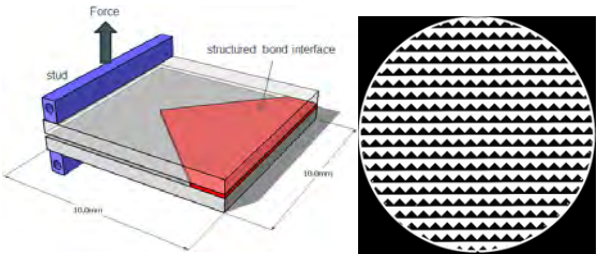

FIGURE 6. Chevron test structure (left) and C-SAM measurement at wafer level (right).

Chevron structures can be measured for test wafers to characterize a bond process (Fig.6, right). For product wafers a non-destructive method would be needed. Therefore some further work to provide a non-destructive bond strength analysis, e.g., by C-SAM was proposed [10].

THROUGH SILICON VIA (TSV) MODULE

TSV processing comprises the key process steps of Si Deep Reactive Ion Etching (DRIE) forming a trench, isolation layer deposition and etch, barrier layer deposition (TiN, Ta, ...), metal deposition (W, Cu, ...) , and passivation layer formation. The only structural difference is that metal is either deposited as a liner (open TSV, Fig.1) or used to fill the TSV explaining similar metrology requirements. An inherent issue of DRIE is the formation of scallops due to the switching between etching and sidewall passivation cycles. Defects include side wall damage during DRIE due to insufficient passivation, and residuals.

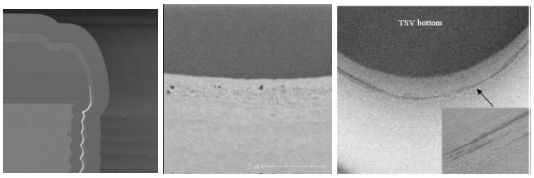

FIGURE 7. Scallops (left), particles and damage (center) and residuals inside the TSV (right).

Therefore, inspection after TSV etching and cleaning is required. For deposited layers, film thickness measurements and defect inspection is also mandatory. Side wall inspection can be performed by methods such as tilted SEM. The trench depth and the TSV bottom can be inspected using optical tools such as spectrophotometers and interferometers [11].

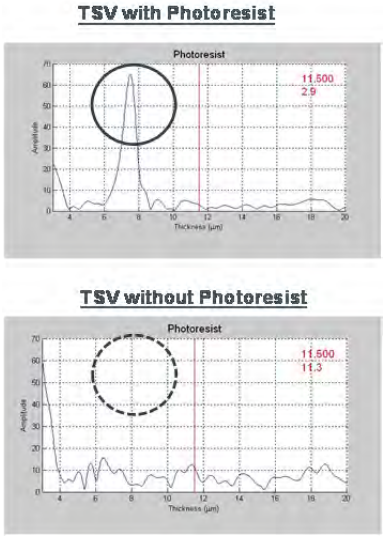

FIGURE 8. Resist thickness measurements at the TSV bottom using a commercial white light spectrophoto-meter [11].

Results for non-destructive in-line resist thickness measurements inside the TSV are shown in Fig. 8.

CONCLUSIONS

Various 3D IC metrology methods already exist. Cost reduction in manufacturing 3D ICs will benefit from further metrology R&D especially for non-destructive bond strength as well as defect- and film thickness measurements inside TSVs.

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KEYWORDS

metrology, 3D, Integrated Circuit, manufacturing, Through Silicon Via, wafer bonding