Silicon Spintronics and its Applications

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Continuous miniaturization of CMOS devices effectuated the breath taking increase in performance of integrated circuits. Numerous tough problems were solved on this exciting journey; however, growing technological challenges and soaring costs will gradually bring CMOS scaling to an end. This puts foreseeable limitations to the future performance increase, and research on alternative technologies and computational principles becomes paramount.

The spin of an electron possesses several exciting properties suitable for future devices. It is characterized by only two projections on a chosen axis – up or down, and it can change its orientation rapidly by utilizing an amazingly small amount of energy. Employing spin, as a compliment to electron charge, opens an exciting opportunity for developing conceptually new non-volatile nanoelectronic devices for future low power applications [1].

Silicon, the main material of microelectronics, is characterized by weak spin-orbit interaction and zero-spin nuclei, which gives rise to a long spin lifetime. This long spin lifetime makes silicon perfectly suited for spin-driven applications. Experimentally at low temperatures, spin propagation through an undoped bulk silicon wafer of 350μm thickness has been already demonstrated [2], [3]. Coherent spin propagation over such long distances makes the fabrication of spin-based switching devices in the near future increasingly likely.

The spin field-effect transistor (SpinFET) proposed by Datta and Das [4] is a switch which employs the electron spin to modulate the current through the device. The SpinFET is composed of a semiconductor channel region sandwiched between two ferromagnetic contacts. The source contact injects spin-polarized electrons in the semiconductor. The gate-voltage-dependent spin-orbit interaction in the channel is used to modulate the current through the SpinFET. It causes the electron spin to precess during the electron propagation through the channel. Only the electrons with their spins aligned to the drain contact's magnetization can leave the channel through the drain contact, thus contributing to the current.

For a practical realization of a SpinFET it is therefore mandatory to resolve the problem of spin injection into the channel and spin detection as well as spin propagation, control, and spin manipulation [5], [6].

The impedance mismatch [5] between ferromagnets and semiconductors has long hampered the experimental observation of electrical spin injection into silicon. The first successful demonstration in 2007 of spin injection into undoped silicon employing the method of hot electrons [3] allowed circumventing the impedance mismatch. Two years later a successful demonstration of all-electrical spin accumulation in *n*- and *p*-doped silicon by injection trough a tunnel barrier at room temperature was reported [6]. The key was optimizing the contact resistance such that it is not too small to evade the impedance mismatch, and that it is not too large to prevent thermionic emission and to keep tunneling currents detectable [5]. Recently, spin accumulation at elevated temperature up to 500K was reported [7]. Spin injection and detection in lateral structures [8] and silicon nanowires [9] has also been just reported. Alternative ways to inject spin in silicon by spin pumping [10] and thermal Seebeck spin tunneling [11] can be applied to develop conceptually new power- or energy-efficient spin devices.

Successful spin injection into a number of semiconductors was demonstrated by using different materials for ferromagnets and dielectrics in the tunnel contacts [4], [9],[12]. Regardless undoubted progress in electrically creating spin currents in semiconductors by means of tunnel contacts, several important issues are yet to be resolved. One of them is the level of spin accumulation which displays several orders of magnitude discrepancy [4], [13] with the standard theory. Experimental indications of a strong decrease in spin injection efficiency at elevated temperatures [9] suggest that further efforts in careful understanding, design, and fabrication of high quality tunnel contacts are urgently needed.

Close to interfaces the spin diffusion length and relaxation time at room temperature appear to be shorter with a much weaker temperature dependence than in the bulk [8]. Thus, external spin relaxation mechanisms due to the presence of a Si/SiO_2 interface become central, and methods to boost the spin lifetime in MOSFETs are needed. We utilize a spin-dependent **k·p** Hamiltonian [13-18], where only the [001] valleys are included. Without strain the unprimed subbands are degenerate. This degeneracy produces a large mixing between the spin-up and spin-down states from the opposite valleys, resulting in hot spots characterized by strong spin relaxation induced by surface roughness scattering taken proportional to the derivatives of the wave functions at the interface [19]. The hot spots are defined by zeroes of $D\varepsilon_{xy} - \hbar^2 k_x k_y \left(\frac{1}{m_t} - \frac{1}{m_0}\right)$, where D = 14eV is the shear strain deformation potential, m_t is the transverse mass, and ε_{xy} is shear strain. In strained samples the hot spots are moved away

from the center of the two-dimensional Brillouin zone, which reduces their contribution to spin relaxation. Thus, strain used to enhance on-current in nano-CMOS can significantly boost spin lifetime [18].

For building a SpinFET, a purely electrical spin manipulation in the channel is required. The spin-orbit interaction controlled by the gate voltage is an option. However, the channel length required to rotate the spin substantially by the electric field dependent spin-orbit interaction must be in the order of several microns even for the optimum channel orientation [20]. The only viable option left to use nano-CMOS is likely to convert a MOSFET to a Spin-MOSFET by adding the spin degree through introducing ferromagnetic source and drain contacts [21]. The current in this structure depends on the relative orientation of the magnetizations of source and drain pawing the path towards programmable non-volatile logic. The contact magnetization direction can be switched electrically by using spin torque transfer. However, due to the low spin injection efficiency at room temperature, the Spin MOSFET has not yet been realized.

Many new ideas to build spin-based devices have been recently introduced [22-30], however, much more efforts are required to better understand their operation mechanisms and bringing them to applications. In order that these new devices can be commercially successful, they need to fulfill several important requirements. Room temperature operation, compatibility with CMOS, and non-volatility are desirable must. Although significant progress in understanding spin injection, transport, and detection in silicon has been achieved, more research is urgently needed to boost the spin injection efficiency at room temperature and to resolve the issue of spin manipulation by pure electrical means. Albeit many exciting inventions are lying ahead, the viable practical option for the near future is to benefit from combining CMOS with magnetic tunnel junctions (MTJs). MTJ-based spin transfer torque MRAM is CMOS compatible, non-volatile, and, most importantly, close to production. A combination of a MTJ with a MOSFET to a pseudo-spin-MOSFET circuit can mimic the behavior of the Spin MOSFET [21]. Even more, arrays made of MTJs open new opportunities to built non-conventional non-volatile logic-in-memory systems [31].

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