Modeling Spin-Based Devices in Silicon

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Continuous miniaturization of CMOS devices made the breath taking increase in performance of integrated circuits become a magnificent reality. Numerous tough problems were solved on this exciting journey; however, growing technological challenges and soaring costs will gradually bring CMOS scaling to an end. This puts foreseeable limitations to the future performance increase, and research on alternative technologies and computational principles becomes paramount.

The spin of an electron possesses several exciting properties suitable for future devices. It is characterized by two projections on a chosen axis – up or down, and it can change its orientation rapidly by utilizing an amazingly small amount of energy. Employing spin, as a compliment to electron charge, opens new exciting opportunity for developing conceptually new non-volatile nanoelectronic devices for future low power applications [1].

Silicon, the main material of microelectronics, is characterized by weak spin-orbit interaction and zero-spin nuclei, which gives rise to a long spin lifetime. This makes silicon perfectly suited for spin-driven applications. Spin propagation through an undoped 350μm thick silicon wafer [2] gives hope for fabrication of silicon spin-based devices in the near future increasingly likely.

The success of microelectronics has been assisted by smart Technology Computer-Aided Design tools. Because a commercial support for spin applications is entirely absent it is mandatory to develop a simulation environment for spin-based devices in silicon [3]. Understanding spin-polarized transport in silicon and in compatible hysteretic materials facilitates inventing, modeling, and optimizing prototypes of spin-based switches and memory devices for the 21st century.

The canonical spin field-effect transistor (SpinFET) proposed by Datta and Das [4] is a switch which employs the electron spin to modulate the current through the device. The SpinFET is composed of a semiconductor channel region sandwiched between two ferromagnetic contacts. The source contact injects spin-polarized electrons in the semiconductor. The gate-voltage-dependent spin-orbit interaction in the channel is used to modulate the current through the SpinFET. It causes the electron spin to precess during the electron propagation through the channel. Only the electrons with their spins aligned to the drain contact's magnetization can leave the channel through the drain contact, thus contributing to the current. For practical realization of a SpinFET it is mandatory to solve the problem of spin injection and detection as well as spin propagation, control, and manipulation [5]. Successful spin injection from different ferromagnets into a number of semiconductors through several oxides has been demonstrated [5-7]. Regardless the undoubted progress, the level of spin accumulation which displays several orders of magnitude discrepancy [5] with the standard theory is not yet understood.

Close to interfaces the spin diffusion length and relaxation time at room temperature appear to be shorter with much weaker temperature dependence than in the bulk [7]. Thus, external spin relaxation mechanisms due to the presence of a Si/SiO_2 interface become central, and methods to boost the spin lifetime in MOSFETs are needed. We utilize a spin-dependent **k·p** Hamiltonian [8], where only the [001] valleys are included. Without strain the unprimed subbands are degenerate. This degeneracy produces a large mixing between the spin-up and spin-down states from the opposite valleys, resulting in hot spots characterized by strong spin relaxation. The hot spots are defined by the condition $D\varepsilon_{xy} - \hbar^2 k_x k_y \left(\frac{1}{m_t} - \frac{1}{m_0}\right) = 0$, where D = 14eV is the shear strain deformation potential, m_t is the transverse mass, and ε_{xy} is shear strain. In strained samples the hot spots are moved away from the center of the two-dimensional Brillouin zone (Fig.1), which reduces

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their contribution to spin relaxation. Thus, strain used to enhance on-current in nano-CMOS can significantly boost spin lifetime [9] (Fig.2).

The spin-orbit interaction in silicon films is due to the interface-induced inversion symmetry breaking [10]. Silicon nanowires with [100] orientation display a stronger modulation of the conductance as function of spin-orbit interaction and are preferred for practical realizations of SpinFETs [11]. However, the channel length required to manipulate spin is about a micron. The spin degree can be introduced into nano-CMOS by using ferromagnetic source and drain contacts [1], however, due to the low spin injection efficiency at room temperature [12], it has not yet been realized. Many new ideas to build spin-based devices have been recently introduced [5], [13]. To be successful, these devices must operate at room temperature and be compatible with CMOS. Albeit many exciting inventions are lying ahead, the practical option for the near future is to benefit from combining CMOS with magnetic tunnel junctions (MTJs). MTJ-based spin transfer torque MRAM is CMOS compatible, non-volatile, and close to production. A combination of a MTJ with a MOSFET to a pseudo-spin-MOSFET appears to be very beneficial [14]. Arrays made of MTJs offer new opportunities to build non-conventional non-volatile logic-in-memory systems [15].

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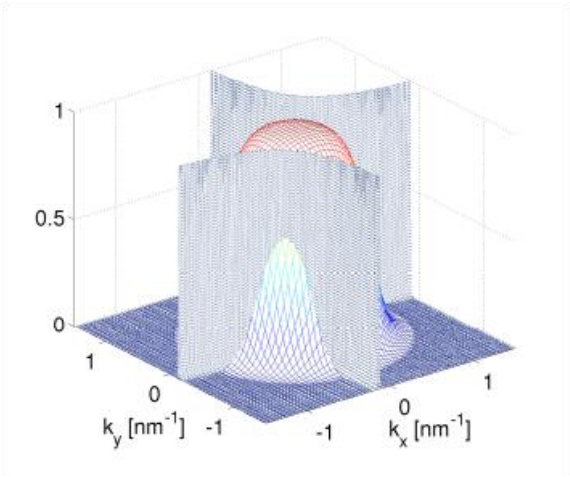

Fig. 1. Spin relaxation hot spots in strained samples.

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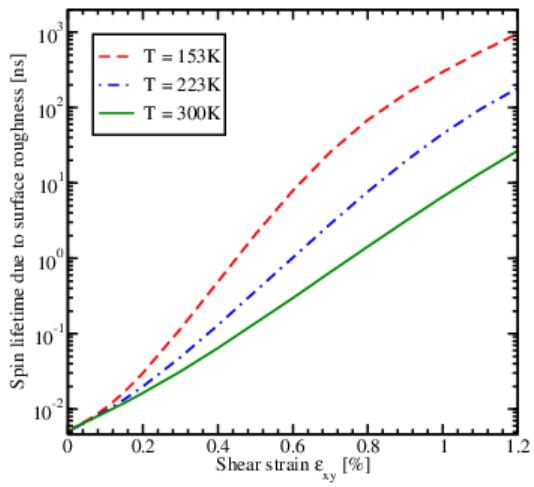

Fig. 2. Spin lifetime enhancement by shear strain.