Impact and measurement of short term threshold instabilities in MOSFETs of analog circuits

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ABSTRACT

Short term threshold instabilities may cause erratic behavior in analog circuits like comparators and analog-to-digital-converters. As conventional characterization procedures have not been appropriately sensitized to such issues, this kind of erratic behavior usually only occurs in products where it is very difficult to identify. Therefore, for example prior to the introduction of a new gate stack, it is essential to do a careful experimental characterization of short term threshold instabilities, which goes beyond standard NBTI or PBTI measurements. A reliable forecast of the effect of threshold instabilities on the performance of analog circuits will require circuit simulations taking the threshold instabilities into account.

I. INTRODUCTION

Threshold shifts ΔV_{th} of MOSFETs due to NBTI and PBTI are determined in general for accelerated stress conditions and for long stress times of typically 10,000 s. The ΔV_{th}'s of interest typically are in the regime of 30mV (for 30nm-CMOS) to 100mV (for 90nm-CMOS), corresponding to fail criterions for digital circuits.

In analog circuits, however, even threshold voltage shifts on the order of 1mV, much smaller than the ones leading to failure of digital circuits, may cause failure. This fact has hardly been acknowledged or investigated.

These threshold voltage shifts in the mV-regime, caused by very short stress pulses at nominal operation voltage are the topic of this work. To demonstrate its importance, we begin by giving an example where these small ΔV_{th}'s occur and can cause failure. As the measuring technique to detect these ΔV_{th}'s with sufficiently accurate resolution is non-standard, it will be explained in detail in section III. Time, electric field and temperature dependencies will be discussed in section IV and an overview over the different technologies will be given in section V, followed by the conclusions.

II. IMPACT of SHORT TERM ΔV_{th}

As mentioned above, a considerable impact of threshold hysteresis is not expected in digital circuits. In logic gates, only minor delay changes may occur, and in flip-flops setup time violations could result in a design with very small timing margins. In SRAM cells, read failures can occur, as has been shown in [1].

In most analog circuits, gate-source as well as drain–source voltages are much smaller than the supply voltage, so no effects are to be expected. But in operational amplifiers operated in open loop configuration, almost the full supply voltage may occur at one of the inputs, giving rise to an asymmetric threshold shift, i.e. to an offset between the two input terminals. Permanent degradation and hysteresis effects for this configuration have been reported in [2, 3], respectively. This operation mode occurs in comparators and can lead to faulty output of analog to digital converters. Commonly, there are offset compensation circuits which sense the offset in one clock phase and add a corresponding signal to the input in the next clock phase. At the end of this second phase, the comparator makes its decision. Therefore, slowly varying, permanent offsets do not represent a cause of error. But this is different for a dynamic offset since the compensation refers only to the V_{th} shift at the end of the compensation phase. If V_{th} changes during the second clock phase, the decision made by the comparator may be wrong. To give a quantitative example: The comparator in a successive approximation converter (see Fig.1) has to compare the reference signal from the DAC to the input voltage. The error due to the offset of the comparator must not change by more than **½ of the converter's LSB** (i.e. ½ the resolution) during the different stages of the conversion (i.e. decisions about all bits MSB down to LSB). It is worth mentioning that an erroneous decision may impact not only the LSB but all bits up to the MSB.

To summarize this section: for the above DAC example the stress "seen" by the comparator input stage may be in the regime of V_{dd}, it lasts for a stress time on the order of 1µs, and a ΔV_{th} built up during this time corresponding to a voltage ½*LSB might cause errors. For a 10-bit converter and a technology with V_{dd}=1V this value is V_{dd}/1024=1mV.

As a consequence for the measurement, in order to do a meaningful assessment of short term threshold instabilities, our measurement technique must be able to detect ΔV_{th}'s of less than 1mV, and the resolution should be only a fraction of this 1mV. ΔV_{th}'s must be measured after well defined stress- and recovery times, which should be as short as possible, both extended down to the µs-regime.

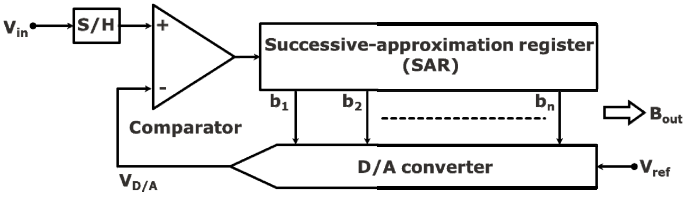

Fig. 1: N-bit successive approximation analog-to-digital converter (ADC) showing with an analog comparator. The comparator compares ADC's input to the output of the internal digital-to-analog converter (DAC). The worst case asymmetric stress signal to the comparator occurs when V_{IN} is at V_{dd}-level and V_{DAC} is at ½*V_{dd} (for a full scale input of V_{dd}).

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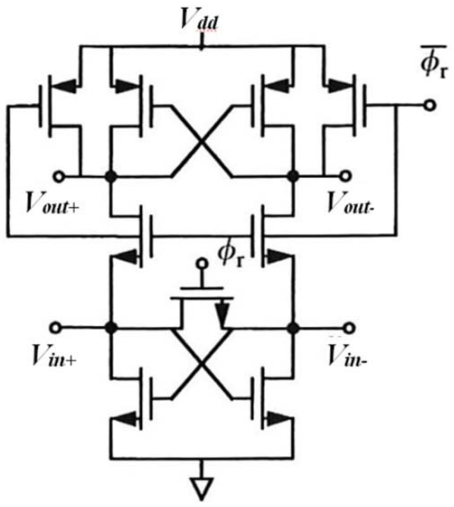

Fig. 2: Example for the input stage of the comparator of Fig.1. With the worst case asymmetric stress condition described in Fig.1, the negative input V_{in-} experiences a considerable ΔV_{th} in a short stress time while the ΔV_{th} of the positive input is close to zero. Thus the offset voltage of the comparator changes by the value ΔV_{th} during stress and recovers fast after the end of stress. [15]

III. MEASUREMENT TECHNIQUE

Short term threshold instabilities, often called hysteresis, due to short stress pulses and measured with short recovery times have been characterized before [4-6]. Clearly any attempt to determine this short term hysteresis with standard analyzers is useless, since ΔV_{th} vanishes almost completely after a 1ms measuring delay (compare Fig. 4). So far the fast-ramp technique [4-7] has been employed to determine the threshold hysteresis. This technique applies fast up/down ramps – using a pulse generator – to the gate of the MOSFET under test and simultaneously records the drain current – using a digital storage scope – while ramping. The disadvantages of this technique are:

i) The noise amplitude generated by a pulse generator is on the order of 10mV in the MHz frequency range. This is more than one order of magnitude higher than the noise of a good quality DC voltage source. Note that this pulse generator has to provide the stress voltage as well as the "readout" voltage (which is critical to noise). Thus – as seen in [6, Fig. 9], for example – the ΔV_{th} resolution achieved by these fast-ramp techniques is no better than 20 mV. Compared to the goal defined in section II of detecting 1mV ΔV_{th}'s with a 0.1mV resolution this resolution is insufficient. In fact the ΔV_{th}'s around 1 mV cannot be detected at all by the fast ramp technique.

ii) The fast ramp techniques produces a hysteresis curve that allow the extraction of a ΔV_{th}. Due to the up/down ramps there is no well-defined stress- and recovery history correlated to this ΔV_{th}. That is, it is not possible to say that this specific ΔV_{th} has been produced by applying a stress pulse of a given height and width and a given recovery time. Or vice versa the ΔV_{th} produced by a given stress pulse and recovery cannot be determined.

iii) The recovery is not directly and continuously monitorable, and thus a separation or observation of trapping of positive and negative charge at the same time is not possible.

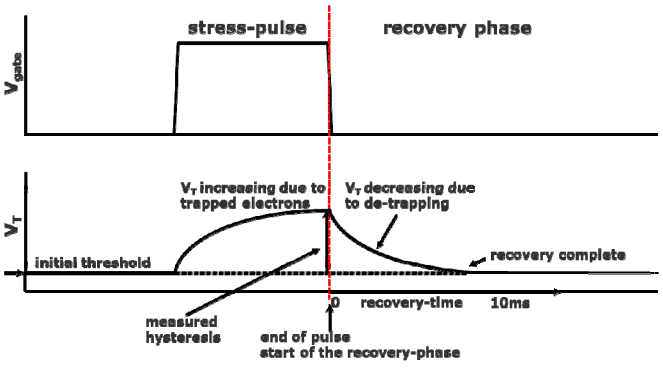

Fig. 3: Timing of a measurement and effect on V_{th} caused by a single stress pulse (schematic)

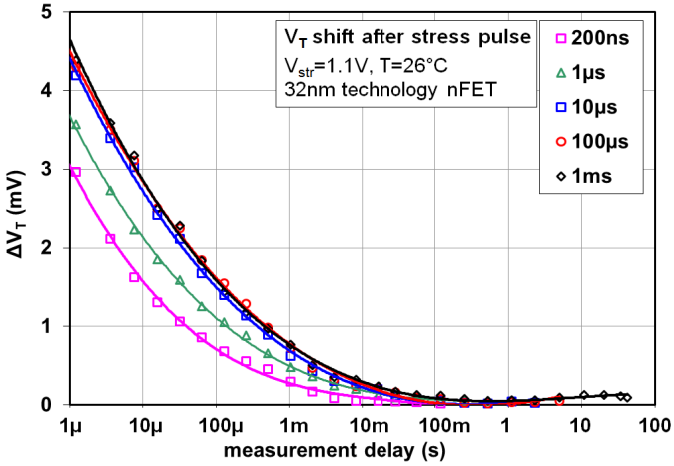

Fig. 4 –Example for recovery curves after short stress pulses. The width of the stress pulses is given in the legend. Each curve is the average over a number of 32...100 single recovery traces.

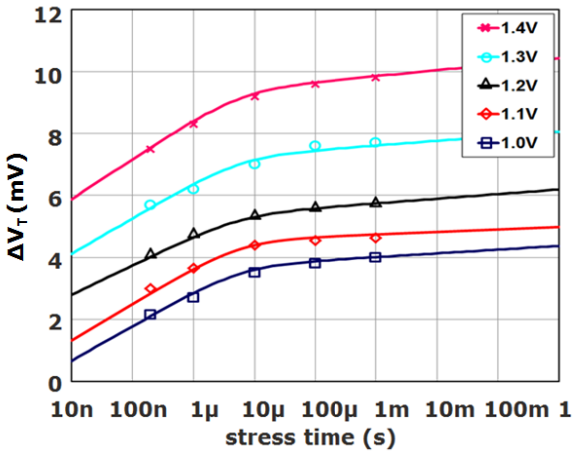

Fig. 5 –ΔV_{th} taken from the recovery traces (comp. Fig.4) after a recovery time of 1µs after different stress times (all data from same sample, same sample as in as Fig.4); Note that the ΔV_{th}-resolution is better than 0.05mV in these data.

To overcome these disadvantages of the fast ramp technique we employed our fast **M**easure-**S**tress-**M**easure technique [8] which has been improved to meet the requirements given in section II. Using a fast analog feedback loop the value of V_{th} – which is the gate voltage corresponding to a fixed (selectable) drain current and voltage – can be read out directly. The applied stress pulses are rectangular and their width can be varied from 200ns to infinity. Shorter stress pulses are not applicable due to a finite length of the test leads (several cm) and the missing impedance matching of voltage source and device under test (on wafer). The timing of the measurement is schematically shown in Fig. 3. Figs. 4 and 5 give an example of the performance and resolution which can be achieved with this setup. As can be seen in Fig. 5, the resolution in ΔV_{th} is better than 0.02mV. This value of 0.02 mV, however, is not the resolution which can be achieved by a single, fast measurement of V_{th}. Due to noise in the drain current the resolution of single measurements for short measuring delays (or recovery time) in the µs-range is around 0.2 mV only. When the measuring delay is increased, the integration time per measured point is increased. Thus the noise is decreasing and the resolution is improved. The resolution in ΔV_{th} shown in Figs. 4 and 5 – compared to single fast measurements of V_{th} – has been increased by two measures:

1) ΔV_{th} after short stress pulses does completely recover after recovery times of typically 1 s (see Fig. 4). Thus a given trace can be measured over and over again and the result can be averaged. For the data in Fig. 4 typically averages over 100 traces have been used, which only takes a few minutes. This averaging decreases the statistical current fluctuations by a factor $\sqrt{100}$ and thus improves resolution in ΔV_{th} by a factor of 10.
2) Since ΔV_{th} vs. log(recovery time) is a smooth function (see Fig. 4) the single data points of a recovery trace can be replaced by a spline or a polynomial (or similar) bringing about an additional reduction of fluctuations by typically a factor of 2.

IV. TIME, FIELD and TEMPERATURE DEPENDENCE of SHORT TERM ΔV_{th}

In this section the determination of the short term threshold shift has been chosen to be done for stress times of 1µs and after a recovery time of 1µs. The real relevant worst case stress and recovery times are a matter of the application and might be different from these values.

a) Dependence on stress time:

For both PBTI and NBTI and *standard stress conditions*, i.e. stress fields >=5MV/cm (SiO_2-equivalent) and stress times > 100s ΔV_{th} vs. stress time follows the normal behavior for NBTI for all technologies. That is a power law, t^n , with n around 0.15 to 0.2 in most cases. For low stress voltages (around nominal V_{dd}) and short stress times a special short term behavior can be observed for Hi-K metal gate technologies compared to SiON technologies. Examples for a saturating behavior can be seen in Figs.5 and 7. This saturating behavior is a hint that a special species of defect with a distinct and short capture time exists in these samples in addition to the widely distributed time constants characteristic for NBTI and PBTI. Other samples, especially from early generations of Hf-based gate stacks show trapping and recovery of both positive and negative charges at the same time.

b) Field dependence:

A typical stress voltage dependence of a Hi-K metal gate pMOSFET is shown in Fig. 6. Actually the field dependence for the short term ΔV_{th} is very similar to the field dependence observed for NBTI [9] which goes roughly with F^3. Thus the field dependence is rather severe: Increasing the field by 25% doubles the effect.

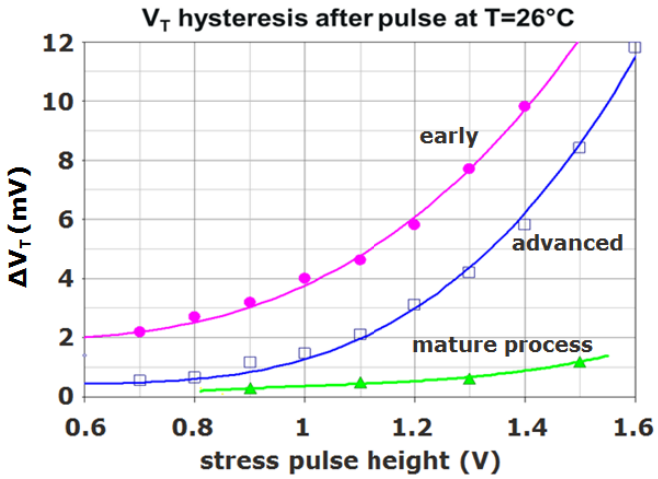

Fig. 6 – Stress voltage dependence of threshold hysteresis for 3 different Hi-K metal gate technologies. Data taken at 25°C after a 1µs stress pulse width.

b) Temperature dependence:

The example in Fig. 7 shows that there is no pronounced temperature dependence of the short term threshold hysteresis. In many cases the measured ΔV_{th} is even less at high temperature than at low temperature for stress times below ms. It cannot be concluded, however, that the effect is not temperature dependent. If capture and emission of carriers is thermally activated with an activation energy in the order of 1eV (as found in [10]) then degradation at 125°C would be sped up by a factor 10,000 compared to 25°C. But it has been pointed out in [11] that this acceleration cannot be seen experimentally if the capture and emission time constants are evenly and widely distributed. Somewhat simplified, if degradation (=capture) is accelerated by a factor of 10,000 but recovery is sped up by a similar factor then the net effect of thermal activation vanishes.

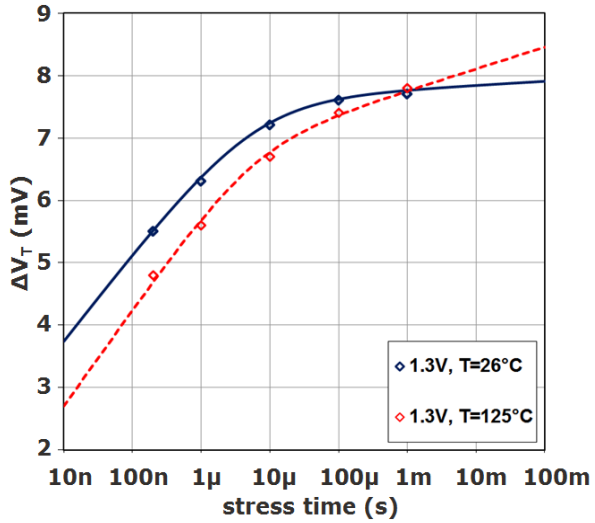

Fig. 7 – Threshold hysteresis as a function of stress pulse width for high and low temperature

V. SUMMARY for different TECHNOLOGIES

Fig. 8 shows a comparison of the threshold hysteresis for a couple of different technologies. It should be mentioned that all results in this study were from production quality samples, except denoted otherwise.

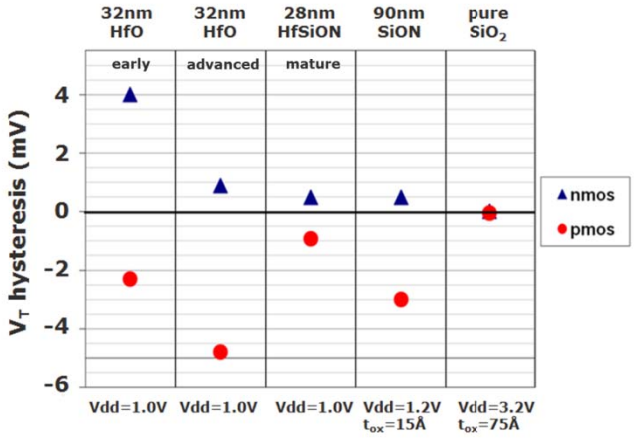

Fig. 8 – ΔV_{th}'s compared for different technologies. ΔV_{th}'s are measured after a stress pulse of 1µs and a recovery time of 1µs for worst case temperature (25°C for Hi-K and 125°C for SiON and SiO2).

In Fig. 8 three high-k metal gate technologies with E_{OT}'s around 12• are compared, where the 28nm HfSiON is the most advanced one. The pMOSFET of the 28nm HfSiON technology has actually even better properties than the one from conventional 90nm technology with the nitrided gate oxide. The ΔV_{th}'s for the non-nitrided technology are very close to zero. They could not be measured directly at V_{dd} but were measured at higher stress voltages and extrapolated down to V_{dd}. The values for ΔV_{th} were 0.04mV and <0.02mV for pMOS and nMOS, respectively.

The physical origin(s) for the ΔV_{th}'s generated by P/NBTI are still under debate. Our results suggest that for the nitrided and non-nitrided oxides the short term threshold shift is just from the normal N/PBTI effect, which we think has its origin in pre-existing oxide defects. The capture and emission time constants of these defects have a wide and nearly uniform distribution on a log scale. The situation is more complicated for the Hi-K material which appears to have additional defects with short and distinct time constants, probably due to the additional interfaces within the insulator.

Finally we want to mention that we also characterized the threshold hysteresis in samples which have been degraded (by N/PBTI) to levels corresponding to the standard fail criterion. Only an insignificant increase of the short term ΔV_{th}'s by about 10 to 20% has been observed.

VI. CONCLUSIONS

(1) It has been pointed out that very small and transient threshold instabilities on the order of 1mV can lead to failures in analog circuits, for example comparators and analog-to-digital converters. This issue has not received sufficient attention in the past. We also have shown that ΔV_{th}'s in the 1mV regime can be generated by short stress pulse in the µs-regime at nominal V_{dd}.

(2) An estimation of the impact of these threshold instabilities requires non-standard, very sensitive measurement techniques and special assessments and considerations. Standard N(P)BTI assessment cannot give the required information, since a "down-extrapolation" from long stress times to short term hysteresis is not reliable.

(3) We have compared technologies from non-nitrided, to nitrided oxides, to different generations of Hi-K metal gate stacks. Our results strongly suggest that due to the complex gate stacks with more than one interface and the advanced processes the short time threshold hysteresis of Hi-K MG technologies should receive special attention. However, contrary to early studies which showed a significant 'fast charging' component, the latest generation HiK MG appear perfectly able to meet the requirements.

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