

On the Correlation Between NBTI, SILC, and Flicker Noise

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Abstract—Negative Bias Temperature Instability (NBTI) is suspected to be linked to various other MOSFET phenomena. We report measurements of increased drain current noise, increased gate leakage current, and decreased recoverable threshold voltage shift after multiple cycles of negative bias temperature stress and relaxation for three different technologies. We also find that stress conditions have to be carefully selected, otherwise oxide breakdown will be erroneously interpreted as a correlation between NBTI, noise and gate leakage. Finally, the implications of our findings on the modelling of oxide defects are highlighted.

in I_G was only observed after catastrophic oxide breakdown events, which might lead to wrong conclusions. We perform a detailed study on three different technologies to explore the potential correlation between these phenomena *prior* to oxide breakdown and highlight some potential pitfalls.

The relevance of thorough study of the effects described above is twofold: First, if there is a correlation between NBTI degradation, noise, and SILC, a sound physical defect model must be able to predict all these effects. In addition, if long term NBTI stress had an impact on device noise, this would once more challenge the assertion that NBTI is governed by the reaction-diffusion model, with just a short initial transient from hole trapping. And second, chances are that in order to calibrate a defect model, only data from one type of measurement is required, possibly enabling to *predict* the device's performance in the other areas.

I. INTRODUCTION

Recently, a number of groups have investigated the significant contribution of oxide defects to the negative bias temperature instability (NBTI) [1–5]. The assumption that an ensemble of defects with widely distributed timescales exists across the oxide can successfully explain a wide variety of experimental observations. The fact that the same assumption has been employed to explain flicker noise in MOSFETs for over 50 years [6–8] has stimulated research about a possible common root of both phenomena [9]. In thin oxide transistors, an additional observable presents itself in the form of the gate current, where defects can conduct a trap-assisted current through the oxide [10, 11], creating a stress-induced leakage current (SILC). In this picture, the charge state of an oxide trap is thought of as a ‘gate’ for an oxide current path with the trap acting as a support for trap-assisted tunneling (TAT), whereas upon capturing a carrier from the channel due to NBTI degradation, the current path is blocked.

It has recently been observed that the recoverable component of NBTI, R , reduces with increasing stress time [12, 13], possibly by some form of defect transformation. Following the observation that a strong decrease in R correlated with a strong increase in I_G and noise, it has been suggested [12] that the defects responsible for R can transform into those responsible for SILC and flicker noise. This observation provides a strong clue towards the missing link between these phenomena. However, in this previous study, the increase

II. EXPERIMENTAL

Devices of three different technologies were used in the experiments: Technology 1 is a 0.35 μm CMOS process with 3 nm SiO₂ oxide, where pMOSFETs with $W/L = 10 \mu\text{m}/10 \mu\text{m}$ were used. Technology 2 is a 0.14 μm CMOS process with 2.9 nm SiON oxide, where devices with $W/L = 8 \mu\text{m}/8 \mu\text{m}$ were used. Technology 3 is a 90 nm CMOS process with a 2.2 nm SiON oxide with $\approx 6\%$ nitrogen content, where devices with $W/L = 10 \mu\text{m}/10 \mu\text{m}$ were used. All experiments were carried out at $T = 200^\circ\text{C}$.

Two experiments were carried out for each stress condition on two devices each, for each wafer: Experiment one obtains an initial drain current noise spectrum S_{I_D} at a suitable gate voltage V_m (where $V_m = -0.5\text{V}$, -1.0V , and -0.6V for technologies 1, 2, and 3, respectively), and an initial $I_G(V_G)$ characteristic. After that, the device is stressed at V_s for $t_s = 1\text{ks}$, relaxed at 0V for $t_r = 1\text{ks}$, and S_{I_D} and $I_G(V_G)$ are recorded again. The drain voltage $V_D = -100\text{mV}$ for the noise measurement, and $V_D = 0\text{V}$ otherwise. The noise spectra are least-squares fitted with $S_{I_D} = S_0/(f/1\text{Hz})^a$ via S_0 and a . The

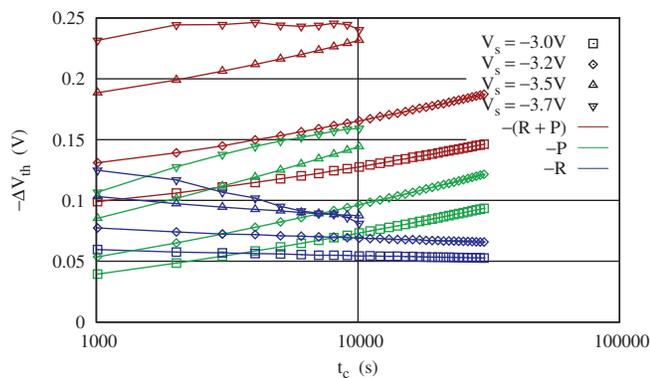


Fig. 1. Permanent component and relaxing component of $\Delta V_{th} = P + R$ for technology 1 and different biases. At $V_s = -3.7$ V TDDB starts, at $V_s = -4.0$ V the oxide is severely damaged (not shown).

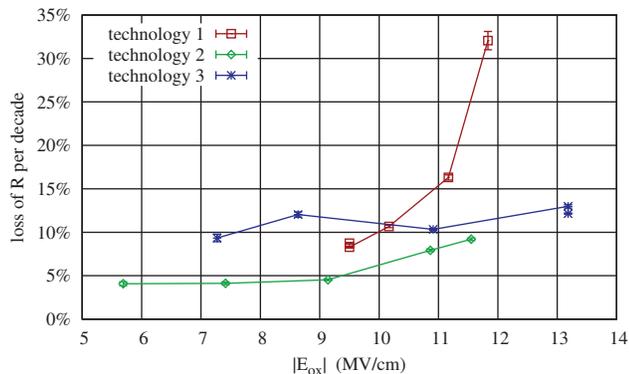


Fig. 2. Loss of R at $T = 200^\circ$ C for all three technologies.

gate currents are sampled at $V_G = -2$ V. This experiment is repeated continuously, and data is presented as function of the cumulative stress time $t_c = nt_s$. In the course of the noise measurements the mean drain current is also recorded, and will be denoted as I_D^n . The frequency exponents a observed were in the range $[1.0, 1.5]$.

In experiment two, we record an $I_D(V_G)$, then stress the device for t_s at V_s , then measure the drain current for $t_m = 1$ s at $V_G = V_m$, relax the device for t_r at 0 V, and measure again at V_m for t_m . During stress and measurement $V_D = -100$ mV, whereas for the relaxation $V_D = 0$ V. The voltage V_m is chosen equal to the particular technology’s V_m used in experiment one. The ‘permanent’ component is arbitrarily defined as $P := \Delta V_{th}(t_r)$, the relaxing component as $R := \Delta V_{th}(t_d) - \Delta V_{th}(t_r)$, where t_d is the intrinsic measurement delay, $t_d \approx 2$ ms [12, 13]. Also this procedure is repeated continuously. Figure 1 shows the results exemplarily for technology 1. Furthermore, the expression $1 - b \log_{10}(t_c/t_s)$ is least-squares fit to the normalised relaxing component $R(t_c)/R(t_s)$. The parameter b directly represents the loss of R per decade of t_c . This loss is plotted for all three technologies in Figure 2.

III. RESULTS AND DISCUSSION

Technology 1 shows a correlation between the temporal evolution of drain current degradation, drain current noise

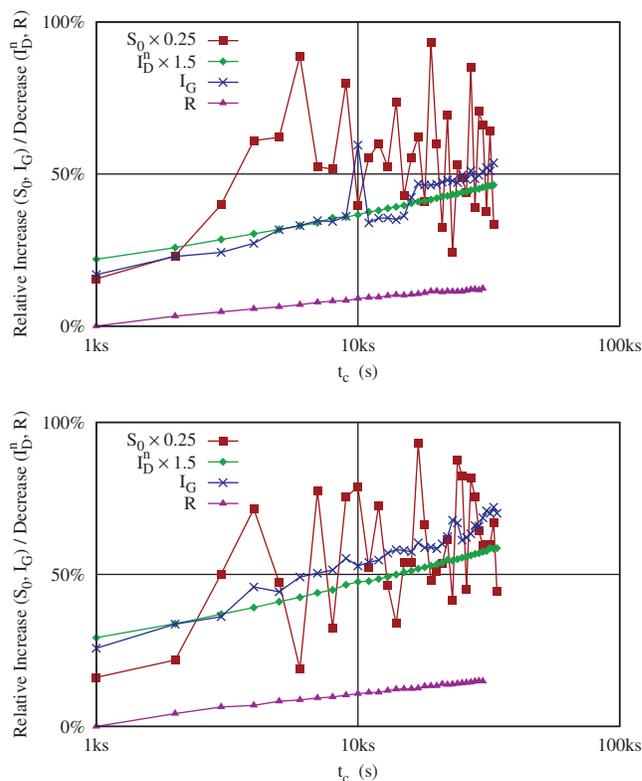


Fig. 3. Change of drain current, drain current noise, gate current, and recoverable component for technology 1 at $E_{ox} = 9.5$ MV/cm (top) and $E_{ox} = 10.2$ MV/cm (bottom). The individual traces are scaled to better show a possible correlation.

increase, gate current increase, and loss of recoverable component of ΔV_{th} for not too excessive stress voltages (Figure 3). In contrast, technology 2 shows less degradation in drain current, almost no increase in gate current and no increase in noise in Figure 4, although the oxide field in this device is comparable to technology 1. The loss of R for technology 2 is only smaller by a factor of 2 compared to technology 1. The increase in gate current of technology 3 is very small even at high oxide fields (Figure 5). Figure 8 shows the noise and gate leakage behaviour of technology 3. It must be noted that our equipment is not able to resolve the unstressed transistors’ noise of this technology, so the lack of increase in S_0 cannot be taken as an indication of non-increasing noise after stress. Nevertheless, both measurements show a sudden increase both in gate current and noise, which is remarkable. For a measurement with $V_s = -3.0$ V, no increase in I_G was seen during 43 ks stress, stresses above -3.5 V immediately broke the transistor.

At higher stresses the devices show time dependent dielectric breakdown (TDDB), which manifests itself as an abrupt increase of I_G over orders of magnitude, which is only sometimes accompanied by an increase in noise. Devices of technology 1 showed this behaviour for $E_{ox} = 11.2$ MV/cm (Figure 6), whereas at $E_{ox} = 11.8$ MV/cm the transistor completely breaks after 27 ks of stress. This shows also that measurements of drain current noise must be carefully checked against oxide breakdown. If the gate current is increased by

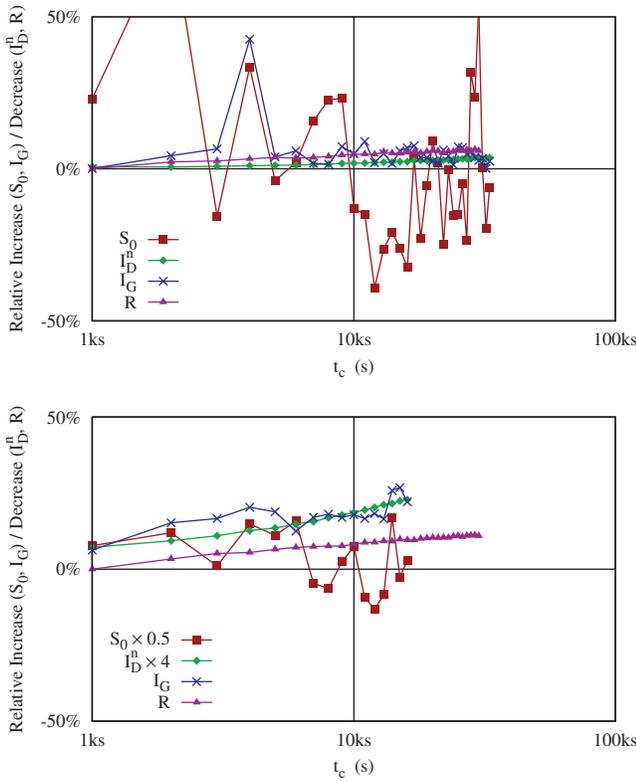


Fig. 4. Change of drain current, drain current noise, gate current, and recoverable component for technology 2 at $E_{ox} = 9.1\text{MV/cm}$ (top) and $E_{ox} = 10.9\text{MV/cm}$ (bottom). The individual traces are scaled to better show a possible correlation.

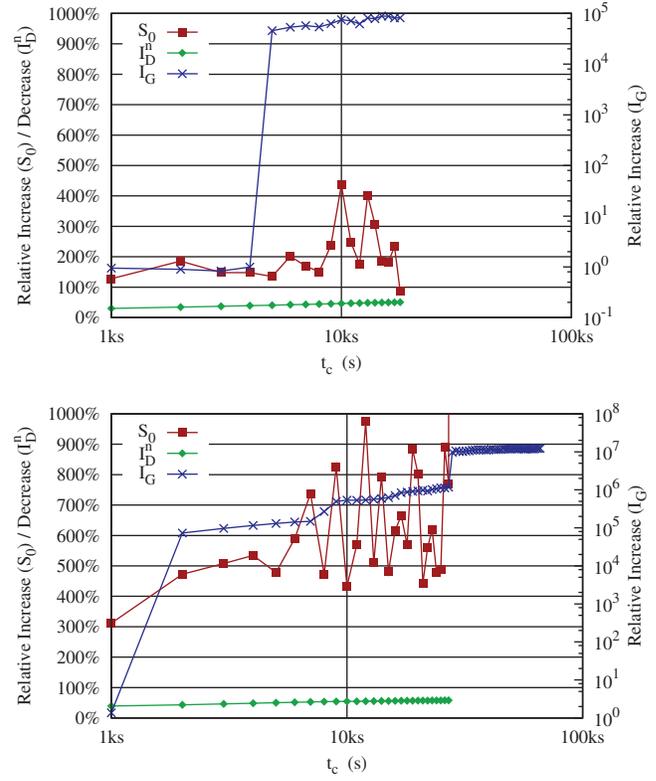


Fig. 6. Change of drain current, drain current noise, and gate current for technology 1, $E_{ox} = 11.2\text{MV/cm}$ (top) and $E_{ox} = 11.8\text{MV/cm}$ (bottom).

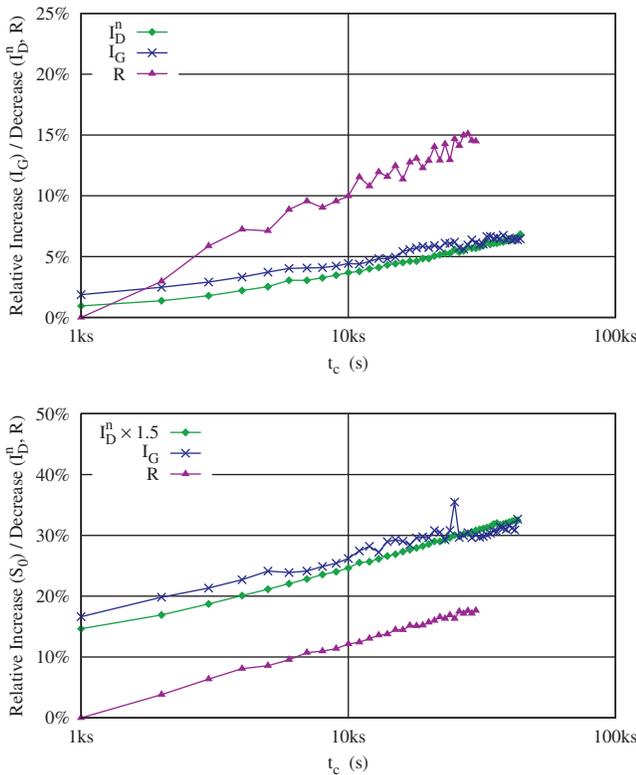


Fig. 5. Change of drain current, gate current, and recoverable component for technology 3 at $E_{ox} = 11.0\text{MV/cm}$ (top) and $E_{ox} = 13.0\text{MV/cm}$ (bottom).

orders of magnitude from its initial value, as seems to be the case in [12], it may readily add to the drain current noise. For technology 2, Figure 7 shows comparable increases in gate current, while in one case the noise only slightly increases, whereas in the second case a comparable large increase in noise is observed.

In contrast to [12], we find different behaviour (increasing vs. constant) noise after NBTI for different technologies, although all technologies show a loss in R at $T = 200^\circ\text{C}$. We also find large increases in noise and I_G at some conditions, but attribute them to the beginning destruction of the oxide.

We also remark that a decrease in the recoverable component R and an increase in the drain current noise are not reconcilable in a two-state defect model: If the reduction in R is explained by defects transforming into a ‘more permanent form’, i.e. their emission times grow larger than t_r , these defects cannot possibly contribute anymore to a noise spectrum with a minimum frequency larger than $1/t_r$. The increase of SILC while R is decreasing would necessitate a defect that in its initial configuration has a short or moderate emission time, but does not contribute to the gate current. Upon transformation, the charge in the defect becomes locked in, but on the other hand, the defect would act as a center for SILC/TAT, which seems to be contradictory. Therefore, we strongly believe that if the same defects are responsible for NBTI degradation, noise, and SILC, these defects have to be modelled by a multi-state model, like [14].

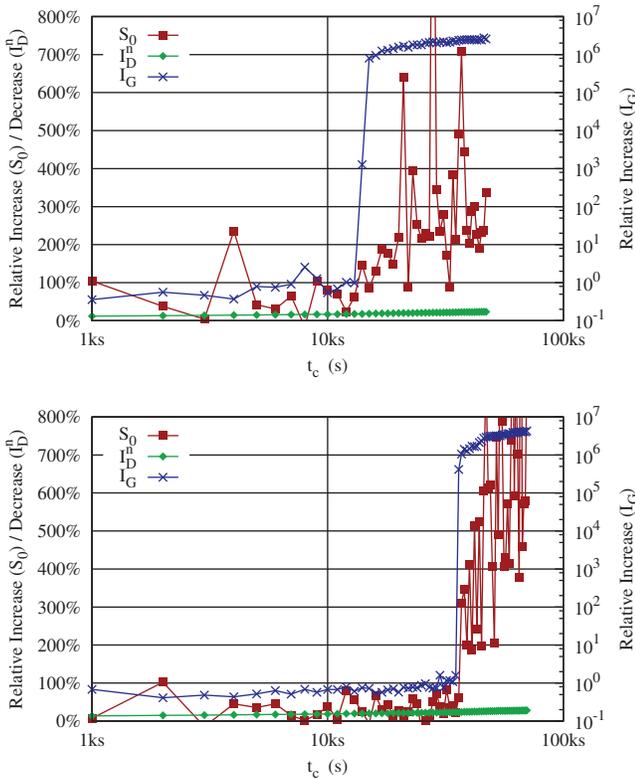


Fig. 7. Change of drain current, drain current noise, and gate current for technology 2, $E_{ox} = 11.6\text{MV/cm}$ (top) and $E_{ox} = 11.9\text{MV/cm}$ (bottom).

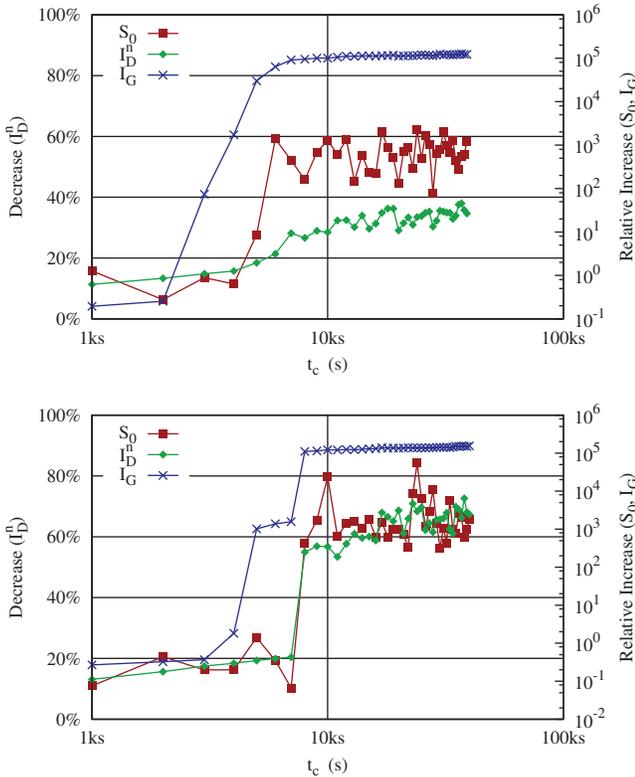


Fig. 8. Change of drain current, drain current noise, and gate current for technology 3, $E_{ox} = 13.6\text{MV/cm}$ (top) and $E_{ox} = 14.1\text{MV/cm}$ (bottom).

IV. CONCLUSION

We showed that NBTI stress at high temperatures increases SILC, and in some technologies also drain current noise. Contrary to other groups we do not always find a correlation between noise and SILC increase on one hand and the reduction in NBTI recoverable component on the other hand. We stress that care has to be taken not to enter the TDDDB regime when assessing noise or SILC after NBTI, and we believe that some reports of strong increases in SILC or noise are actually caused by beginning oxide breakdown. Lastly, we argue that a simple two-state defect model can not consistently explain our experimental findings.

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