Materials Science Forum Vols. 740-742 (2013) pp 757-760 Online available since 2013/Jan/25 at www.scientific.net © (2013) Trans Tech Publications, Switzerland doi:10.4028/www.scientific.net/MSF.740-742.757

# Efficient Characterization of Threshold Voltage Instabilities in SiC nMOSFETs Using the Concept of Capture-Emission-Time Maps

Gregor Pobegen<sup>1,a</sup>, and Tibor Grasser<sup>2,b</sup>

<sup>1</sup>KAI GmbH, Europastrasse 8, A-9500 Villach, Austria

<sup>2</sup>Institute for Microelectronics, TU Vienna, Gusshausstrasse 27-29, A-1040 Vienna, Austria <sup>a</sup>gregor.pobegen@k-ai.at, <sup>b</sup>grasser@iue.tuwien.ac.at

**Keywords:** SiC-MOSFET, Vth-instabilities, drain-current-instability, reliability, defects, traps, capture/emission time constants

**Abstract.** We utilize the recently suggested capture-emission-time (CET) maps [1] for the first time for SiC technologies. CET maps are a very powerful characterization technique which allow the elegant and comprehensive analysis of oxide/interface traps at or near the semiconductor-dielectric interface and were originally developed to characterize degradation of Si based MOSFETs. For asprocessed SiC MOSFETs [2] we present first results of the SiC-SiO<sub>2</sub> interface using CET maps. We suggest that oxide traps are mainly responsible for the instability in SiC MOSFETs. Furthermore we state that the large time constants and the temperature activation of the traps in SiC MOSFETs can be consistently explained when accounting for multi-phonon processes for the microscopic charge exchange. A recently suggested model including such microscopic transitions [3] is applied to SiC MOSFETs and shown to reproduce our experimental data with high accuracy for a large temperature range.

## Introduction

The instability of the threshold voltage of SiC MOSFETs is conventionally attributed to the trapping of channel electrons (for n-channel devices) into interface and/or oxide traps [4] and modeled using standard Shockley-Read-Hall (SRH) theory [5]. Within standard SRH theory [6, 7] negative charge build-up can only be due to either electron capture, which happens quasi-instantaneously with a bias switch ( $\tau_{\rm cn} \propto \exp((E_{\rm C}-E_{\rm F})/kT)$ ), or through hole emission, which is independent of the position of the Fermi level ( $\tau_{\rm ep} \propto \exp((E_{\rm T}-E_{\rm V})/kT)$ ). However, experimentally, a simple turn-on of a SiC nMOSFET as depicted in Fig. 1a leads to long-lasting negative charge build-up inconsistent with either hole emission or electron capture of the standard SRH theory. Also an adapted version of the SRH model for oxide charges [8, eq. (76)], is shown in Fig. 1b to be fairly at odds with the experimental data. Consequently we must conclude that SRH-like models are not capable to describe the charging behavior of SiC MOSFETs and we have to find an alternative description to understand the instability. Before discussing a possible physical origin, we look at the problem in a systematic way using CET maps.

## **CET** map occupancy

A CET map is a two-dimensional plot of the density of traps versus their corresponding logarithmic capture and emission times [1]. Integration of certain areas of the CET map gives the number of trapped charges and thus the  $\Delta V_{\rm TH}$  at any instant of time. The integration area is defined through the duration of charging/discharging periods due to bias switches at the gate. The simplest case for charging traps in a SiC MOSFET is to switch the gate bias from 0V to the  $V_{\rm TH}$  of the device (filling of the CET map from bottom to top). This typically results in a semilogarithmic charging behavior [9], which is due to a superposition of a large number of individual charging events with a very broad distribution of capture time constants  $\tau_{\rm c}$  [1]. The energetic position of the traps responsible for the

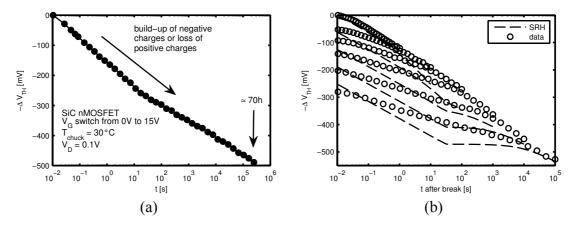


Fig. 1: (a) A simple turn-on of a SiC nMOSFET leads to a long lasting continuous charging transient. Approximately  $10^{11} \text{cm}^{-2}$  defects are charged at constant bias during approximately two days  $\approx 2 \times 10^5 \text{s}$ . This behavior cannot be explained with SRH theory which excludes interface traps as the cause for the instability. (b) An adapted version of the SRH model for oxide charges [8, eq. (76)], which basically maps a distribution of vertical defect positions into a logarithmic distribution of time constants, suggests a strong correlation between the emission and the capture time constant of a single oxide trap. These correlations would especially be visible when interrupting the charging of the device as depicted in (b), where five interruptions at 0V with 1s duration were performed. The correlations of the emission and capture time constants leads to a characteristic charging behavior which is fairly at odds with the experimental result.

charging is between  $E_{\rm F}(V_{\rm G}=0{\rm V})$  and  $E_{\rm F}(V_{\rm G}=V_{\rm TH})$ . When the constant bias phase is interrupted, some of the defects emit their charge again, provided the interruption was longer than their emission time constants  $\tau_{\rm e}$ . This leads to rather complicated charging transients like those depicted in Fig. 2. But independently of the exact distribution of  $\tau_{\rm c}$  and  $\tau_{\rm e}$ , the transients of Fig. 2 can already be understood in terms of an occupation pattern in the CET map.

## **CET map model**

Further accuracy of our approach is achieved when not only the occupancy of the CET map is considered but also the underlying distribution of time constants. This distribution is not completely uniform (which would lead to a straight line in Fig. 1a) and it has to become zero for extremely short or long time constants. Given the extremely wide distributions of time constants, which is reminiscent of those observed in Si devices [10], complete characterization of all time constants is unfeasible. We therefore follow the approach suggested in [3] and validate an analytical Ansatz against experimental data.

For this we use a model which was successfully used to explain Si MOSFET degradation [3]. There, the time constants are modeled with two bivariate log-normal distributions with large mean and variance. The model is based on the observation that the time constants are temperature activated because of multi-phonon processes which lead to charge transfer to oxide traps. We therefore directly deal with effective activation energies  $E_{\rm A,c;e}=kT\log{(\tau_{\rm c;e}/\tau_0)}$ , with  $\tau_0$  a yet to be determined normalization constant. The normal distribution can be analytically integrated as described in [3, 11] for the given times and temperatures of the experimental data. The result is compared to the experimental data and a non-linear data fitting algorithm is used to adapt the parameters of the distributions such that the least square sum of the difference to the data is minimized. The result of such a fit for five different devices at five different temperatures between  $30^{\circ}C$  and  $200^{\circ}C$  is depicted in Fig. 3. When this CET map is integrated for a particular charging sequence, the experimental data is nicely reproduced, as depicted in Fig. 1b.

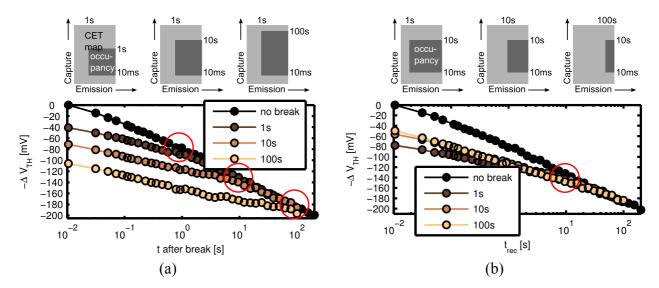


Fig. 2: (a) The time before a 1s interruption during charging significantly alters the charging characteristic. The occupancy states for the first measurement point after the break give an intuitive explanation for the experimentally observed charging behavior. The transients merge when the total charging time becomes larger than the charging time before the break (circles). (b) Increasing the duration of the 0V break enables more traps to emit their charges and brings the transient closer to the no break line. All transients merge at the point when the second charging period exceeds the charging period before the break.

#### Conclusion

We suggest a powerful approach for the understanding of the defect dynamics which lead to the instability of SiC MOS devices. Our approach allows for the calculation of arbitrary sequences of on/off phases through an analytical integration of a CET map [1]. This is especially beneficial for circuit designers to predict the device behavior during its operation.

Our work further reveals that the charging of interface traps described with standard SRH theory is at odds with experimental data. One option would be that oxide traps are responsible for the  $V_{\rm TH}$  instability. The long time constants of the traps are due to microscopic charging processes which involve several individual phonons. Modeling the  $V_{\rm TH}$  instability of a SiC nMOSFET taking this into consideration leads to a good agreement between the model and the experimental data.

#### Acknowledgment

This work was jointly funded by the Austrian Research Promotion Agency (FFG, Project No. 831163) and the Carinthian Economic Promotion Fund (KWF, contract KWF-1521|22741|34186). The authors would like to thank Dethard Peters and Thomas Aichinger (both Infineon Technologies Austria) for their kind guidance and support.

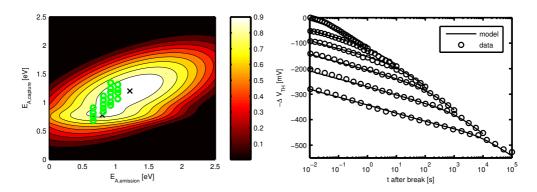


Fig. 3: Resulting activation energy CET map after [3] fitted to several different charging transients of five different devices at temperatures between  $30^{\circ}C$  and  $200^{\circ}C$ . The green points indicate the position of the experimental data. The exact extensions of the distributions at some distance from the experimental data is a consequence of the extrapolation of the underlying model. The map is plotted with a logarithmic normalization operator as defined in [3] to resolve all details of the map.

#### References

- [1] H. Reisinger, T. Grasser, W. Gustin, and C. Schluender, "The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress," in *IEEE International Reliability Physics Symposium*, 2010, p. 7.
- [2] A. Lelis, D. Habersat, R. Green, A. Ogunniyi, M. Gurfinkel, J. Suehle, and N. Goldsman, "Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1835–1840, Aug. 2008.
- [3] T. Grasser, P. Wagner, H. Reisinger, T. Aichinger, G. Pobegen, M. Nelhiebel, and B. Kaczer, "Analytic modeling of the bias temperature instability using capture/emission time maps," in *IEEE International Electron Devices Meeting*, Dec. 2011, pp. 27.4.1–27.4.4.
- [4] M. Gurfinkel, H. Xiong, K. Cheung, J. Suehle, J. Bernstein, Y. Shapira, A. Lelis, D. Habersat, and N. Goldsman, "Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I-V Techniques," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 2004–2012, Aug. 2008.
- [5] S. Potbhare, N. Goldsman, G. Pennington, A. J. Lelis, and J. McGarrity, "Time Dependent Trapping and Generation-Recombination of Interface Charges: Modeling and Characterization for 4H-SiC MOSFETs," *Materials Science Forum*, vol. 556-557, pp. 847–850, 2007.
- [6] W. Shockley and W. T. Read, "Statistics of the Recombinations of Holes and Electrons," *Physical Review*, vol. 87, no. 5, pp. 835–842, Sep. 1952.
- [7] R. N. Hall, "Electron-Hole Recombination in Germanium," *Physical Review*, vol. 87, no. 2, pp. 387–387, Jun. 1952.
- [8] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microelectronics Reliability*, vol. 52, no. 1, pp. 39–70, 2012.
- [9] T. Okayama, S. Arthur, J. Garrett, and M. Rao, ``Bias-stress induced threshold voltage and drain current instability in 4HSiC DMOSFETs," *Solid-State Electronics*, vol. 52, no. 1, pp. 164–170, 2008.
- [10] G. Pobegen, T. Aichinger, M. Nelhiebel, and T. Grasser, "Understanding Temperature Acceleration for NBTI," in *International Electron Device Meeting Technical Digest*, Washington, DC, Dec. 2011, pp. 27.3.1–27.3.4.
- [11] W.-J. Tsay and P.-H. Ke, ``A Simple Approximation for Bivariate Normal Integral Based on Error Function and its Application on Probit Model with Binary Endogenous Regressor," *IEAS Working Paper*, vol. 09, A011, 2009.

# **Silicon Carbide and Related Materials 2012**

10.4028/www.scientific.net/MSF.740-742

Efficient Characterization of Threshold Voltage Instabilities in SiC nMOSFETs Using the Concept of Capture-Emission-Time Maps

10.4028/www.scientific.net/MSF.740-742.757