Schottky-Barrier Normally Off GaN/InAlN/AlN/GaN HEMT With Selectively Etched Access Region

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***Abstract*—A Schottky-barrier normally off InAlN-based high-electron-mobility transistor (HEMT) with selectively etched access regions, high OFF-state breakdown, and low gate leakage is presented. Metal–organic chemical vapor deposition-grown 1-nm InAlN/1-nm AlN barrier stack is capped with a 2-nm-thick undoped GaN creating a negative polarization charge at a GaN/InAlN heterojunction. Consequently, the gate effective barrier height is increased, and the gate leakage as well as the equilibrium carrier concentration in the channel is decreased. After removal of the GaN cap at access regions by using a highly selective dry process, the extrinsic channel becomes populated by carriers. Normally off HEMTs with 8-μm source-to-drain distance and 1.8-μm-long symmetrically placed gate showed a source drain current of about 140 mA/mm. The HEMT gate leakage at a drain voltage of 200 V and grounded gate is below 10^{-7} A/mm with a three-terminal device breakdown of 255 V. The passivated InAlN surface potential has been calculated to be 1.45 V; significant drain current increase is predicted for even lower potential.**

***Index Terms*—Breakdown, GaN HEMTs, InAlN, normally off, polarization engineering.**

THERE is an interest in developing normally off GaN-based high-electron-mobility transistors (HEMTs) for RF [1] and logic [2] applications. Recessed gate technology was used for normally off InAlN/GaN-based HEMTs [3]–[5]. Selective plasma etching with a low damage was suggested to recess the gate until a 2-nm-thin barrier layer remains. However, at a higher drain voltage $V_{\rm DS}$, such a short gate-to-channel distance deteriorates the Schottky-barrier (SB) gate leakage current I_G, and the device OFF-state breakdown $V_{\rm BR}$ appears already at 20–30 V [3], [4]. Gate insulation in metal–oxide–semiconductor (MOS) HEMTs has been demonstrated to improve $V_{\rm BR}$ significantly [5].

In this letter, we report on proof of concept of the normally off HEMT with the 2-nm-thick InAlN/AlN barrier and a 2-nm undoped GaN cap layer. Negative polarization charge at the GaN/InAlN junction depletes the channel below the gate and reduces the gate leakage similar to that demonstrated earlier for AlGaN/GaN [6]. On the other hand, after removing the GaN cap at access regions, electrons populate the channel. See Fig. 1(a) with calculated energy and concentration depth profiles in access regions. Consequently, high $V_{\rm BR}$ and low I_G are achieved without the additional gate insulation. The concept is verified also by using a 2-D numerical device simulator Minimos-NT [8].

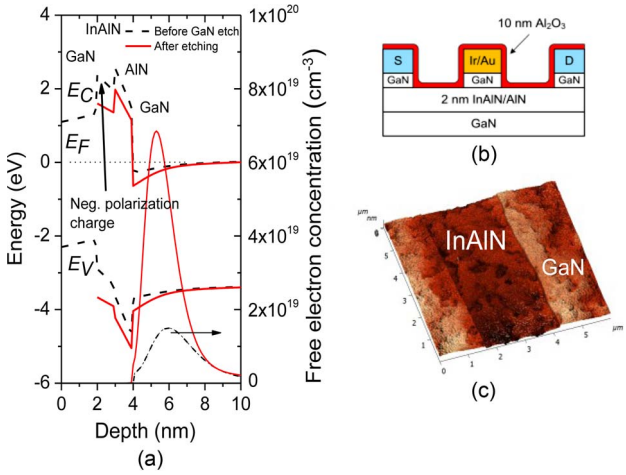

Fig. 1. (a) Calculated energy band and electron concentration profiles at (GaN)/InAlN/AlN/GaN HEMT access regions before and after etching the GaN cap in equilibrium. We assume surface potential $\phi_S = 1.1$ V for GaN and $\phi_S = 1.6$ V for the unpassivated InAlN; see 2-D simulation discussed later in the text. Corresponding polarization charges are $P_{\rm GaN/InAlN} = -4.5 \times 10^{-2}$ C/m^2, $P_{\rm InAlN/AlN} = -5 \times 10^{-2}$ C/m^2, and $P_{\rm AlN/GaN} = 9.5 \times 10^{-2}$ C/m^2[7]. (b) Sketch of the completed HEMT. (c) AFM image of etch test structure showing a 2.5-μm-wide etched window in the GaN cap.

The GaN (2 nm)/$In_{0.17}Al_{0.83}N$ (1 nm)/AlN (1 nm)/GaN (2 μm) HEMTs were grown on a sapphire substrate using a metal–organic chemical vapor deposition (MOCVD) [9]. Ti/Al/Ni/Au ohmic metallization and Ir/Au gate contacts were used. GaN cap at access regions has been removed by using a highly selective CCl_2F_2-based reactive-ion etching in an electron-cyclotron-resonance system with a microwave source turned off. Ohmic and gate contacts served as a mask. The parameters of etching were dc bias of 50 V, RF power of 85 W, gas pressure of 8 Pa, and etching time of 90 s. The surface roughness of the GaN cap is 1.8 nm, and after the GaN removal, the roughness of InAlN surface is 0.9 nm. Selectivity of the GaN etching process (better than 50:1 over InAlN) is due to low-volatile AlF_3 and InF_3 products formed on the barrier

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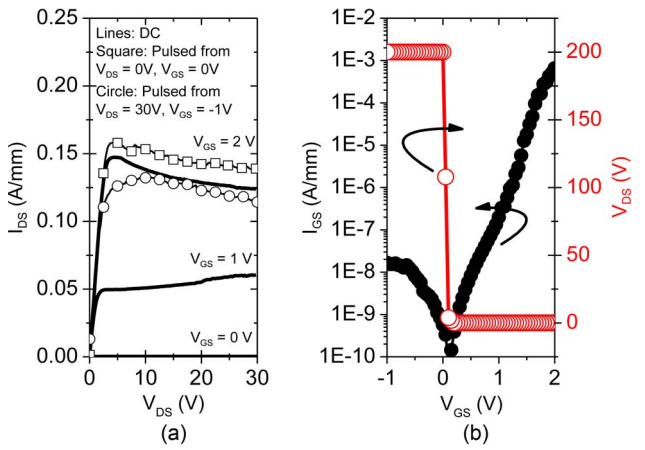

Fig. 2. (a) GaN/InAlN/AlN/GaN HEMT dc and pulsed output characteristics after etching the GaN cap, passivating the InAlN surface, and annealing. In the 1-μs pulsed operation, the quiescent points are (0 V, 0 V) and ($V_{\rm GS} = -1$ V, $V_{\rm DS} = 30$ V), and duty cycle is 0.01. (b) Three-terminal OFF-state breakdown characteristic determined by a drain injection technique at injection current $I_{\rm DS} = 1$ μA/mm. $I_{\rm GS}$ changes the polarity at $V_{\rm GS} \sim 0.1$ V; logarithm of $I_{\rm GS}$ is taken from the absolute values.

surface, while low dc bias is important to minimize plasma-induced damage [10]. Ten-nanometer Al_2O_3 passivation layer was deposited by MOCVD and annealed at 700 °C for 15 min afterward. Symmetrical HEMTs with a source–drain spacing and the gate lengths of 8 and 1.8 μm, respectively, were prepared.

A transfer-length method test indicated that the channel sheet resistance $(R_{\rm CH})$ drops from ~ 15 to ~ 2.5 kΩ/sq after removal of the GaN cap and to ~ 1.5 kΩ/sq after the passivation/annealing; the contact resistance (R_C) was 2.5 $\Omega \cdot$ mm. The source–drain current $I_{\rm DS}$ after the passivation/annealing is typically about 140 mA/mm at $V_{\rm GS} = 2$ V [see Fig. 2(a)], while the threshold voltage V_T determined from the transfer characteristics (see Fig. 4 hereinafter) is between 0.1 and 0.5 V. DC characteristics are also compared with the pulsed ones; devices indicate some level of the trapping, most probably also because of the close surface-to-channel distance. The observed V_T coincides well with V_T reported earlier for the recessed gate HEMTs having 1-nm InAlN/1-nm AlN barrier without any cap [3]. Indeed, by taking into account the following charge symmetry and assuming

$$P_{\rm GaN/InAlN} = -\left(P_{\rm InAlN/AlN} + P_{\rm AlN/GaN}\right) \quad (1)$$

$$\Phi_{\rm SB(GaN)} \sim \Phi_{\rm SB(InAlN)} - \Delta E_{C(\rm InAlN/GaN)}/e \quad (2)$$

where $\Phi_{\rm SB}$ and ΔE_C are a corresponding SB height and a conduction band discontinuity, respectively, and by using a Poisson equation, it can be shown that V_T is invariant to the presence of the GaN cap as

$$\begin{aligned} V_T \sim{}& \Phi_{\rm SB(GaN)} \\ &- \Sigma\Delta E_C/e - \left[(d_{\rm GaN} + d_{\rm InAlN} + d_{\rm AlN})P_{\rm AlN/GaN}\right. \\ &\qquad + (d_{\rm GaN} + d_{\rm InAlN})P_{\rm InAlN/AlN} \\ &\qquad \left. + d_{\rm GaN}P_{\rm GaN/InAlN}\right]/\varepsilon \\ ={}& \Phi_{\rm SB(InAlN)} - \Sigma\Delta E_C/e \\ &- \left[(d_{\rm InAlN} + d_{\rm AlN})P_{\rm AlN/GaN} + d_{\rm InAlN}P_{\rm InAlN/AlN}\right]/\varepsilon \end{aligned} \quad (3)$$

where d is a corresponding layer thickness and ε is a dielectric constant. For a first approximation, ε is considered to be constant throughout the stack. From (3), it follows that the maximal V_T of (GaN)/InAlN/AlN/GaN SB HEMTs is limited by $\Phi_{\rm SB(InAlN)} - \Sigma\Delta E_C/e < 1$ V. To increase V_T further, one may use, e.g., an "asymmetrical" polarization concept similar to that described for InGaN/AlGaN/GaN normally off HEMTs with inserting the InGaN cap [11] or, in the case of MOS HEMTs, by manipulating charges (i.e., reduction of surface donors and/or introduction of a negative oxide charge) at the oxide/semiconductor interface [12]. However, as shown here, the usage of the In-free lattice-matched GaN cap enables highly selective etching of the cap, low leakage/high breakdown SB gates, and the high HEMT ON/OFF ratio without a compromise to the strain or defects in the cap, while higher V_T in MOS HEMTs, in some cases, is acquired only because of a high density of interface states (i.e., E_F pinning) [12]. There is some similarity between our concept and a piezo neutralization technique reported elsewhere [13]. However, in the later approach, the charge neutralization is necessary to provide uniform V_T of the recessed gate, while in our case, the gate is not recessed and the negative polarization charge at the cap/barrier junction and not the charge symmetry is a prerequisite condition for a desired HEMT functionality.

A drain injection technique [14] has been used for determination of $V_{\rm BR}$ at $I_{\rm DS} = 1$ μA/mm. Fig. 2(b) indicates $V_{\rm BR}$ above 200 V at $V_{\rm GS} = 0$ V, where we already reached a voltage limit of the Keithley 4200 SCS. $V_{\rm BR} > 200$ V is a record value for SB normally off InAlN/GaN HEMTs. Subthreshold $I_{\rm GS} < 1 \times 10^{-7}$ A/mm even at the maximal $V_{\rm DS}$ has been observed, and that may indicate that the breakdown event occurs in the device buffer and not at the gate. Thus, the GaN cap is effective in blocking the gate tunneling current by increasing the contact to channel distance, by increasing the effective barrier height, and/or by capping conductive defects at the InAlN surface [15].

Hard $V_{\rm BR}$ at $V_{\rm GS} = 0$ V is documented in Fig. 3 where $I_{\rm DS} = 1$ μA/mm is reached at 255 V. $I_{\rm DS}$ and $I_{\rm GS}$ semilog transfer characteristics at $V_{\rm DS} = 10$ V, shown in the inset of Fig. 3, reveal $I_{\rm DS}$ below 10^{-6} A/mm at $V_{\rm GS} = 0$ V and *ON/OFF* ratio 10^5. For $V_{\rm GS} < -0.2$ V, we observe that $I_{\rm DS}$ and $I_{\rm GS}$ decrease down to 10^{-8} A/mm. The GaN cap below the gate lowers the equilibrium concentration of carriers, and that enhances the ON/OFF ratio. Nevertheless, AlGaN back barrier [16] may further improve OFF-state characteristics. Submicrometer gate-length technology needs to be applied in the future to access fully the leakage reduction; nevertheless, present $I_{\rm GS}$ is by far better than that of the uncapped InAlN/GaN HEMTs with a similar gate geometry [10]. Moreover, high thermal load during the processing (700°C for 15 min) indicates possible feasibility of the concept for normally off HEMTs operating at high-temperature conditions.

Surface potentials Φ_S were calculated by using the 2-D model [8]. By fitting to the transfer characteristics (see Fig. 4), we extracted Φ_S(GaN) = 1.1 V before the etching and Φ_S(InAlN) = 1.6 and 1.45 V before and after the passivation/annealing, respectively. We calculated $I_{\rm DS}$ at $V_{\rm GS} = 2$ V ($I_{\rm DSmax}$) as a function of Φ_S(InAlN); see the inset of

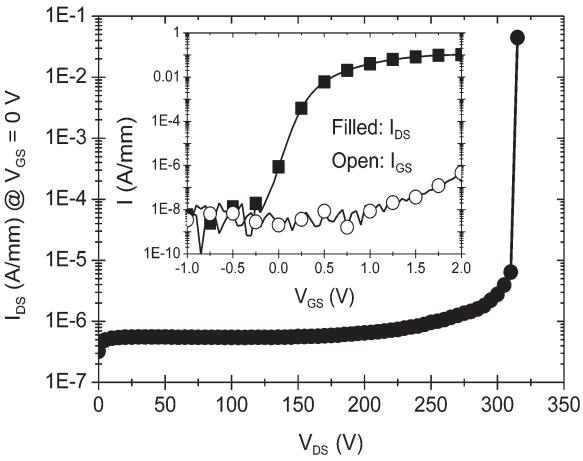

Fig. 3. Three-terminal OFF-state breakdown characteristic measured at $V_{\rm GS} = 0$ V with $V_{\rm DS}$ step of 5 V. Inset shows $I_{\rm DS}$ and $I_{\rm GS}$ semilog transfer characteristics at $V_{\rm DS} = 10$ V. The ON/OFF ratio at $V_{\rm GS} = 2$ V/0 V is 10^5. Gate-to-drain spacing is 3 μm.

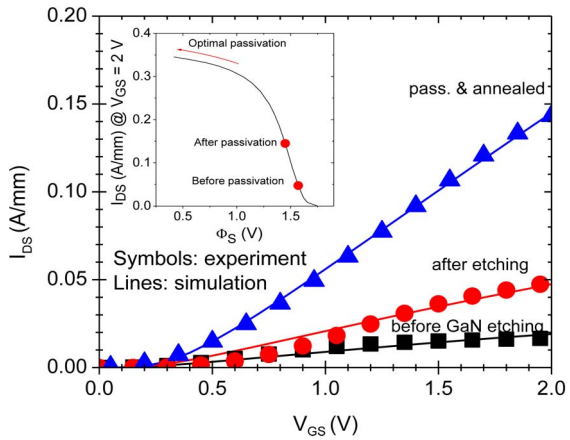

Fig. 4. Experimental and calculated transfer characteristics of the GaN/InAlN/AlN/GaN HEMT at various stages of the processing. Inset shows the calculated dependence of $I_{\rm DSmax}$ on Φ_S(InAlN). In the inset, points correspond to the experimental results, and the arrow indicates the range of the surface potential for the anticipated optimal passivation.

Fig. 4. Due to close vicinity of the surface to the QW channel, a fairly strong dependence of $I_{\rm DSmax}$ on Φ_S can be obtained for $\Phi_S > 1$ V. On the other hand, maximal $I_{\rm DS}$ saturates at $\sim$0.3 A/mm for Φ_S(InAlN) ≤ 1 V, and we may suggest that, to maximize $I_{\rm DS}$, the passivation should fulfill $\Phi_S \leq 1$ V. Moreover, for $\Phi_S = 0.4$ V and $R_C = 0.5\ \Omega \cdot$ mm, we calculated $I_{\rm DSmax} = 0.7$ A/mm (not shown).

In conclusion, normally off SB InAlN/GaN-based HEMTs with low leakage currents and high breakdown voltage have been developed without using the gate insulation. Instead, GaN cap layer under the gate proves to be efficient in lowering the gate leakage current while maintaining the positive V_T. By removing the GaN cap at access regions, InAlN surface passivation is found to be crucial for the device performance.

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