3D TECHNOLOGY INTERCONNECT RELIABILITY TCAD

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ABSTRACT
For the realization of modern three-dimensional (3D) integrated circuits new metallization components such as through-silicon-vias (TSVs) and solder bumps, together with complex multi-level 3D interconnect structures are applied. Due to new technologies and ongoing miniaturization, the impact of the microstructure, which defines material properties and residual stresses in a metallic interconnect structure, gains importance. A systematic reliability study of interconnects in 3D stacked chips is currently not available. The reliability assessment of specific components of 3D interconnects and whole chips demands development of new TCAD methods and their utilization in a combination with experimental reliability tests. In the scope of our work we develop models and a simulation tool applicable for the most important reliability issues of modern 3D interconnects. The application of new materials and material compounds makes a multi-level approach of modeling a necessity. Thus, our work also comprises the influence of the technology process conditions on metal microstructure and the residual stress in interconnects. For the reliability study of interconnect components continuum mechanics and electromigration models are used and simulations based on the finite element method are carried out. The information obtained from our reliability assessment is subsequently applied for design modifications and development of new interconnects components which exhibit a significantly lower failure risk.

Key words: 3D integration, interconnect, reliability, electromigration

INTRODUCTION
Three-dimensional (3D) integration is an emerging technology which can form highly integrated systems by vertically stacking and connecting various materials, technologies, and functional components. The potential benefits of 3D integration can vary depending on the utilized approach; they include multi-functionality, increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration, and reduced overall costs.

3D technologies can be divided into three categories based on their similarity to other technologies:

- 3D packaging technology
- 3D transistor build-up technology
- Wafer-level back end of line (BEOL) compatible 3D technology

Each of these technologies has its specific electromigration (EM) and stress related reliability issues. EM and stress induced degradation act closely together and, in most cases, it is impossible to separate their impact on materials building specific interconnect structures [1]. According to the International Technology Roadmap for Semiconductors, EM will become a limiting factor for high current density packages [2]. A characteristic of 3D integration is also an increased significance of heat transfer. On a silicon chip, the elements which generate heat are the transistor, the contact metallization, the multilayered Cu and Al interconnects, and the solder bumps. In a large system, e.g., a mainframe computer, the heat will be conducted away with an elaborate cooling system using water and liquid helium or liquid natrium in an air conditioned room. However, for consumer electronics, such as hand-held wireless devices, typically a thermal interface material (TIM) will be inter-posed between the back-side of the Si chip and a piece of metallic plate or the metallic case of the hand-held device in order to conduct heat away. For 3D integrated circuit structures heat reduction is a challenging issue. Heat generation can be elevated by a factor relating to the number of chips in stacking, yet heat dissipation becomes much more difficult. Applying TIM only partially solves the problem, because it allows the heat to dissipate only from the top piece in the stack. It is technologically difficult to add TIM to the intermediate chips in the stack. The temperature gradient in a 3D structure must cover a large distance in order to transport heat through all the chips in the entire stack. The effect of increased temperature on EM and stress induced degradation is manifold; on the one hand side it enhances the material transport by increasing diffusivity coefficients; on the other hand side, in most of the cases it activates dislocation movements producing complex plastic effects both in metals and semiconductors. It is clear that the problem relating to the thermal budget must be particularly addressed while dealing with electromigration and stress related issues.

RELIABILITY ISSUES IN 3D TECHNOLOGY

Today, most studies concentrate on packaging-based 3D integration enabled by wire bonding and flip-chip bonding. From the point of view of device design and reliability, EM in a flip chip solder bump is significantly different to that in Al or Cu interconnects [1], [2]. The way that electric current flows through a solder bump is not uniform. The origin of this non-uniform current distribution is due to a high to low current density transition at the contact window between the on-chip metal line and the solder bump. According to the International Technology Roadmap for Semiconductors, EM will become a limiting factor for high current density packages [3]. Flip-chip solder joints are recognized as an outstanding risk factor and, therefore, their reliability has been intensively studied in recent years [4]. These investigations include the failure mechanism for Pb-based and Pb-free solders with under-bump metallization (UBM). It was found that current crowding induces voiding on the cathode/chip size of the solder joints.

The mechanical stress effects which affect the stability of 3D ICs can be divided in the local ones which lead to delamination and cracking in the vicinity of TSVs and inside solder joints, and compound failures which are produced by superposition of stresses by different stress sources, such as cracking in silicon and warpage of TSV chips [5]. Both local and compound failures can affect the device performance [6] and, therefore, engineers need to be very well aware of the stress levels, even if those are below thresholds for mechanical failure. Also, the mechanical strength of TSV chips is an issue, when the thickness of the chip is very thin. The strength depends on the design of the array of TSVs and tends to decrease with increasing density and/or number of vias. When the mechanical strength is weak, the chip can fracture easily. The tensile stress on silicon causes reliability problems such as cracking and crack propagation. In addition, the stress can change the mobility of carriers. Tensile stress enhances the electron mobility, and the hole mobility is either enhanced or degraded depending on the TSV position and transistor channel direction. Longitudinal tensile stress reduces the hole mobility while transverse tensile stress increases it.

In the following, we present reliability studies of Sn-based solder bump and copper and tungsten-based TSVs. We focus on the most critical issues: EM and mechanical stress.

EM IN PB-FREE SOLDER INTERCONNECT

In order to meet the demand for high density, utilizing solder bumps has become one of the key technologies for 3D die stacking. The reduced dimension is a critical issue to be investigated for both EM reliability and mechanical integrity of the solder bump. Many EM studies have been focused on the various combinations of UBM, solder composition, and BEOL structure to improve current density distributions and consequently EM reliability [7]. Pb-based solders have been used for the last five decades due to its advantages of low melting point and excellent wetting properties. However, Pb is harmful to the environment and health, and therefore use of Pb-based interconnects are banned across the world from all engineering application including microelectronic packaging. Pb-free flip chip solders are today widely used in many commercial products. However, the reliability for high performance logic chip application still has to be further improved. Typical solder bumps in flip chip technology are used to connect a functional silicon chip (top) with a certain FBEOL and UBM structure to a substrate (bottom). In this work we study EM behavior of Sn-based solder bump. Pure Sn has been identified as the best Pb-free solder for ultra-fine pitch solder bumps for advanced 3D packaging applications due to its baseline advantages of being electrodeposited and lower melting temperature.

EM Failure Modes of Sn Solder Bumps

The microstructure is defined by a network of grain boundaries and by the crystal orientation inside the grains. The network of grain boundaries influences the vacancy transport during EM in several ways. The diffusion of point defects inside the grain boundary is faster, when compared to grain bulk diffusion [8] due to the fact that a grain boundary generally exhibits a larger diversity of point defect migration mechanisms. Moreover, formation energies and migration barriers of point defects are, on average, lower than those for the lattice. In polycrystalline metals, grain boundaries are also recognized (together with dislocation loops) as sites of vacancy generation and annihilation [9], [10]. Therefore, the EM failure rate should depend on the grain size of the metallization. This dependence is well documented for Al interconnects; however, the dependence is found to be less pronounced in Cu interconnects. The probable reason is EM domination along interfaces in Cu interconnects. The Sn solder bump microstructure and interface reaction also play an important role in interconnect reliability. Compared to Cu, Sn crystallization produces 100-1000 times larger grains. Correspondingly, the role of grain boundaries as fast diffusivity paths is much more pronounced. Sn solder bumps often consist of several large Sn grains, such that most solder bumps exhibit one or at most a few Sn grain orientations [11]. Sn has a bulk tetragonal crystal structure which exhibits highly anisotropic diffusional, electrical, mechanical, thermal, and electrical properties [8]. A clear dependence of the thermo-mechanical response of a Sn solder bump on microstructure and Sn grain orientation was also observed [11]. The coefficient of thermal expansion is higher in the *c*-axis direction than in *a*- or *b*-axis directions.

Reliability testing of the Sn-based solder bumps has produced two EM failure modes [6] caused by Sn-crystal anisotropy:

- Mode 1. The cathode Ni barrier layer and the IMC remain intact while electromigration induced voids are formed at the Sn solder bump interface to the IMC.
- Mode 2. The Ni barrier layer and the IMC are depleted and swept away. Inside the Ni layer a void is formed.

General EM Model

A general, three-dimensional expression for the vacancy flux $\vec{J}_v$ driven by gradients of the chemical potential and EM is given by

$$\vec{J}_v = \frac{C_v}{k_B T} \overline{\overline{D}}_v (\nabla \mu_v + |Z^*| e \nabla \varphi). \quad (1)$$

The meaning of the symbols is as in [12]. Here we also introduce a tensorial diffusivity $\overline{\overline{D}}_v$ which describes the anisotropy of vacancy transport caused by the crystal properties and the influence of mechanical deformation.

The vacancy flux expression (1) and the models based on it have been widely used for the analysis of EM in dual-damascene copper interconnects. In order to model EM in solder bumps which, in addition to host atoms (e.g. Sn), also include impurity atoms (e.g. Ni, Cu), (1) must be extended. We assume that, prior to EM stressing, all impurity atoms have occupied substitutional positions. Thus, after applying electric current, EM removes the impurity atoms from their substitutional sites and causes them to drift. Each drifting host or impurity atom induces a movement of vacancies in a direction opposite to its drifting direction and the total vacancy flux is composed of the vacancies produced by the host atoms and the impurity atoms.

The total flux $\vec{J}_v^T$ is given by

$$\vec{J}_v^T = \vec{J}_v + \sum_i \vec{J}_v^i. \quad (2)$$

Here, $\vec{J}_v^i$ is the vacancy flux corresponding to impurity i and $\vec{J}_v$ is the flux of the host vacancies. $\vec{J}_v^i$ are expressed by expressions similar to (1), but specific diffusivity coefficients and effective charges must be used. Particularly, the effective charges can vary significantly [13], [14].

Simulation and Discussion

We have utilized an interconnect structure as presented in Fig.1. This structure consists of a Sn based solder bump with Ni under bump metallization at the cathode end. The cathode and anode ends are connected to copper interconnect layers. In order to study the complete problem we must consider EM in both Ni and Sn segments as well as at their interface.

As we know from experimental observations, at the interface between Ni and Sn, an inter-metallic compound is formed.

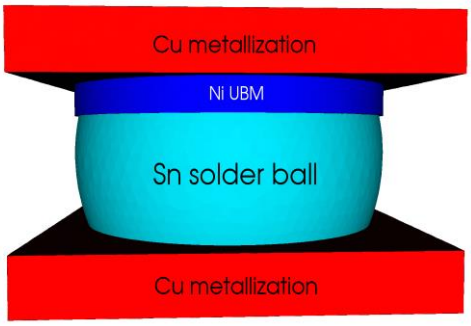

Figure 1. Solder bump structure used for simulation.

EM in the Sn and Ni segment is described by the standard EM model [12]. For the IMC we assume at first a simple Ni segregation model [15]. Ni has a face-centered cubic crystal and in the unstressed state self-diffusion and EM in such crystals is isotropic. In this work the predominant focus is on the effects of EM; therefore, the models for stress induced anisotropy of the diffusivity tensor are neglected [16].

The isotropic self-diffusivity coefficient of Ni is [17]

$$D_{Ni} = 2.9 \exp\left(-\frac{2.88\ eV}{k_B T}\right) \frac{cm^2}{s}. \quad (6)$$

Measurements of self-diffusion in Sn clearly show an anisotropic atomistic transport. From [18],[19] we have

$$D_{c,Sn} = 3.7\ 10^{-8} \exp\left(-\frac{0.25\ eV}{k_B T}\right) \frac{cm^2}{s}, \quad (7)$$

$$D_{a,Sn} = D_{b,Sn} = 8.4\ 10^{-4} \exp\left(-\frac{0.45\ eV}{k_B T}\right) \frac{cm^2}{s}. \quad (8)$$

First we consider failure Mode 1. Here the *c*-axis of the Sn grain exhibits a large angle with the current direction, where the rate of Ni diffusion in Sn is small. Failure is mainly due to Sn self-EM, resulting in a peak vacancy concentration between the IMC and solder (cf. Fig.2).

By rotating the Sn crystal by 90°, the crystal *c*-axis becomes aligned with the electric current direction. Ni atoms are transported from the Ni layer through the IMC into the solder bump below, where they electromigrate rapidly along the *c*-axis. At this instance, the peak in vacancy concentration occurs in the UBM Ni layer as can be seen in Fig.3. The locations of the vacancy concentration peaks in both failure modes correspond to sites of peaks of tensile stress, which are sites of void nucleation.

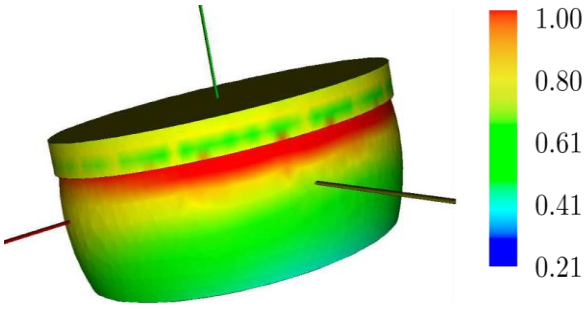

Figure 2. Normalized vacancy distribution in failure Mode 1. The peak concentration is reached in the bump.

Our simulations have shown that the crystal orientation in a Sn solder bump cannot be the sole reason for the difference in EM behavior between Mode 1 and Mode 2. Even if the EM of Ni in the *a*- and *b*-axis direction is much smaller than the EM in the *c*-axis direction, it is still higher than Sn self-

EM, so we would expect a similar behavior in both failure modes. We conclude that the structure of the transition region (IMC) plays a significant role. This structure, in the case when the Ni layer is attached to the *a*- or *b*-axis oriented crystal, is such that it represents a barrier for EM of Ni atoms. In our simulation we have applied a segregation model [15] to describe the capturing of Ni atoms in the IMC. The anisotropy of Ni diffusion in Sn is much more pronounced than the anisotropy of Sn self-diffusion. In the case of fast *c*-axis Ni diffusion in Mode 2 we have an

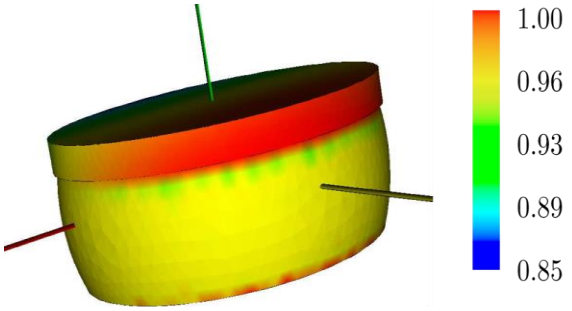

Figure 3. Failure Mode 2 - large portion of UBM with high vacancy concentration.

additional effect: the Sn crystal orientation produces an IMC structure which is preconditioned for a fast dissolution. This dissolution subsequently drowns atoms from the UBM causing the failure in Mode 2.

More detailed simulations based on molecular dynamics could eventually deliver results to design a more accurate phenomenological model for the IMC.

In Fig. 4 we compare the time dependent rise in the vacancy concentration due to Sn self-diffusion and self-EM for different crystal orientations. Three cases are studied:

- c-axis is parallel to electric current direction
- c-axis is rotated by θ = 30◦
- c-axis is rotated by θ = 60◦

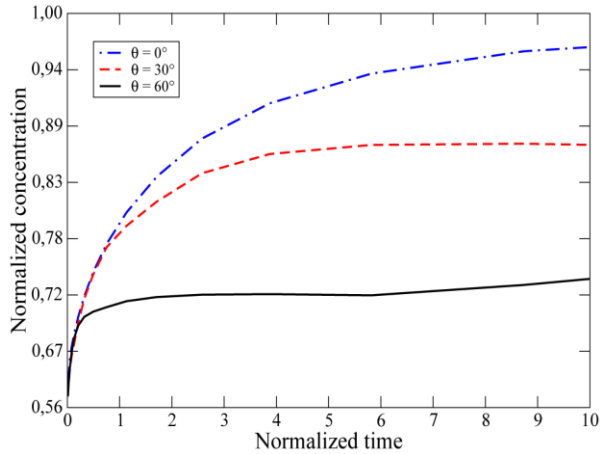

Figure 4. Increase in vacancy concentration in failure Mode 1 for three different crystal orientations.

The impact of the IMC and the Ni-related vacancy-influx is neglected in order to obtain a clear picture of the influence

As we can see in Fig.4, a crystal rotation causes a reduction of the EM intensity. We denote with θ an angle between the current density and the *c*-axis of the crystal. By comparing the curves for $\theta = 0^{\circ}$ and $\theta = 60^{\circ}$ we see that the vacancy concentration at $\theta = 0^{\circ}$ keeps rising, while the curve at $\theta = 60^{\circ}$ stays almost at equilibrium. This result helps to understand the experimental observation of failure development in solder bumps which consist of two large grains. In these cases the grain with the *c*-axis oriented in parallel to the electron flow is completely swept away, while the other grain is still intact [11].

EM VOIDING IN COPPER TSV

In this section we present results of investigations of the electromigration failure mechanisms in copper dual-damascene lines with a TSV located at the cathode end of the line. The resistance change of such interconnect structures is studied based on 3D numerical simulations. We show that imperfections at the TSV bottom originated from the fabrication process can lead to an additional failure mechanism, where a significant resistance increase is caused by small voids under the TSV. In addition, an analytical model is proposed to describe such a failure mechanism.

Modeling

In [20] electromigration experiments using downstream electron flow show void formation and growth under the TSV at the cathode end of a line as sketched in Fig. 5 and Fig. 6. It was observed that the development of the resistance as a function of time can be divided in two periods: at first the resistance remains practically constant, which is then followed by a measurable resistance increase. Failure analyses indicated that during the first period the void diameter is smaller than the TSV section, while the measurable resistance increase period starts as soon as the void diameter becomes larger than the TSV section. Considering a cylindrical void under the TSV, as shown in Fig. 6, and that $r_{void} > r_{TSV}$, the resistance change is modeled as [20]

$$\Delta R(r_{void}) = \frac{\rho_b}{2\pi t_b} ln\left(\frac{r_{void}}{r_{TSV}}\right), \quad r_{void} > r_{TSV} \qquad (9)$$

where r_{void} and r_{TSV} are the void and the TSV radii, respectively, ρ_b is the barrier resistivity, and t_b is the barrier layer thickness at the bottom of the via. Assuming isotropic void growth, the resistance change as a function of time is given by [20]

$$\Delta R(t) = \frac{\rho_b}{2\pi t_b} ln\left(\frac{t}{t_0}\right), \quad t > t_0 \qquad (10)$$

with

$$t_0 = \frac{\pi h r_{TSV}^2}{A_l v_d} = \frac{\pi h r_{TSV}^2\, kT}{A_l D_v e\, Z^* \rho j}, \qquad (11)$$

where h is the copper line thickness, A_l is the line cross sectional area, v_d is the vacancy drift velocity, D_v is the vacancy diffusivity, e is the elementary charge, Z^* is the effective charge, ρ is the copper resistivity, and j is the applied current density. t_0 is the time at which the void radius becomes equal to the radius of the TSV and the logarithmic resistance increase starts. Thus, (10) is valid for the period $t > t_0$, when $r_{void} > r_{TSV}$.

Although Frank *et al.* [20] assumed that the resistance trace is constant for $t < t_0$ (i.e. $r_{void} < r_{TSV}$), void growth under the TSV leads, in fact, to a small resistance increase which cannot be experimentally measured. In this case, the resistance change is caused by the reduction of the effective conducting area in relation to the cross sectional area of the TSV. Therefore, the resistance change is given by [21]

$$\Delta R(r_{void}) = \frac{\rho_b t_b}{\pi r_{TSV}^2}\left(\frac{\left(r_{void}/r_{TSV}\right)^2}{1-\left(r_{void}/r_{TSV}\right)^2}\right) \qquad (12)$$

for $r_{void} < r_{TSV}$, and the resistance change as a function of time becomes

$$\Delta R(t) = \frac{\rho_b t_b}{\pi r_{TSV}^2}\left(\frac{t/t_0}{1-t/t_0}\right), \quad t < t_0 \qquad (13)$$

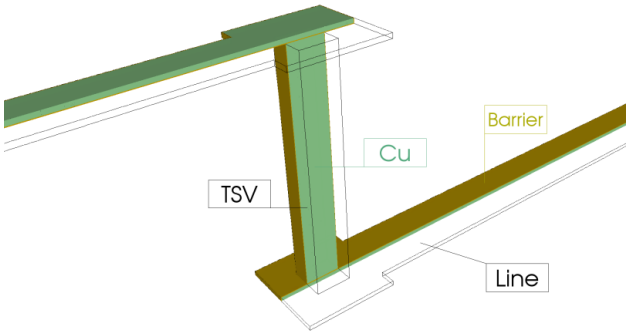

Figure 5. Copper dual-damascene line/TSV structure.

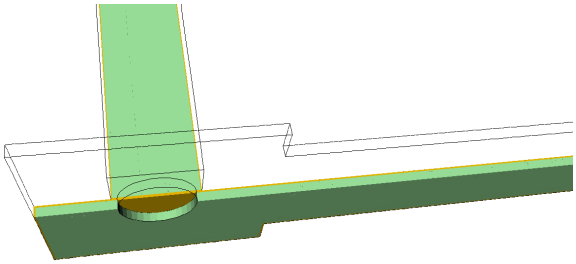

Figure 6. Detail of the TSV bottom and void under the via.

It should be pointed out that the models derived above assume a circular TSV, while the via used in the experimental test structure described in [20], [22] and used in this work is approximately square. Therefore, r_{TSV} should be viewed as an effective via radius. This does not affect the modeling and later we will show that r_{TSV} can be determined by fitting (9) and (12) to the curves of resistance change as a function of void radius obtained from numerical simulations.

Simulation and Discussion

The resistance change caused by the growth of a void located under the TSV was determined from numerical simulations. The geometry, dimensions, and material parameters of the interconnect structure were obtained from [20]. A detailed view of the structure and void at the TSV bottom is shown in Fig. 6. Considering the modeling described above, a cylindrical void is placed under the via and its radius is gradually incremented. For each void size the resistance of the interconnect is determined from the numerical solution of the Laplace equation. In this way we are able to extract the resistance change of the interconnect sketched in Fig. 5 for the whole period of void growth.

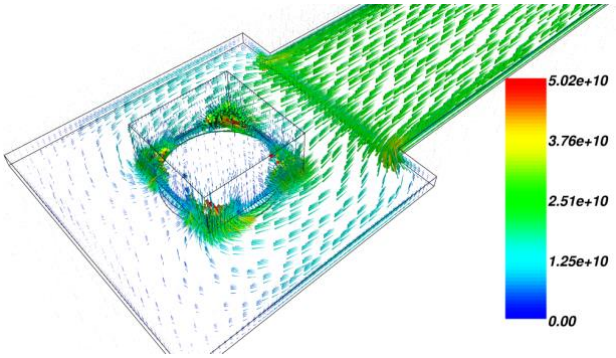

Figure 7. Electron current density distribution (in A/m^2) under the TSV in the presence of a void. Current crowding towards the corners of the via can be seen.

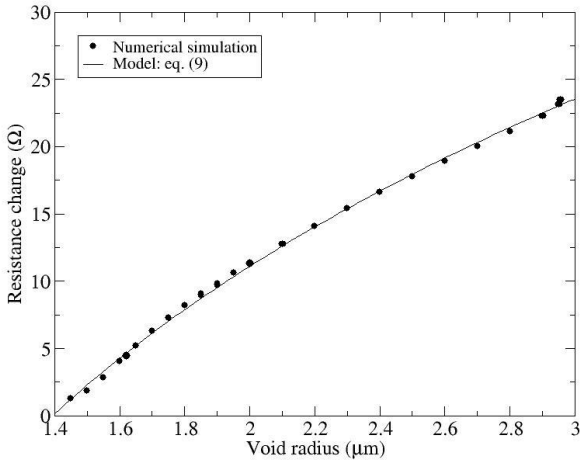

Figure 8. Interconnect resistance change as a function of void radius for $r_{void} > r_{TSV}$.

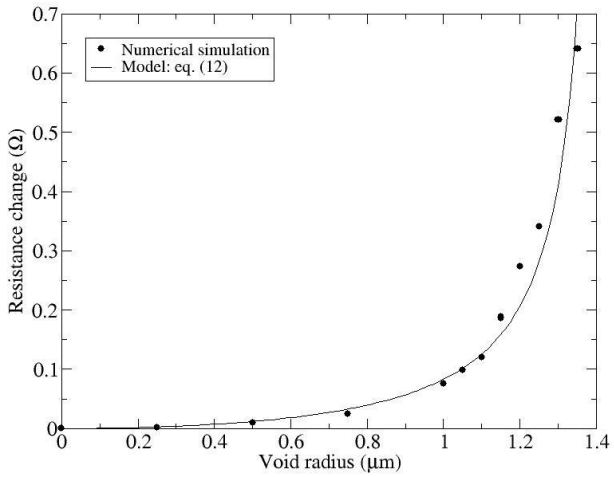

Figure 9. Change as a function of void radius for small voids ($r_{void} < r_{TSV}$).

Fig. 7 shows the electron current density distribution at the TSV bottom in the presence of a void. The void causes a reduction of the effective conducting area at the TSV bottom. The electron flow is displaced towards the corners of the via, which leads to current crowding in this region, as can be readily seen in Fig. 10. The resistance change as a function of void radius is shown in Fig. 8 and Fig. 9.

THERMOMECHANICS OF OPEN TSV

In this section a reliability evaluation of a specific TSV technology [23] is carried out. The goal is to gain advanced insight into material performance and reliability issues. This particular 3D integration technology uses wafer bonding and TSVs to directly integrate low output sensors with their associated analog amplification and signal processing circuitry. A diagram of the TSV structure is presented in Fig. 10. The tungsten metallization and the SiO_2 passivation are deposited conformally on the TSV surfaces following the Si etch process. Typical TSV Si etch dimensions are 250μm and 100μm for depth and diameter, respectively [24].

The impact of stress can be controlled by the choice of the materials and the geometry, which forms the TSV. A good design should manage the mechanical issues while ensuring the electrical functionality of the device. One of the most common and well documented layouts is the cylindrical copper TSV. The good electrical properties of copper and the fabrication easiness are clear advantages of this technology. However, the difference of more than one order of magnitude between silicon and copper CTEs (coefficient of thermal expansion) negatively affects mechanical reliability. The TSV technology considered in this work uses the open via strategy to diminish the mechanical impact in the silicon. Furthermore, the adoption of tungsten as via metal enhances the mechanical stability of the structure [25] due to the low CTE mismatch between tungsten and silicon. Although this TSV technology has several advantages regarding the mechanical stability of the via surroundings, the via itself gives stress related issues. Tungsten films usually possess high residual stress after the deposition process and this stress can lead to cracking of the material or detaching of the film layer and, consequently, a TSV failure. Therefore, the understanding of the stress development in the metal layer is necessary to predict failure scenarios.

During thermal cycling, 3D geometrical features influence the distribution of mechanical stress, especially at the top and bottom of the via. Hence, 3D simulations enable the determination of sites which are particularly exposed to high mechanical stress. The device is expected to work properly in the temperature range of -40 ◦C to 125 ◦C. With our simulation we assess the mechanical response of the structure in this scenario considering the stress free temperature of 25 ◦C, although, the existence of residual stress in the metal layer of the TSV is known [26]. Furthermore, pre-stress in elastic simulations would only bias the final stress without major modifications to the general behavior. For the simulation we take advantage of the cylindrical symmetry of the structure to reduce the size of the problem and speed up the meshing process and the simulation itself. In this way only one-quarter of the structure is considered. The mesh is given in Fig. 11 and Fig. 12 shows the von Mises stress for one quarter of the TSV. In the 3D case, one can see that the highest stress has developed in the metal layer at the bottom and near the top of the structure. Here we have a combination of two impact factors: the first is the thermal mismatch between the metal and the surrounding layers and the second is the geometry. High mechanical stress in connection with microstructural properties, which weaken the stability of the crystal (dislocations, grain boundaries), can cause a fracture of the metal layers ending in complete failure of the TSV.

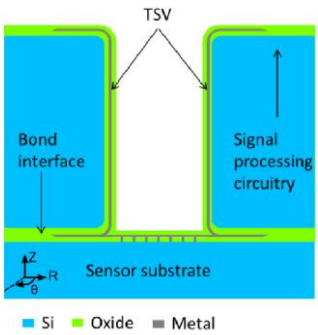

Figure 10. Schematic overview of 3D integrated technology using waferbonding and TSVs [23].

CONCLUSION

Interconnect structures for 3D integration technology introduce a considerable number of new reliability issues. As in the case of planar technologies, the interconnects are affected by degradation due to electromigration and mechanical stress, however, the specific structures for 3D integration, such as TSVs and solder bumps, open the possibility for completely new failure scenarios. In this work we have presented TCAD reliability studies of TSV and solder bump technologies for 3D integration. Prior to studying each of the particular cases, applied models for

electromigration and mechanical stresses are discussed. Also, an overview of the main experimental and TCAD modeling/simulation reliability investigations are provided. The results and discussion of TCAD studies in combination with experimental findings have a potential to essentially improve the understanding of degradation mechanisms of important components of 3D interconnect technology.

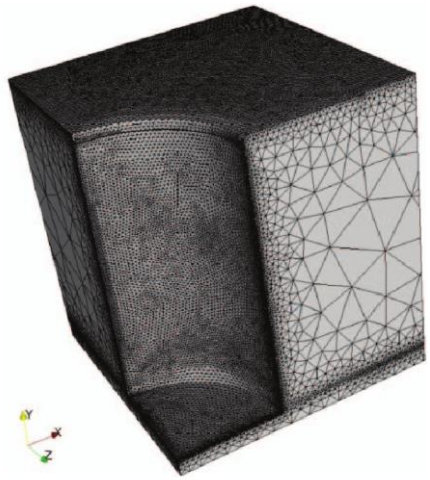

Figure 11. 3D mesh used for simulation.

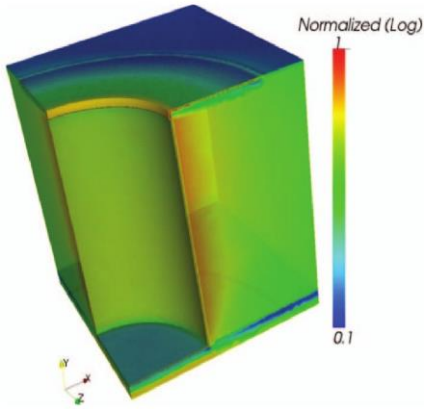

Figure 12. 3D von Mises stress in log-scale.

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