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A method to determine the lateral trap position in ultra-scaled MOSFETs

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Abstract

We propose the new method for the evaluation of the lateral trap position in ultra-scaled MOSFETs with a precision of less than 1nm. The method is based on a simple analytical model which links the surface potential in the presence of a discrete trap and the drain voltage. To verify this analytical approach we employ the TCAD data obtained on test both n- and p-MOSFETs with different channel lengths.

1. Introduction

Stress induced build-up of charged defects can heavily disturb the electrostatics of a MOSFET. This results in a local perturbation of the surface potential, and, hence, in a threshold voltage shift [1]. Defects situated in different places in the device can essentially disturb the device performance. As such, the information about the spatial position of the trap is of great importance. Several papers devoted to the effect of the defect position on the MOSFET performance have been published so far [2-4]. In some of them, however, the impact of random dopants and traps on the channel potential is not considered [2-3]. Other authors mainly focus on the impact of the trap depth in the oxide [4].We present an analytical model which demonstrates that the lateral channel position of the interface trap X_T can be extracted from the dependence between the surface potential shift in the damaged region $\delta\psi^T_s$ and the drain voltage V_d. Special attention is devoted to random dopants effect.

2. Model description

The distribution of the surface potential in a MOSFET is basically obtained as a solution of the Poisson equation with corresponding boundary conditions [5-6]. In this work we consider n- and p-MOSFETs with a single discrete interface trap. We use an analytical expression linking the local surface potential near a trap ψ^T_s with the lateral position X_T and the applied drain voltage V_d. This problem is a particular case of that discussed in [6]. In the case of a discrete interface trap, the width of a damaged region is small (e.g. 0.1nm) and the expression is:

$$\psi_s^T(X_T,V_d) = V_G - V_{FB} - \frac{Q_{dep}}{C_{ox}} - \frac{qN_f}{C_{ox}} + b(X_T,V_d)e^{kX_T} + c(X_T,V_d)e^{-kX_T} \quad (1)$$

where V_G is a gate bias, V_{FB} is a flat-band voltage, Q_{dep} is a total charge inside the depletion layer, N_f is a density of the interface charges, and k is a function of the depletion layer depth y_d [6]. The relations for coefficients $b(X_T,V_d)$ and $c(X_T,V_d)$ are similar to those obtained for the damaged region in [6]. The shape of $\psi^T_s(V_d)$ characteristics is thus defined by the trap position X_T and allows to extract it.

3. Results and discussion

The TCAD simulations were performed on n-MOSFETs (N_A=10^{18} cm^{-3}) and p-MOSFETs (N_D=$6\cdot10^{17}$ cm^{-3}) with channel lengths L=35nm and L=100nm respectively. Initially the surface potential distribution along the Si/SiO$_2$ interface has been extracted for numerous lateral positions of discrete interface traps. The results for both n- and p-MOSFETs with three different positions of the interface traps are given in Fig.1. The charged interface trap induces a local shift of the surface potential with the position of the potential minimum/maximum for an n-/p-MOSFET exactly corresponding to the trap position.

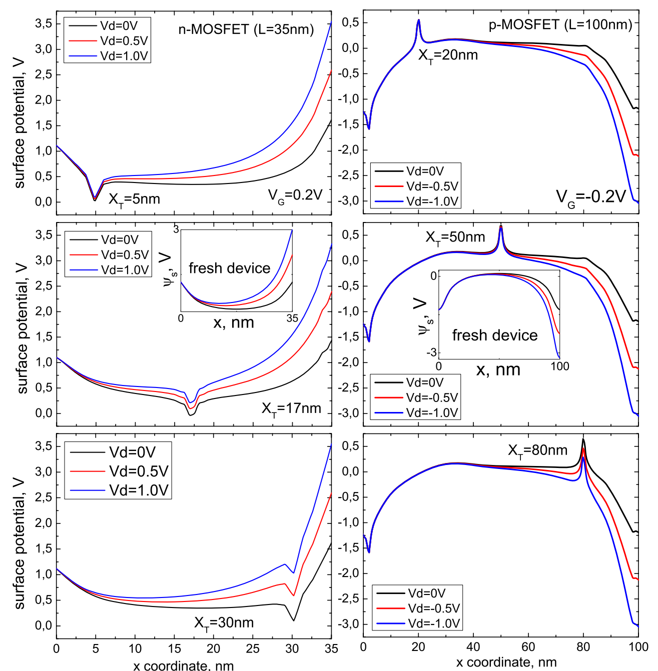

Fig. 1 Surface potential distribution along the interface.
Left: n-MOSFET, right: p-MOSFET. The insets illustrate the surface potential of the device without traps. Traps are located near the source (upper plots), in the center of the device (center plots) and close to the drain (lower plots).

In addition, one can see that this local surface potential shift depends on the applied drain voltage V_d and that this dependence becomes stronger as the trap is shifted towards the drain.

The change of $\psi^T_s(V_d)$ characteristics as X_T varies has been studied in detail. Hundred different random dopants configurations have been examined for each trap position, see Fig. 2.

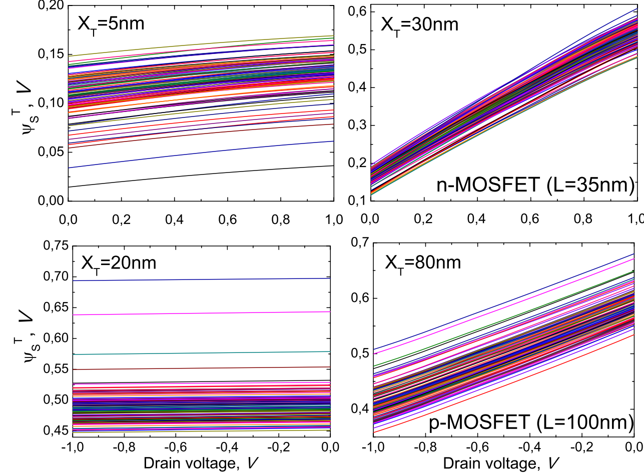

Fig. 2 $\psi^T_s(V_d)$ characteristics for the different trap positions. Top: n-MOSFET, bottom: p-MOSFET.

The obtained characteristics can be linearly parameterized as follows:

$$\psi^T_s(X_T,V_d) = p(X_T)V_d + \psi^T_s(X_T,V_d=0) \tag{2}$$

The slope p as a function of X_T is plotted in Fig. 3, where the standard deviations due to random dopants are considered. One can see that the slope of $\psi^T_s(V_d)$ is almost not affected by random dopants, especially for the device with longer channel. It also strongly increases if the trap is located closer to the drain. In contrast, the intercept $\psi^T_s(X_T,V_d=0)$ may be different for different random dopant configurations and also almost symmetrical with respect to the middle of the channel (Fig. 3, inset). Thus, extraction of

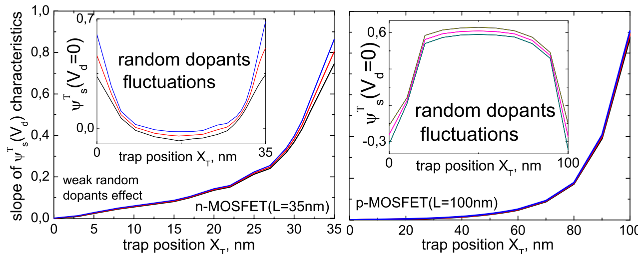

Fig. 3 Slope of $\psi^T_s(V_d)$ characteristics versus X_T for both devices. The intercepts $\psi^T_s(X_T, V_d=0)$ are plotted in the insets.

the trap position based on this characteristic appears problematic. Rather, only the V_d-induced shift of the local surface potential $\delta\psi^T_s$ has to be used:

$$\delta\psi^T_s(X_T,V_d) = p(X_T)V_d \tag{3}$$

In Fig.4 one can see that $\delta\psi^T_s(V_d)$ characteristics extracted from TCAD simulations are reasonably reproduced by those obtained with the analytical approach. The slope p calculated with our model vs. X_T is in good agreement with the TCAD results (Fig.4, insets).

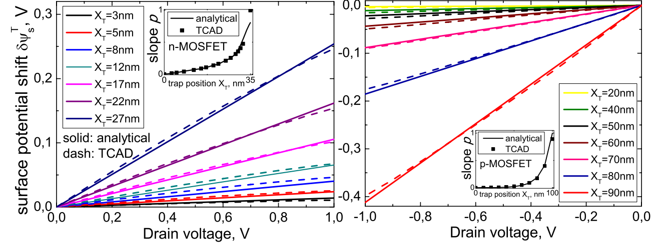

Fig. 4 $\delta\psi^T_s(V_d)$ characteristics for different trap positions. Left: n-MOSFET, right: p-MOSFET.

The abrupt growth of $p(X_T)$ allows us to determine the trap position with very high precision of less than 1nm. Especially high accuracy will be reached close to the drain.

3. Experimental realization

The proposed method may be further verified experimentally. The setup for this can be realized using the Kelvin probe force microscopy (KPFM) equipment [7] with the possibility to apply V_d. Thus, the surface potential distributions measured at different V_d will allow the extraction of $\psi^T_s(V_d)$ dependences. After this the background $\psi^T_s(V_d=0)$ has to be subtracted in order to get the $\delta\psi^T_s(V_d)$ characteristics and fit them with analytical results (e.g. Fig.4).

4. Conclusions

An analytical expression linking the trap-induced surface potential shift with the applied drain voltage and trap position has been derived. The results obtained with the proposed model are in good agreement with TCAD simulation data for n- and p-MOSFETs with different channel lengths. The lateral position of the charged interface trap can be evaluated with a good precision of less than 1nm. The main advantage of the method is that the random dopant fluctuations have almost no influence on its accuracy. The proposed technique has a high potential of practical realization using modern scanning probe microscopy techniques.

Acknowledgements

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