Use of SSTA Tools for Evaluating BTI Impact on Combinational Circuits

Vinicius V. A. Camargo, Ben Kaczer, Gilson Wirth, *Senior Member, IEEE*, Tibor Grasser, *Senior Member, IEEE*, and Guido Groeseneken, *Fellow, IEEE*

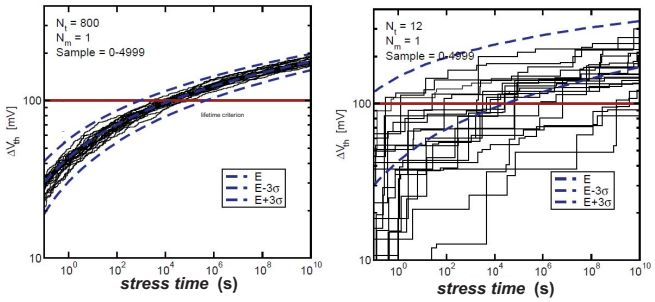
***Abstract*— This paper presents an extensive statistical study on the impact of bias temperature instability (BTI) on digital circuits. A statistical framework for the evaluation of BTI at the electrical (SPICE) level, enhanced by an atomistic model for BTI, is introduced. This framework is then employed to perform the timing analysis of different combinational paths using cells from a given library, aiming to statistically model BTI at the higher abstraction level. A statistical static timing analysis (SSTA) method is then performed and the results are compared to detailed simulations using atomistic models based on experimental data. The comparison between the two methods shows that for large paths both methods converge to the same distribution for the delay while for short paths the delay distributions are different causing the SSTA method to generate misleading results. An analysis is then performed in order to understand and formalize the results.**

***Index Terms*— Bias temperature instability (BTI), reliability, statistical static timing analysis (SSTA), variability.**

I. Introduction

STANDARD cell methodology is widely used for the design of application-specific integrated circuits (ASICs). During each step of this design flow, the designer is aided by static timing analysis (STA) tool, which is the tool responsible to verify if the time constraints are being accomplished. The principle of the STA tool is to sum the delay of each cell and connection in a circuit's path, according to its position in the path. In order to do that, each cell is characterized by its delay for different input signals with different fan-outs. This is done for different process-voltage-temperature corners.

The downscale of the transistors together with limitations in the manufacturing process produces new sources of variability that must be taken into account during the design stage. All these sources convert to variability in the electrical characteristics of the transistor and propagate to the higher levels of the design [1]. The traditional corner analysis is not able to deal well with the high variability in state-of-the-art transistors, leading to overpessimistic designs. As the parameter uncertainty becomes larger, it may be advantageous, in some circumstances, to sacrifice yield to gain in performance. To solve this problem during the design flow, the STA tools were improved to be able to deal with these issues and started to be called statistical STA tools, or just statistical static timing analysis (SSTA). SSTA tools, together with their compatible characterization tools, analyze the circuit considering the parameter variability through statistical methods, such as linear sensitivity analysis [2]–[4]. They predict the probability density function (pdf) of electrical performance. Because aging effects were not considered to be stochastic in the past, the design of the SSTA tools was originally done to consider only process variations at the starting time. These process variations are usually described following normal distributions for parameters such as threshold voltage (V_{th}) and transcondutance. This way, the linear sensitivity analysis method presents a satisfactory response.



(a) (b)

Fig. 1. (a) Random properties of many defects in large devices average out, resulting in a well defined lifetime. (b) Stochastic nature of fewer defects in deeply scaled devices becomes apparent. Figure first presented in [7].

Bias temperature instability (BTI) is a critical reliability mechanism that affects device electrical parameters such as the V_{th} [5]. It is caused by charging of defects in the gate oxide. In large devices of older CMOS technologies, BTI was considered to be a deterministic effect for a given circuit and stress condition. New "atomistic" studies show that the BTI degradation (aging) in state-of-the-art technologies based on deeply scaled transistors will lead to a huge increase in time-dependent variability [6]. This trend is illustrated in Fig. 1.

The literature presents suggestions on how to include the BTI and other aging effects in the (S) STA tools [8]–[12]. These works, however, are all based on the assumption that

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V_{th} degradation due to BTI is either deterministic or follows a normal distribution. Yet, we could not find any commercial tools that are already available using any of the approaches suggested in the literature. Due to this, in order to consider aging effects in the (S) STA tools available in the market, we propose a "time" corner to be defined for the desired life expectancy of the circuit, and characterization to be performed for each aged cell.

This paper implements a characterization method for the linear sensitivity analysis-based SSTA tools, and compares it to the result of a SPICE simulation enhanced with an atomistic model for BTI. The study aims to evaluate the viability of modeling BTI degradation as normally distributed when performing SSTA simulations. First, our BTI model applied in the electrical simulations is introduced. Then, we present our SPICE-based simulation framework, which is enhanced using atomistic simulations and used as reference to evaluate the SSTA model. Then, aiming to evaluate the use of SSTA tools for BTI analysis, the comparison methodology and the paths used for simulation are presented. Finally, we present the results of the comparisons and the conclusions of this paper.

II. Atomistic BTI Model and Simulation Framework

BTI is a degradation phenomenon well discussed in the literature due to its importance in transistors aging and in circuits' reliability over time. Recent studies presented a new way to model BTI assigning the increase of transistor V_{th} to charge traps [13]. According to this model, each transistor has a certain number of traps in its dielectric, which become populated (occupied by a charge carrier) during operation. An occupied trap causes an effect that can be modeled as an increase in V_{th}. With the transistor stressed, there is a tendency of traps to become populated, increasing transistor degradation. Here, we assume that trap capture times are uniformly distributed on a logarithmic scale, while the V_{th} shift caused by each trap follows an exponential distribution with the average inversely proportional to the area of the device. The number of traps per device is assumed to follow a Poisson distribution with its average proportional to the area of the device. These assumptions have been experimentally verified and are well accepted in the literature [6], [14].

In order to properly simulate the BTI effect at the electrical level, a tool that implements the model based on the "atomistic" level is needed. This tool should be capable of following the traps' states in each transistor at each instant of time. Moreover, since the traps' chances of being occupied are a function of the environmental conditions, such as the electric field or the temperature, this tool should be integrated to an electrical simulator. The details of the implementation of this tool are described in [7].

In order to simulate the defect activity in an electrical simulation, a Verilog-A component modeling a transistor according to the BSIM4 model was used and enhanced in accordance with the behavioral description of the traps. During a transient electrical simulation, at each time step the solver calculates all the variables in the circuit. By adding the traps' kinetics into a Verilog-A component that models a transistor, the traps' activities get included into the solver calculus and are then evaluated at each step. This way, it is possible to track the trap occupancy at every time step of the simulation, and in the same way every step of the simulation accounts for the trap state producing an accurate result.

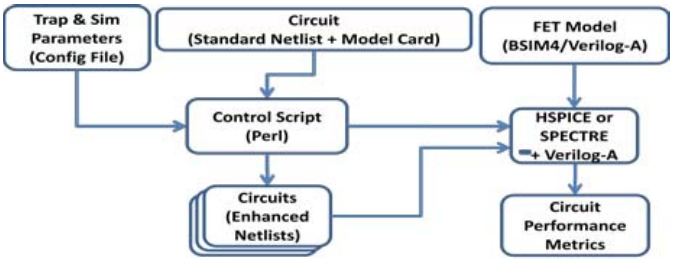


Fig. 2. Netlist and the traps' parameters are used as inputs. The control script organizes the information and creates an enhanced netlist which is run by the solver.

The probability of a trap to change its state (from populated to empty and vice versa) follows (1), where Δt is the time step of the simulation, "p" is the process, either capture (c) or emission (e), and τ is the time constant. The bar indicates the complementary process. It is important to remember that the time constants are a function of bias point and environmental parameters, such as temperature and stress voltage applied at that given time step [15], [16]

$$P_p = \frac{\tau_{\overline{p}}}{\tau_e + \tau_c} \left\{ 1 - \exp\left[- \left(\frac{1}{\tau_e} + \frac{1}{\tau_c} \right) \Delta t \right] \right\}. \quad (1)$$

Based on the probability of the trap to change its state, the simulator randomly defines the state of the trap for the next time step. For each populated trap, its related V_{th} shift is added to the VTH0 parameter in the FET Model used to model the transistor. The process is repeated for all traps in all transistors at each simulation step.

Trap properties, such as their time constants and the induced V_{th} shift, are generated by the control script which also parses a standard SPICE netlist in order to rewrite it including the traps descriptions on each Verilog-A component instance. Since the number of traps and its properties are a function of transistor parameters, such as area, the control script first reads the netlist in order to identify all the transistors and their parameters. After this, the simulator has all transistor and technology data, informed in the Config File, and generates the number of traps and their properties. The SPICE netlist is rewritten with the trap properties, here referred as enhanced netlist, and then run in the solver. The entire simulation framework is illustrated in Fig. 2.

III. BTI Evaluation in SSTA

The SSTA method used here to evaluate BTI effects on circuits is based on the linear sensitivity analysis, which is the method used by the most commercial SSTA tools. This method first simulates the circuit with all parameters at nominal values and then performs one new simulation for each random parameter. The simulations are used to evaluate numerically the derivative of the output regarding each one of the random parameters and the mean value of the output. These

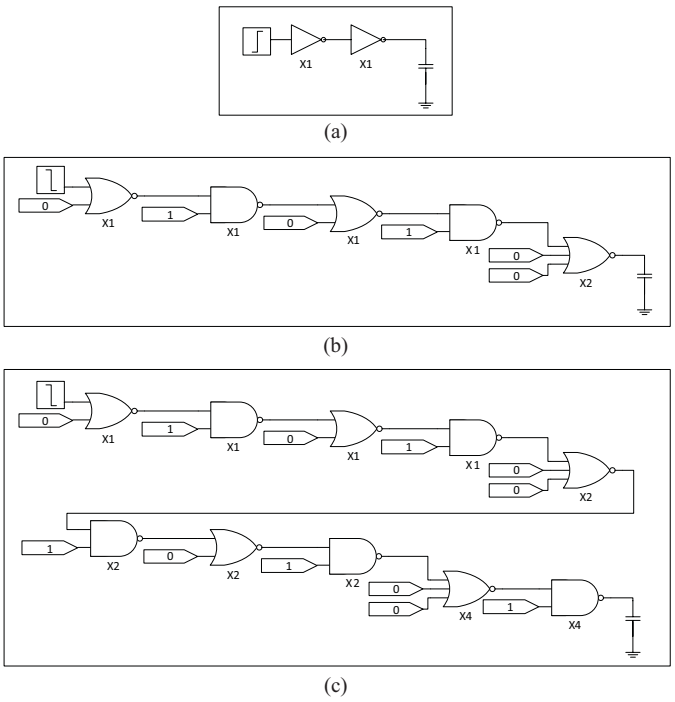


Fig. 3. Schematic of the analyzed paths. (a) Path 1. (b) Path 2. (c) Path 3.

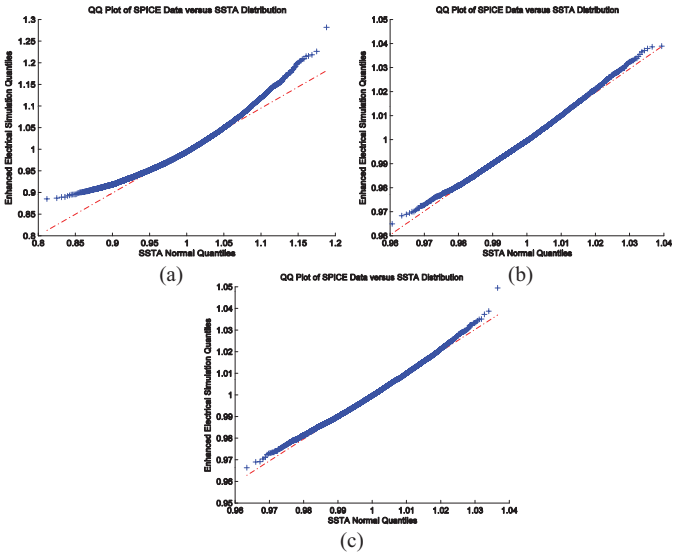


Fig. 4. Q–Q plot of the normalized delay generated by the electrical simulation in comparison with the one generated by the SSTA analysis in (a) path 1 after 10^4 s, (b) path 2 after 10^4 s, and (c) path 3 after 10^4 s.

derivatives and the pdf of the random parameters are used as inputs and combined to evaluate the standard deviation of the output [17]. Once the tool has evaluated the delay pdf of each cell, it makes a sum of the delay on each stage finding the possible critical paths. Changes in the waveform and power consumption are also evaluated. This method assumes the pdf of each parameter as a normal distribution and a linear dependence between parameters and output.

In order to characterize the cells for a linear sensitivity analysis-based SSTA tool, it is needed to obtain not only the fan-out versus slope tables for a cell with its parameters at nominal values, but also a new version of this table, changing each random parameter in the design allowing the SSTA tool to evaluate the derivatives used in the linear sensitivity analysis. For the sake of simplicity and to have a result that can be easily interpreted, the only random variable reported on each transistor due to BTI will be the V_{th}. All this information is generated by ordinary SPICE simulations and then translated into a Liberty file which is later used by the SSTA tool.

The third step of the process is to obtain the random parameter distribution in a transistor after the amount of time that will be defined in the time corner of the SSTA analysis. In this paper, this information was generated by an electrical simulation using the enhanced SPICE simulator presented in Section II, but this may be also a parameter provided by the foundry. This information is used as an input to the SSTA tool. In our case, we defined the amount of operation time to be 1, 10^4, and 10^8 s. In the first analysis, only trap-dependent variability (BTI) will be considered; on further analysis, the time zero variability is also included.

IV. Simulation, Results, and Discussion

Aiming to assess the accuracy of the SSTA simulation method to evaluate the BTI phenomena on circuits, a comparison between the SSTA method and the electrical simulation presented in Section II was performed.

Once the library is properly characterized and the statistical data of the BTI degradation are obtained, it is already possible to run the SSTA simulations. As a case study, we define three circuits on which we will compare the SSTA results with the enhanced SPICE ones. In order to study the behavior of circuits with different complexity, we selected three circuits with different logic depths. They are shown in Fig. 3.

The electrical simulations were performed using the Monte Carlo method. The number of runs was 10 000, producing a sampling error of 0.0244 in the skewness and 0.0489 in the kurtosis according to [18]. The library used in this paper was the Nangate Open Cell Library for a 45-nm technology node used together with a PTM model [19].

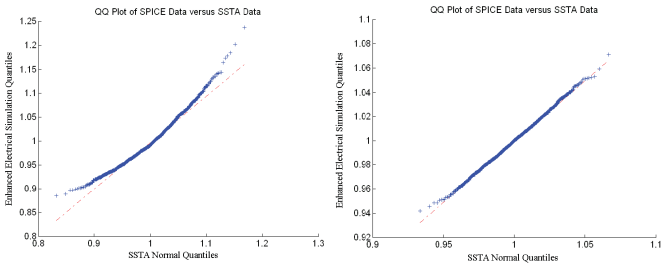
The distributions obtained with both methods are graphically compared using Q–Q plots. This kind of plot technique is used to compare different pdfs highlighting the differences in the tails of the distributions. In [20], a brief explanation is presented about this kind of graph and how it is built.

Fig. 4 compares the delay obtained by the enhanced electrical simulation to the delay obtained by the SSTA method, after a stress time of 10^4 s. The delay is normalized by its mean value. The result obtained by the SSTA method is a normal distribution, and hence represented by the dashed lines (straight lines) in the Q–Q plots. It is important to pay attention to the tails of the distribution, where the failing circuits are located. Looking at the tails, one can see a significant difference between both methods for the case study with less complex paths, while for the more complex paths the error is less severe.

Table I presents both skewness and kurtosis of the distributions versus the depth (measured in logic stages) at the different stress times. The kurtosis value was chosen because it is the most representative value of the weight of the tails of a distribution, while the skewness is the measure of the pdfs asymmetry. For a normal distribution, the value of the kurtosis

TABLE I
DELAY DISTRIBUTIONS CHARACTERISTICS FOR THE THREE STUDIED PATHS FOR DIFFERENT STRESS TIMES

	Stress Time	Skewness	Kurtosis
Path 1 (1 logic stage)	1s	0.7211	3.7664
	10^4s	0.7033	3.6994
	10^8s	0.7439	3.8634
Path 1 (5 logic stages)	1s	0.2201	3.1849
	10^4s	0.2021	3.0134
	10^8s	0.2827	3.0344
Path 3 (10 logic stages)	1s	0.2153	3.0615
	10^4s	0.2258	3.1128
	10^8s	0.2066	3.0468



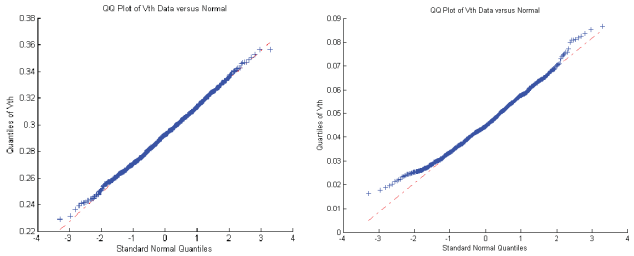
(a) (b)

Fig. 5. Q–Q plots of the delays on paths (a) 1 and (b) 2 after 10^4s of stress considering time zero variability.

should be equal to 3 and the value of the skewness should be equal to zero. This table shows a tendency of the delay's pdf to become closer to a normal distribution as path complexity increases. The accuracy of the SSTA tool to evaluate the chance of a timing violation is correlated with the normality of the path's delay.

Let us focus first on Fig. 4(a), which is the case where the error of the SSTA tool is the largest. Since there is just one logic stage, the linear sensitivity analysis is evaluated only for that cell. The linear sensitivity analysis assumes that the input random variables are all given by normal distributions. In the BTI case, these random variables are the V_{th} of both the pMOS and nMOS transistors in the gate. Because these random variables are not normally distributed [22], it leads to an error in the shape of the delay distribution. The other important error generated by the linear sensitivity analysis is the fact that it considers the delay as a linear function of the input random variables, leading to minor errors both in the mean and in the variance of the result distribution. The result presented by the enhanced electrical simulator is considered to be accurate since its distribution is automatically generated based on experimental data for the distributions of the trap properties and in first principles.

Another series of simulations were run to evaluate the impact of the time zero variability. The time zero variability is usually modeled by adding to the V_{th} a normal distributed variable, with mean equal to zero and the standard deviation being a function of the technology node and transistor size [24]. In this case, the standard deviation is assumed to be 10% of the V_{th} for a transistor with the minimal dimensions for the 45-nm technology [21]. The standard deviation was considered to be inversely proportional to a transistor channel area.



(a) (b)

Fig. 6. Threshold voltage distribution due to NBTI (a) considering time zero variability and (b) not considering time zero variability.

TABLE II
DELAY DISTRIBUTIONS CHARACTERISTICS FOR CIRCUITS FROM THE ISCAS'85 BENCHMARK

Circuit		From	To	Depth	Skewness	Kurtosis
c17	setup	n6	n22	3	0.5777	3.5426
c880	hold	n89	n450	3	0.5720	3.6315
c880	setup	n51	n878	24	0.2502	3.0546
c6288	hold	n1	n545	1	0.7904	3.9095

The simulation of the delay on paths 1 and 2 after 10^4s is presented in Fig. 5, where it is possible to see a smaller difference between the results obtained by the electrical simulation and by the SSTA method. This happens because the pdf of the V_{th} becomes the sum of two distributions, one of those is a normal, making the V_{th} pdf more normal like and then more suitable for studies using linear sensitivity analysis. Fig. 6 shows the distribution of the V_{th} due to NBTI in a transistor considering (a) and not considering (b) the time zero variability.

Despite the error for path 1, paths 2 and 3 presented a result much closer to the ones obtained by the SSTA method. As path complexity increases, SSTA accuracy clearly increases. This can be understood if one considers the central limit theorem of statistics, which states that "if S_n is the sum of n mutually independent random variables, then the distribution function of S_n is well approximated by a certain type of continuous function known as a normal density function" [23]. This theorem is applicable to the SSTA case since the total delay is given by the sum of the delays of each stage, which are considered to be mutually independent random variables. Further, simulations on circuits from the ISCAS'85 benchmark were performed and match with the previous results and theoretical discussions. In these, the Monte Carlo simulation was also performed with 10 000 runs. A summary of the results is presented in Table II.

Two other properties of this system of sum of mutually independent random variables are presented in (2) and (3). These properties are valid no matter the shape of the pdf of the random variables

$$\mu_{s_n} = \Sigma_{i=1}^{n} \alpha_i \mu_i \tag{2}$$

$$\sigma_{s_n}^2 = \Sigma_{i=1}^{n} \alpha_i^2 \sigma_i^2. \tag{3}$$

Based on these properties, we can tell that for a long path the delay will tend to be normally distributed with its mean and variance given by (2) and (3) regardless of the shape of the individual cell delays.

SSTA tools are used for two main reasons: to look for setup and hold time violations. The most probable paths where these

violations may occur are the long paths for the setup time and the short paths for the hold time. BTI effects lead to an increased V_{th}, which leads to a larger delay in logical paths, and changes in flip flop parameters, as well as an increase in variability. The increase of the delay of the logic path increases the probability of a setup time violation and reduces the chance of a hold time violation. The change in flip-flop parameters depends on circuit topology, so we cannot present a general case of the BTI's impact on those.

For setup time violation analysis, it is important to consider the critical paths, which usually are the ones with the largest number of logic stages. Hence, one can assume that paths relevant to setup time violation analysis are going to fulfill the long path condition. When working with special designs where an SSTA analysis must be done in a short path, the linear sensitivity analysis used in the recent SSTA tools will produce unreliable results. Electrical simulations are not suited to perform statistical timing analysis at design level due to its huge computational cost. However, newly developed SSTA techniques, presented in [25] and [26], include capabilities to perform SSTA analysis for nonnormal distribution efficiently, and thus may be applied.

V. Conclusion

This paper presented a study on the utilization of SSTA tools taking BTI effects into account during the design level using standard cells technique. It was shown that in state-of-the-art technologies, where the BTI impact is larger, and for longer periods of stress time, the BTI variability becomes a dominant variability issue. For some circuit topologies, due to the nonnormal behavior of BTI, the use of standard SSTA tools may lead to misleading results. It was shown that the SSTA method simulating BTI as a time corner produces inaccurate results for short paths due to the nonnormality of the variability on the transistors threshold voltage due to BTI. Therefore for short paths, techniques which allow the SSTA tool to evaluate nonGaussian distributions with reasonable computational cost should be used. For long logic paths on the other hand, due to the central limit theorem the nonnormality loses importance and the SSTA method becomes an accurate and fast way to evaluate BTI. An analytical justification for this behavior is presented.

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