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Reliability-Based Optimization of Spin-Transfer Torque Magnetic Tunnel Junction Implication Logic Gates

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Abstract: Recently, magnetic tunnel junction (MTJ)-based implication logic gates have been proposed to realize a fundamental Boolean logic operation called material implication (IMP). For given MTJ characteristics, the IMP gate circuit parameters must be optimized to obtain the minimum IMP error probability. In this work we present the optimization method and investigate the effect of MTJ device parameters on the reliability of IMP logic gates. It is shown that the most important MTJ device parameters are the tunnel magnetoresistance (TMR) ratio and the thermal stability factor Δ. The IMP error probability decreases exponentially with increasing TMR and Δ.

Introduction

Material implication (*a* IMP *b* reads '*a* implies *b*' or 'if *a*, then *b*') [1] is one of the four fundamental Boolean logic operations like AND, OR, NOT and is equivalent to '(NOT *a*) OR *b*' as shown in Table I. However, IMP has been seldomly discussed in modern digital electronics as Shannon introduced switching algebra based on the latter three operations [2]. These operations can be easily realized using switching devices, e.g., two switches connected in parallel (series) can mimic the AND (OR) logic function and form a computationally complete logic basis needed to reproduce arbitrary Boolean functions. Recently, the realization of the IMP operation has been demonstrated [3] in a simple circuit with two TiO_2 memristors [4] and a common resistor. Using the non-volatile memristive elements as the main element for the logic computations (logic gate) intrinsically provides a non-volatile logic-in-memory architecture (called "Stateful" logic) and circumvents the leakage power issue which has become an important obstacle for scaling CMOS [5, 6, 7]. However, the TiO_2-based IMP logic requires a different fabrication platform than the existing cost-effective silicon process and provides only low operation speed.

In contrast to [3], we investigated magnetic tunnel junctions (MTJs) as the non-volatile memorizing elements to build spintronic-based IMP gates, and we proposed a new topology driven by a current source, which offers a more energy-efficient and reliable logic implementation than the standard topology with a common resistor [8, 9]. In previously proposed MTJ-based logic-in-memory architectures the MTJs are only used for storing binary data [10]; they require CMOS-based logic units and/or sensing amplifiers [11]. However, the MTJ-based implication logic uses the MTJs also as the main devices for logic computations and is suited for large-scale non-volatile logic-in-memory applications [12, 13]. Therefore, it enables intrinsic non-volatile logic circuits decreasing the device count and power consumption, and it increases logic density and operation speed simultaneously. Here we describe a reliability-based optimization scheme for the circuit and device parameters in the current-controlled IMP logic circuits.

Table I: Material implication (IMP) truth table.

a	*b*	*a* IMP *b*
0	0	1
0	1	1
1	0	0
1	1	1

MTJ-based IMP Gate

A MTJ device consists of a free ferromagnetic layer, a fixed ferromagnetic layer with pinned magnetization direction, and a non-conductive tunnel barrier separating them (Fig. 1a). The magnetization direction of the free layer can be switched freely between a parallel (P) and an antiparallel (AP) state (with respect to the magnetization direction of the pinned layer) using an external magnetic field or the spin torque transfer (STT) effect [14, 15]. The MTJ exhibits a low resistance state (LRS; R_P) across the tunnel barrier for the parallel magnetization alignment and a high-resistance state (HRS; R_{AP}) for the antiparallel alignment. The STT technique allows purely electrical reading and writing of MTJs and thus better scalability than conventional MTJs switched by a magnetic field.

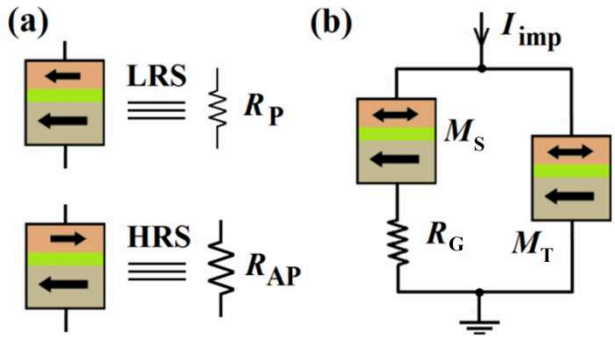

Figure 1: (a) MTJ basic structure with two magnetization states for storing binary data. (b) MTJ-based current-controlled IMP logic gate [9].

Fig. 1b shows the structure of the current-controlled IMP gate including two MTJs and a conventional resistor R_G. The initial resistance states of the target MTJ (M_T) and the source MTJ (M_S) are the logic inputs of the IMP operation (t and s in Table II) and the final resistance state of M_T after applying the current pulse I_{imp} is the logic output of the gate (t'). As shown in Table II, t and t' differ in their logic states only, when both MTJs (s and t) are initially in the high resistance state (State 1). Therefore, the current pulse I_{imp} enforces a high-to-low resistance switching only in State 1 and for any other combination of inputs the resistance states of both MTJs remains unchanged. In fact, depending on the initial resistance (logic) states of the MTJs, the IMP gate realizes a conditional switching in M_T, which is equivalent to the logic operation IMP as shown in Table I and Table II.

Table II: Truth table of the logic operation using the MTJ-based IMP logic gate.

State	s	t	t'
1	HRS≡0	HRS≡0	**LRS≡1**
2	HRS≡0	LRS≡1	LRS≡1
3	LRS≡1	HRS≡0	HRS≡0
4	LRS≡1	LRS≡1	LRS≡1

Optimization of Circuit Parameters

As mentioned before, by applying I_{imp} to the IMP gate, the logic (resistance) states of the MTJs provide a state dependent (conditional) STT switching behavior of M_T. For a reliable logic behavior with given MTJ device characteristics, the parameters I_{imp} and R_G are the two degrees of freedom for the IMP gate circuit design, which have to be optimized.

The IMP correct logic behavior is ensured only, when the gate exhibits correct logic functionality in all possible input combinations (State 1 – State 4 in Table II). In State 1 a high-to-low resistance switching is enforced on M_T, which is the desired switching event according to the IMP truth table (Table I). At the same time, as the current pulse I_{imp} tends to force an undesired

high-to-low resistance switching event in M_S, the probability of this event has also to be taken into account for the error calculation. Therefore, the error probability of the IMP operation in State 1 is given by

$$P_{err}(1) = P_S + (1 - P_T) - P_S\,(1 - P_T) = 1 - P_T + P_T\,P_S, \quad (1)$$

where P_S (P_T) is the switching probability of M_S (M_T) close to zero (one). In this state both MTJs are in the high resistance state, but due to the structural asymmetry caused by R_G, the current flowing through M_S is lower than the current required for STT switching and the majority of I_{imp} flows through M_T. Therefore, a higher R_G reduces the error probability $P_{err}(1)$ in State 1 as shown in Fig. 2, but its maximum value is limited by the required current modulation in State 3 ($P_{err}(3)$) as explained below.

In State 2 M_S (M_T) is in the high (low) resistance state. As the current direction of I_{imp} is fixed, the only possible (undesired) switching event is a high-to-low resistance switching in M_S. Therefore, the error probability is given by

$$P_{err}(2) = P_S. \quad (2)$$

As a higher R_G reduces the current through M_S, the error probability in State 2 ($P_{err}(2)$) decreases with increasing R_G as shown in Fig.2.

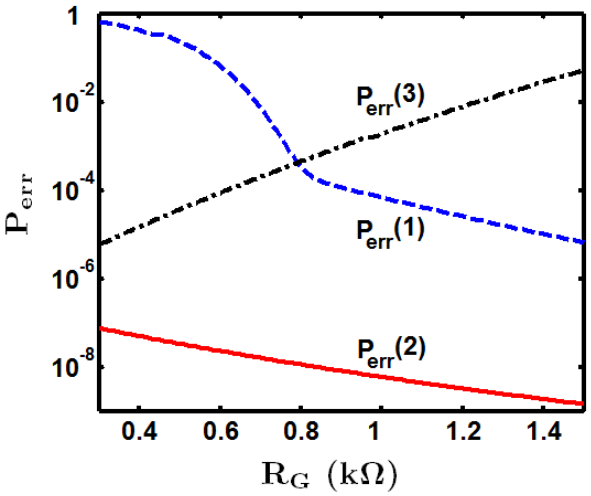

Figure 2: IMP error probabilities for different input combinations as a function of R_G.

In State 3 only M_T is in the high resistance state, while M_S is in the low resistance state. This increases the current flowing through M_S as compared to State 1, where M_S is in the high resistance state. Therefore, the current flowing through M_T is lower than the critical current required for STT switching. The error probability in State 3 is given by

$$P_{err}(3) = P_T. \quad (3)$$

Here, a higher R_G decreases the effect of the resistance modulation on M_S and thus increases the error probability as shown in Fig. 2. Hence, for a given current level of I_{imp}, an optimum R_G which minimizes the total IMP error (P_{err}) must be found. P_{err} is defined as the average of the error probabilities $P_{err}(i)$ by assuming equal probabilities for all input patterns. It should be noted that, when both MTJs are in the low resistance state (State 4), there is no undesired switching event possible, thus $P_{err}(4) = 0$. In order to obtain the error probabilities (Eq. 1 – Eq. 3), we use Eq. 4 to calculate the switching probability of the STT-MTJs in the thermally-activated switching regime (switching time t>10ns) according to the theoretical model [16] and experimental results [17]:

$$P = 1 - \exp\,\{-(t/\tau)\exp\,[-\Delta\,(1 - I_M/I_{C0})]\}, \quad (4)$$

where Δ is the MTJ thermal stability factor, t is the pulse width (50ns in our simulations), τ is 1 ns, I_{C0} is the critical switching current extrapolated to 1 ns, and I_M is the current flowing through the MTJ. In order to calculate the current through each MTJ, we use the voltage-dependent effective TMR model [18]

$$R_{AP} = [1+ \mathrm{TMR}_{eff}]\, R_P = [1+ \mathrm{TMR}/(1+ (V_M/V_0)^2)]\, R_P. \quad (5)$$

TMR_{eff} (TMR) denotes the tunnel magnetoresistance ratio under non-zero (zero) bias voltage (V_M) and V_0 is the bias voltage equivalent to TMR_{eff} = 0.5 TMR.

Fig. 3 shows the error probabilities $P_{err}(i)$ for different input states as function of I_{imp} and given R_G. I_{imp} has to be high enough to enforce a desired switching of M_T in State 1. However, there is an optimum I_{imp} as increasing I_{imp} increases the probabilities of possible undesired switching events in both M_T and M_S. Therefore, as shown in Fig. 4, the IMP gate circuit parameters I_{imp} and R_G have to be optimized for a given MTJ device characteristics. An investigation of the effect of MTJ device parameters on the IMP reliability is presented in the next section.

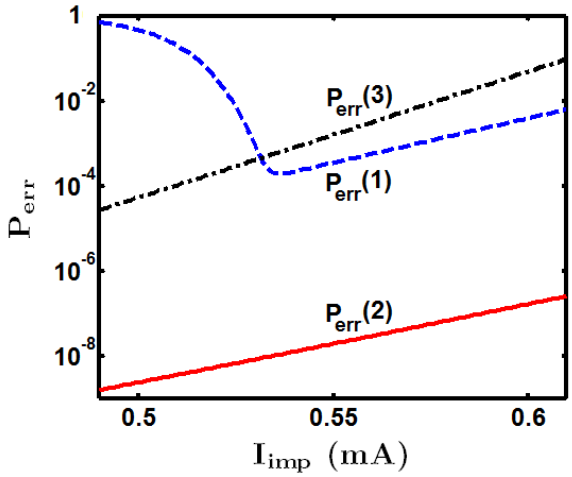

Figure 3: IMP error probabilities for different input combinations as a function of I_{imp}.

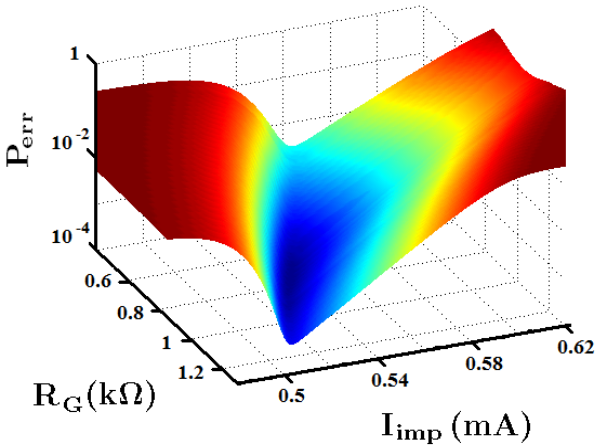

Figure 4: IMP error probability as a function of I_{imp} and R_G for plotted for MTJ devices with TMR=2.5, Δ=40, I_{C0}(AP→P) = 325 μA, and R_P =1.8 kΩ.

MTJ Device Parameters' Effect on the IMP Reliability

In order to investigate the effect of MTJ device parameters on the IMP reliability, we use the circuit optimization method presented in the previous section to determine the minimum IMP gate error probability for given MTJ device parameters.

As mentioned before, a higher R_G reduces the error probabilities in State 1 and State 2 but is limited by the required current modulation in State 3 (Fig. 2). The current modulation in State 3

relies on the modulation of the MTJ resistance between its antiparallel and parallel magnetization states and is described by the TMR ratio according to Eq. 5. From this follows that the TMR ratio is the main device parameter affecting the reliability of the IMP gate. A higher TMR ratio provides a higher current modulation and allows higher values of R_G for IMP circuit parameters design. Fig. 5 shows the two dominant IMP error probabilities ($P_{err}(1)$ and $P_{err}(3)$) for two different values of TMR. It illustrates that a higher TMR has a negligible effect on $P_{err}(1)$ but it decreases $P_{err}(3)$. Therefore, for MTJs with higher TMR, the IMP gate with optimized circuit parameters exhibits a more reliable logic behavior as shown in Fig. 6. Fig. 6a illustrates the minimum IMP error as a function of the TMR ratio for optimized circuit parameters. The corresponding optimum values of I_{imp} and R_G are depicted in Fig. 6b.

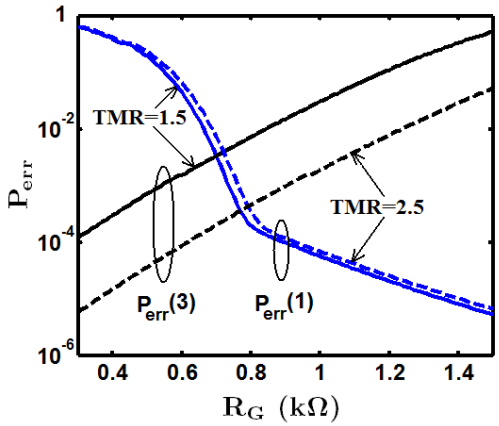

Figure 5: The dominant error probabilities (P_{err} in State 1 and State 3) for two different values of TMR.

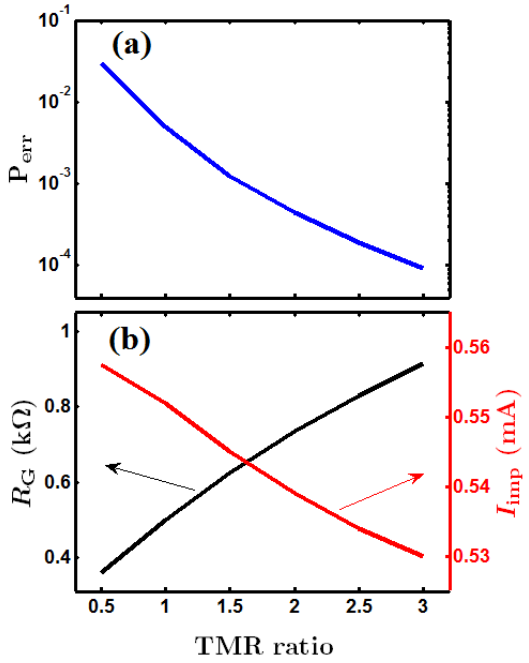

Figure 6: (a) IMP error probability as a function of TMR ratio for Δ=40 with optimized circuit parameters. (b) Optimum circuit parameters corresponding to minimum IMP error as a function of TMR ratio plotted for MTJ devices characterized as $I_{C0}(AP\rightarrow P)$ = 325 μA and R_P =1.8 kΩ.

As stated before, the TMR ratio is the main device parameter for the IMP gate reliability analysis, but it is not the only MTJ device parameter which affects the IMP error probability. According to Eq. 4, the dominant term for the switching probability calculation is $[-\Delta\ (1- I_M/ I_{C0})]$ in which the modulation of (I_M/ I_{C0}) depends on the TMR ratio value. A higher TMR allows a higher modulation and thus a lower IMP error probability. However, a higher Δ enlarges the effect of this modulation in the dominant term of Eq. 4. Therefore, a higher Δ decreases the error probabilities for a given TMR ratio as shown in Fig. 7.

Due to the normalization of the currents and the resistances to the parameters I_{C0} and R_P, the results are independent of the absolute values of these two MTJ device parameters. For instance, if the MTJs cross-sectional area is increased by a factor of 2, the MTJ parameter I_{C0} increases by a factor of 2 while R_P decreases by 50%. Since in the calculations, I_{imp} (R_G) is normalized by I_{C0} (R_P), its optimum value corresponding to the minimum IMP error will increase (decreases) by a factor of 2 (50%). This exactly compensates the respective changes and the IMP error remains unchanged. Furthermore, our results show that, for a two orders of magnitude increment in the I_{imp} pulse duration (the MTJ switching time t in Eq. 4), the IMP error probability increases by a factor of 2. Therefore, the effect of the MTJ switching time is negligible as compared to the TMR and Δ. This can be explained using Eq. 4 as the effect of t is much smaller compared to the internal exponential term.

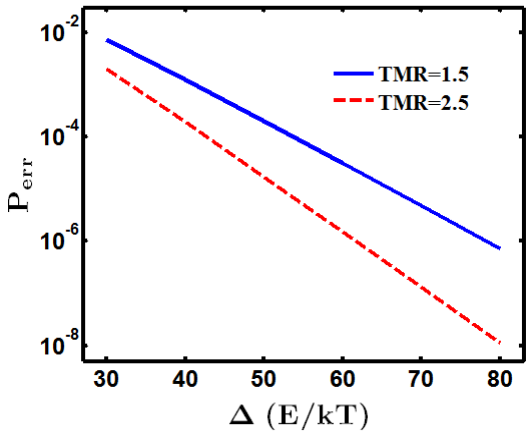

Figure 7: IMP error probability as a function of Δ for two different TMR values and optimized circuit parameters at each point.

Summary

An optimization procedure of the current driven IMP gate reliability operation is presented. For given MTJ characteristics, the IMP gate circuit parameters have to be optimized in order to obtain the minimum IMP error probability. The dominant MTJ device parameters determining the error probability of the IMP gate are TMR and Δ. It is shown that the IMP error probability decreases exponentially with both TMR and Δ parameter values increased.

Acknowledgment

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