NBTI Reliability of SiGe and Ge Channel pMOSFETs With SiO_2/HfO_2 Dielectric Stack

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(Invited Paper)

***Abstract*—Due to a significantly reduced negative-bias temperature instability (NBTI), (Si)Ge channel pMOSFETs are shown to offer sufficient reliability at ultrathin equivalent oxide thickness. The intrinsically superior NBTI robustness of the MOS system consisting of a Ge-based channel and a SiO_2/HfO_2 dielectric stack is ascribed to a reduced availability of interface precursor defects and to a significantly reduced interaction of channel carriers with gate dielectric defects due to a favorable energy decoupling. Owing to this effect, a significantly reduced time-dependent variability of nanoscale devices is also observed. The superior reliability is shown to be process and architecture independent by comparing both our results on a variety of Ge-based device families and published data of other groups.**

***Index Terms*—Ge, NBTI, pMOSFET, reliability, SiGe.**

I. Introduction

DUE to the ever increasing electric fields in scaled CMOS devices, reliability is becoming a showstopper for upcoming technology nodes. Although several groups have already demonstrated functional Si devices with aggressively scaled EOT down to $\sim$5 Å [1], [2], the stability of their parameters at operating conditions cannot be guaranteed [3], [4]. Meanwhile, the use of high-mobility channels is being considered for further device performance enhancement in future CMOS technology nodes [5], [6]. The SiGe or Ge channel quantum-well (QW) technology (Fig. 1) in particular is considered for yielding enhanced mobility and pMOS threshold voltage tuning [7], [8].

While the interface passivation of non-Si channel materials is typically considered a challenging and critical issue, extremely promising device performance was recently obtained by growing epitaxially a thin Si passivation layer (Si cap) on top of a pMOS (Si)Ge channel [5], [9]. This approach allows also for the use of a standard high-k/metal gate stack consisting of a SiO_2 interfacial layer grown by oxidation of the Si cap and a HfO_2 layer. However, open questions existed about the reliability of such complex gate stacks.

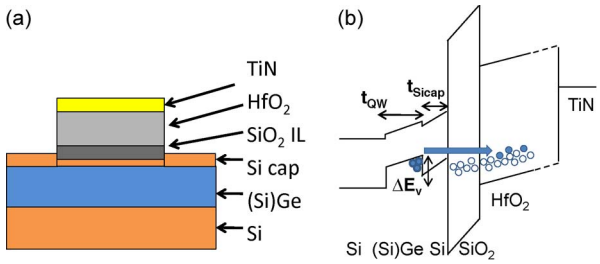

Fig. 1. (a) Gate stack of (Si)Ge devices used in this work. (b) Band diagram sketch in inversion. Channel holes are confined into the (Si)Ge QW due to the valence band offset (ΔE_v) between the (Si)Ge channel and the Si cap. The Si cap thickness (t_{Sicap}) therefore contributes to the T_{inv} of the gate stack.

In this paper, we review our recent studies [10]–[16] regarding the NBTI reliability [17], [18] of Ge-based pMOSFETs with SiO_2/HfO_2 dielectric stack. We show that this technology offers a significant intrinsic reliability improvement which we ascribe chiefly to a reduced interaction between channel carriers and oxide defects. The superior NBTI reliability is shown to be process- and architecture-independent, by comparing our data on a variety of Ge-based device families with published data of other institutions. Furthermore, we show that the (Si)Ge-based technology also significantly alleviates the time-dependent variability [19], [20], which arises as devices scale toward atomistic dimensions [21]. The extensive experimental results summarized here strongly support (Si)Ge pMOS technology as a clear frontrunner for future CMOS technology nodes.

The paper is organized as follows: in Section II, the devices and the experimental methodology used in this work are described. In Section III, the impact of the main (Si)Ge device process parameters on NBTI is assessed, and a gate stack optimization for sufficient device reliability at ultra-thin EOTs is proposed. The NBTI kinetics in SiGe devices is discussed in detail and compared with standard Si devices in Section IV, while in Section V a model for the superior NBTI robustness is proposed. In Section VI we compare NBTI data of a variety of Ge-based device families with SiO_2/HfO_2 dielectric stacks with published data of other groups, showing the superior

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reliability to be process- and architecture-independent. In Section VII we discuss how the reduced NBTI projects to a dramatically reduced time-dependent variability of nanoscale (Si)Ge devices. Finally, in Section VIII we discuss the impact of the proposed reliability-oriented (Si)Ge gate stack optimization on the device performance. The main conclusions are summarized in Section IX.

II. Device Description

A sketch of SiGe device gate stack and its band diagram in inversion are depicted in Fig. 1. The channel layer consists of an epitaxially grown compressively strained thin $Si_{1-x}Ge_x$ layer, with thickness varying between 3 nm and 7 nm. Ge fractions up to $x = 0.55$ were used. Devices with relaxed- and strained-Ge channel (i.e., $x = 1$) were also considered. On top of the $Si_{1-x}Ge_x$ layer, a thin undoped Si cap was grown epitaxially, in order to passivate the surface and allow the use of a conventional SiO_2/HfO_2 dielectric stack. The physical thicknesses of this thin Si cap varied between 0.65 nm and 2 nm (as estimated from C–V curves and TEM pictures of the final device). A detailed description of the epi-process can be found elsewhere [22]. Gate stack fabrication started with a wet chemical oxidation (*IMEC clean* [23]) of the Si cap. On top of the obtained SiO_2 interfacial layer (IL), a $\sim$1.8 nm thick HfO_2 layer was deposited by ALD. Finally, a PVD TiN metal gate was deposited. The metal gate thickness controlled the final IL thickness by means of the oxygen scavenging technique, as discussed in [1]. The mobility enhancement factor of SiGe devices w.r.t. Si ranged between 1.5x and 2.4x, depending on the gate-stack parameters [6], [9]. For comparison, a second set of standard Si channel devices with an identical gate stack was also used.

Due to the valence band offset between the (Si)Ge and the Si cap [see Fig. 1(b)] inversion holes are confined in the high-mobility channel layer, which therefore acts as a quantum well (QW). The Si cap results in lower inversion capacitance as compared to the accumulation capacitance [10]. For a fair benchmarking of these devices it is therefore necessary to consider the capacitance-equivalent thickness (CET) in inversion ($T_{\rm inv}$, evaluated at $V_G = V_{\rm th} - 0.6$ V) which includes the contribution of the Si caps of varying thicknesses.

NBTI stress experiments were performed using the extended measure-stress-measure technique [24]. The devices were stressed at $T = 125$ °C with several gate overdrives, while the sensing bias was $V_G = V_{\rm th0}$. To minimize NBTI relaxation effects for the device lifetime predictions, $\Delta V_{\rm th}$ was evaluated at $t_{\rm relax} = 1$ ms. For each gate voltage the stress time needed to reach a failure criterion, assumed as 30 mV threshold voltage shift, was extracted. The 10 years lifetime operating overdrive ($V_{\rm op}$) was then extrapolated by fitting a power law to the lifetime vs. gate overdrive data sets (see Fig. 2).

III. Experimental Results

Fig. 2 reports the individual impact of three major process parameters of the (Si)Ge pMOSFETs, i.e., the Ge fraction, the SiGe layer thickness, and the Si cap thickness, on the NBTI reliability. As shown in Fig. 2(a), the introduction of Ge in the channel significantly improved the NBTI reliability, with higher Ge fraction boosting the $V_{\rm op}$. Increasing the thickness of the SiGe QW from 3 nm to 7 nm gave an additional improvement of the NBTI reliability [Fig. 2(b)]. The most significant impact on the NBTI reliability was observed when varying the Si cap thickness [Fig. 2(c)]. Interestingly, a reduced thickness of this layer clearly improved the NBTI robustness. Naively one would expect the thinner Si cap to act as a reduced tunneling barrier for holes, but conversely $V_{\rm op}$ increased as the Si cap thickness was decreased from 2 nm to 0.65 nm. This counter-intuitive observation is crucial for understanding the superior NBTI reliability of the MOS consisting of a Ge-based channel and a SiO_2/HfO_2 dielectric stack, as we will discuss in Section V. Moreover, the observation is particularly relevant since a reduced Si cap thickness, while improving the NBTI reliability, also reduces the device $T_{\rm inv}$ [thanks to reduced hole spatial displacement, see Fig. 1(b)] and therefore enhances the current drive performance.

The $V_{\rm op}$ extracted for different Si cap thicknesses are shown in a benchmark plot vs. the $T_{\rm inv}$ values (Fig. 3) and compared

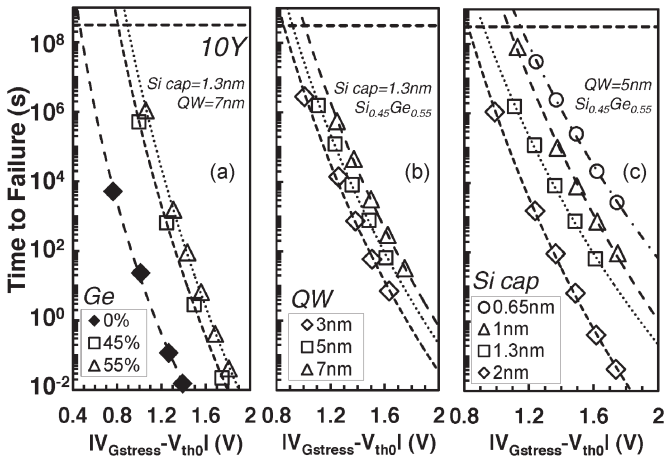

Fig. 2. Extrapolated lifetimes as a function of gate voltage overdrive for varying (a) Ge content, (b) QW thickness, (c) Si cap thickness. The NBTI robustness is boosted by increasing the Ge fraction, increasing the QW thickness and reducing the Si cap thickness. Note that a reduced Si cap thickness also enables $T_{\rm inv}$ reduction. The extrapolated $V_{\rm op}$ values are plotted in Fig. 3 for fair benchmarking vs. $T_{\rm inv}$.

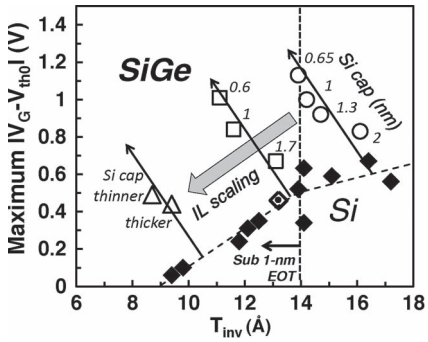

Fig. 3. Maximum operating overdrive for 10 years lifetime ($T = 125$ °C, failure criterion $\Delta V_{\rm th} = 30$ mV) vs. $T_{\rm inv}$ (evaluated at $V_G = V_{\rm th} - 0.6$ V). SiGe devices with a thin Si cap offer improved NBTI reliability, i.e., higher $V_{\rm op}$. The observation is consistently reproduced for three different SiO_2 IL thicknesses, obtained with the O-scavenging technique [1]. Note: the open-diamond and the circles represent the Si ref. gate stack of Fig. 2(a) and the SiGe gate stacks of Fig. 2(c), respectively; the solid diamonds represent Si benchmark data from [4].

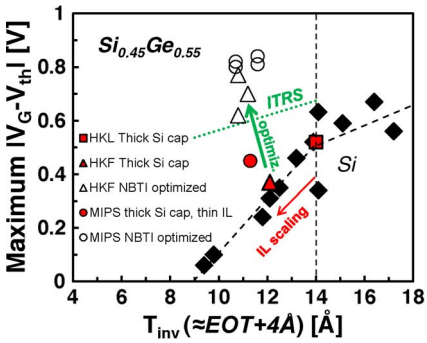

Fig. 4. A high Ge fraction (55%) in a 6.5 nm thick QW, combined with a thin Si cap (0.8 nm) boost $V_{\rm op}$ to meet the target $V_{\rm DD}$ at ultra-thin EOT in a gate-first Metal Inserted Poly-Silicon (MIPS) flow (open circles, as compared to solid circle). The optimization was also implemented in a gate-last Replacement Metal Gate (RMG) flow: high-k last (HKL) SiGe sample with thick Si cap (square) shows poor NBTI robustness; an IL reduction by means of O-scavenging in a high-k first (HKF) process flow (solid triangle), further reduces NBTI robustness; however, the SiGe gate-stack optimization (open triangles) boosts the $V_{\rm op}$ above the ITRS target [25]. The results were reproduced for several process thermal budgets.

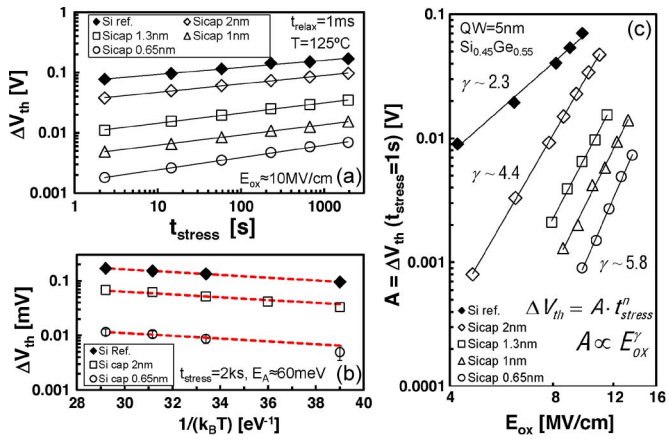

Fig. 5. (a) Measured $\Delta V_{\rm th}$ during NBTI stress at fixed stress conditions on a Si Ref. and on SiGe devices with different Si cap thicknesses. The SiGe device with the thinnest Si cap shows most reduced $V_{\rm th}$ instability. (b) $\Delta V_{\rm th}$ measured at different temperatures on the Si ref. devices, and on SiGe devices with two different Si cap thicknesses (2 nm and 0.65 nm). No clear difference in the apparent $\Delta V_{\rm th}$-activation energy is observed (extracted $E_A \approx 60$ meV). (c) Extracted NBTI $\Delta V_{\rm th}$ power-law pre-factors A: a significant reduction for the SiGe devices is observed, especially with a reduced Si cap thickness. A stronger $E_{\rm ox}$-acceleration for SiGe w.r.t. the Si ref. device is also noted.

with benchmark data measured on Si channel pMOSFETs. As one can see, it is clear that reducing the Si cap thickness yields a significant $V_{\rm op}$ boost together with a $T_{\rm inv}$ reduction. Such a $V_{\rm op}$ boost for reduced Si cap thickness was observed consistently for several IL thicknesses. This trend is clearly opposite to the data collected on Si channel devices where a $T_{\rm inv}$ reduction (normally achieved by IL scaling) is always associated with a reliability reduction, as also shown in Fig. 3.

This remarkable property can be used to optimize the SiGe gate-stack and salvage the NBTI reliability of devices with aggressively scaled IL. Fig. 4 reports that combining the beneficial effects of a *high Ge fraction, a thicker QW* and *a thinner Si cap*, the NBTI lifetime was boosted above the ITRS [25] target $V_{\rm DD}$ condition at ultra-thin EOT (10 years continuous operation at $|V_G - V_{\rm th}| \approx 0.6$ V at $T_{\rm inv} \approx 1$ nm, EOT ≈ 0.6 nm). We note that other device degradation mechanisms as Channel Hot Carrier and Time-Dependent Dielectric Breakdown do not represent a concern for this NBTI-optimized SiGe gate stack, as we observed in [16].

IV. NBTI Kinetics in (Si)Ge

In this Section the NBTI kinetics on (Si)Ge devices is discussed and compared to Si reference devices, highlighting similarities and differences. Fig. 5(a) shows the typical NBTI $\Delta V_{\rm th}$ evolution vs. the stress time for the Si ref. and the SiGe devices with different Si caps. The NBTI $\Delta V_{\rm th}$ evolution is often described as a power law of the stress time ($\Delta V_{\rm th} = At_{\rm stress}^n$), with a pre-factor A dependent on the stress $E_{\rm ox}$, and an apparent exponent n typically reported in the range of 0.15 to 0.25 [17] depending on the relaxation allowed by the measurement delay [24]. While no significant difference is observable in the NBTI kinetics (similar time exponents [15]), the SiGe devices show a significantly reduced $\Delta V_{\rm th}$, especially for the samples with reduced Si cap thickness. No significant difference between Si and SiGe devices is also observed in the temperature dependence of NBTI [Fig. 5(b)], with a typical *apparent* activation energy $E_A \sim 60$ meV [27].

A significant difference is observed instead in the field-dependence. Fig. 5(c) shows the NBTI power law prefactors A [i.e., $\Delta V_{\rm th}(t_{\rm stress} = 1\ {\rm s})$]. The prefactors clearly show a dramatic reduction for the SiGe devices, with a further reduction for a decreasing Si cap thickness. Moreover, a significantly stronger $E_{\rm ox}$-acceleration for SiGe w.r.t. the Si ref. is clearly observed, resulting in further benefit at the lower operating fields. This higher field-dependence is another crucial aspect to understand the superior reliability of (Si)Ge technology, as discussed in Section V.

NBTI is often ascribed to two components [26], [27]: a recoverable (R) one related to hole trapping in pre-existing bulk oxide defects ($\Delta N_{\rm ot}$), and a so-called permanent one (P) typically associated with creation of new interfaces states ($\Delta N_{\rm it}$). To get insights into the measured NBTI trends, the charge pumping (CP) technique [28] was used to monitor the interface state creation during the NBTI stress. While $\Delta N_{\rm it}$ was monitored by CP, $\Delta N_{\rm ot}$ was calculated by subtracting the $\Delta N_{\rm it}$ contribution from the total $\Delta V_{\rm th}$ measured. Fig. 6 reports $\Delta N_{\rm it}$ and $\Delta N_{\rm ot}$ evolutions measured on SiGe devices with two different Si cap thicknesses and on the Si ref. device for fixed stress conditions ($E_{\rm ox} = 10$ MV/cm, $T = 125$ °C). The SiGe device with a thin Si cap shows reduced both R and P, with the reduction in R being of higher relevance, since R contributes most to the total $\Delta V_{\rm th}$ measured at short $t_{\rm stress}$ [cf. y-axis of Fig. 6(a) and (b)]. Interestingly, $\Delta N_{\rm it}$ follows a power law with stress time with the same exponent of ~0.25 for the Si and for SiGe devices with different Si caps, suggesting the same interface bond breaking process. This conclusion is also supported by the P component showing the same dependence on the stress electric field for the SiGe and Si reference devices, as illustrated in Fig. 7.

The above discussed experimental observations on SiGe devices with reduced Si cap thickness can be summarized as:

1) Similar $\Delta V_{\rm th}$ kinetics;

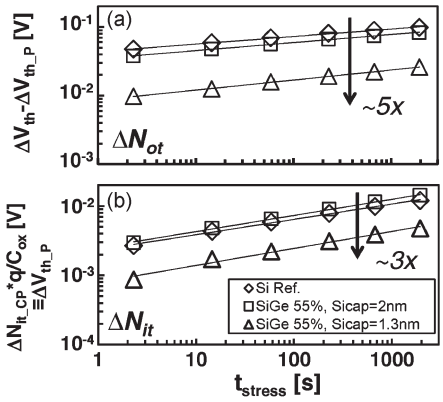

Fig. 6. Total $\Delta V_{\rm th}$ split into (a) the so-called recoverable component of NBTI (R), assumed to be caused by filling of pre-existing oxide traps $(N_{\rm ot})$, and (b) the so-called permanent component (P), assumed to be caused by $\Delta N_{\rm it}$. $\Delta N_{\rm it}$ measured with charge pumping during NBTI stress were converted to $\Delta V_{\rm th\_Permanent} (= \Delta N_{\rm it}.q/C_{\rm ox})$ in order to decouple their contribution from the total measured $\Delta V_{\rm th}$. $\Delta N_{\rm it}$ follows a power law on the stress time with the same exponent (∼0.25) on all three samples. However SiGe devices with thinner Si cap show both reduced P and R, with the reduction of R having a higher impact on the total $\Delta V_{\rm th}$ since R contributes most of the measured $\Delta V_{\rm th}$ [cf. the y-axis ranges of (a) and (b)].

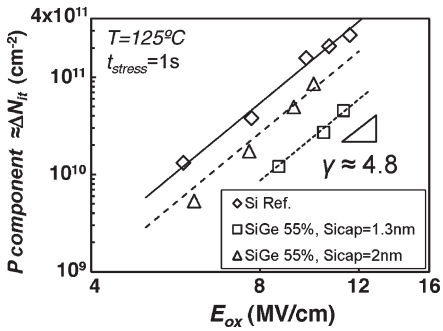

Fig. 7. The P component $(\sim \Delta N_{\rm it})$ extracted with the universal relaxation methodology [24], [26] and plotted vs. the stress electric field $(E_{\rm ox})$ for the Si reference device and SiGe devices with two different Si cap thicknesses (2 nm and 1.3 nm). A reduced P component is observed for the SiGe device with a thinner Si cap, while the similar $E_{\rm ox}$-dependence suggests the same interface bond breaking process taking place as in the Si device.

2) Similar apparent temperature activation $(E_A \approx 60$ meV) as Si ref.;
3) Reduced NBTI, i.e., lower power-law pre-factor;
4) Stronger $E_{\rm ox}$-acceleration;
5) Similar $\Delta N_{\rm it}$ time exponent and field-dependence as Si;
6) Significantly reduced $\Delta N_{\rm it}$ and $\Delta N_{\rm ot}$, with the latter reduction being of greater relevance.

V. Model

The observations related to the generation of interface states [i.e., same time dependence, cf. Fig. 6(b); same voltage dependence, cf. Fig. 7; same apparent activation energy of total $\Delta V_{\rm th}$, cf. Fig. 5(b)] suggest that the same bond breaking process at the Si/SiO_2 interface, i.e., the de-passivation of H-passivated Si dangling bonds (Pb_0), is likely to be taking place also in (Si)Ge devices. We have previously reported [12] Electron Spin Resonance Spectroscopy (ESR) [29] measurements on a Ge substrate with a thick Si cap which revealed a high Pb_0 density

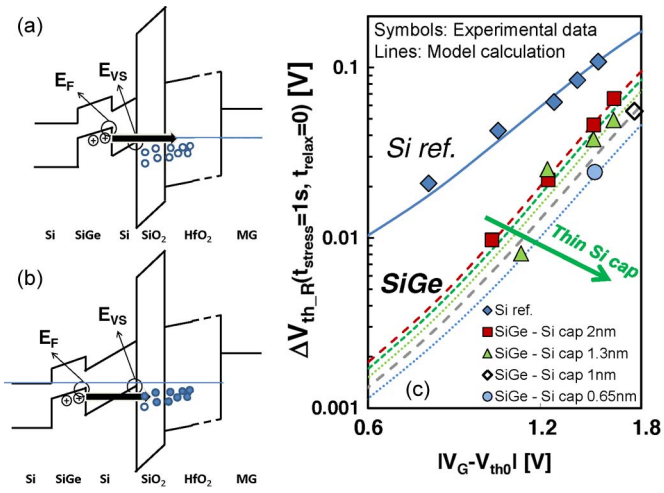

Fig. 8. A model including defect bands in the SiO_2 IL and in the HfO_2. (a) Fewer defects are energetically favorable for trapping channel holes thanks to the higher Fermi level in SiGe as compared to Si. (b) The additional voltage drop on a thicker Si cap 'pushes' down the Fermi level in the channel (when benchmarking at constant electric field or constant gate overdrive) and therefore more oxide defects become energetically favorable for hole trapping. (c) Calculated $\Delta V_{\rm th}$ vs. experimental data of the recoverable component. The model was first calibrated on the Si reference data, then the same defect band parameters were used to calculate the expected $\Delta V_{\rm th}$ for SiGe devices (including the valence band offset between the SiGe and the Si cap, and the voltage drop on Si caps of varying thickness). The simple model matches the experimental data remarkably well.

$(\sim 1 \times 10^{12}$ cm$^{-2})$, while these defects could not be detected $(< 10^{11}$ cm$^{-2})$ on a very thin Si cap. This observation suggests that the Ge segregation at the Si/SiO_2 interface reported for Ge-based channels and enhanced by the use of a Si cap with reduced Si cap thickness [30] can reduce the $N_{\rm it}$ precursor defect density (Si-H bonds) and therefore the $\Delta N_{\rm it}$ during NBTI stress. We note, however, that the enhanced presence of Ge atoms at the Si/SiO_2 interface is likely to induce additional electrically active interface states, thereby reducing the degree of interface passivation of the unstressed device. This might result in a trade-off between initial device performance and reliability, as discussed later on in Section VIII [cf. Fig. 16(a)].

However, while this reduced creation of interface states certainly plays a role in the improved NBTI reliability observed for (Si)Ge channel devices, it cannot completely explain the strongly reduced overall NBTI degradation which is mainly caused by a significant reduction of the hole trapping component ($\Delta N_{\rm ot}$, cf. Fig. 6). We suggest that the $\Delta N_{\rm ot}$ reduction is related to a favorable alignment shift of the Fermi level in the SiGe channel with respect to the pre-existing bulk oxide defect energy levels [Fig. 8(a)]. Larger misalignment can cause carriers to interact with a smaller fraction of accessible oxide traps. We note that the carrier energy alignment to a defect level has been often invoked to explain Positive BTI mechanisms in high-k/Metal Gate nMOS devices [31]–[33]. To model this effect, we assume the existence of defect bands both in the SiO_2 IL and in the high-k layer. We note that the interacting defects might be located in both dielectric layers since the same NBTI trends on SiGe with different Si caps were consistently observed when scaling the IL thickness (cf. Fig. 3). As depicted in Fig. 8(a), the Fermi level in the channel determines which part of the defect band is accessible to channel holes. Thanks

to the band alignment of the (Si)Ge channel toward the gate stack, fewer defects are energetically favorable for channel holes. However, the additional voltage drop over a thicker Si cap (when benchmarking at fixed gate overdrive voltage or at fixed equivalent oxide electric field, as customary for NBTI studies), 'pushes' the channel hole energy level down and therefore more defects become energetically favorable for charging [Fig. 8(b)].

We implemented this model concept by representing the defect bands as Gaussian distributions over energy in order to calculate the induced $\Delta V_{\rm th}$ caused by accessible defects for different gate stacks and as a function of the applied gate overdrive voltage. The mean values of the distributions were pinned at 0.95 eV below the Si valence band for the IL (corresponding to the $E'_\gamma[E_{0/+}]$ center in SiO_2 [34]) and at 1.4 eV below the Si valence band for the high-k (corresponding to the neutral oxygen vacancy $[O_o]$ level in HfO_2 [35]). All the defects located above the channel Fermi level are considered occupied by trapped holes, while all the defects below are neutral. (Note: no trapping/de-trapping kinetics are included in this calculation, i.e., the thermodynamic equilibrium is represented.) The model was first calibrated using the NBTI data on the Si reference devices: the standard deviations of the Gaussian distributions were used as a fitting parameter (in the range of $0.3 \sim 0.5$ eV) in order to capture the correct electric field dependence, while the defect densities were fitted in order to match the observed $\Delta V_{\rm th}$ magnitude. The scaled $\Delta V_{\rm th}$ contribution of defects located at varying depths due to their electrostatic effect was also included. Then, with the same defect band parameters, the expected $\Delta V_{\rm th}$ was calculated for SiGe channel devices, including the valence band offset of $+0.35$ eV in the channel and including the varying voltage drop on Si cap with varying thicknesses.

As shown in Fig. 8(c) the simple model matches excellently the experimental recoverable component $(\Delta N_{\rm ot})$ of NBTI. Both the reduced degradation and the stronger field dependence observed for SiGe devices with reduced Si cap thicknesses are readily captured.

The model explains also the other experimental observations previously made concerning the Ge fraction and the quantum well thickness. In order to minimize the fraction of accessible defects, i.e., in order to 'push up' the Fermi level in the channel with respect to the defect band, the valence band offset between SiGe and Si has to be maximized—higher Ge fraction (reduced bandgap and higher ΔE_v) and thick quantum well (to reduce quantization [36]) are therefore beneficial. Moreover, this model explains the distinct relation between the fresh device $V_{\rm th0}$ and the NBTI observed in SiGe devices with varying process parameters [Fig. 9(a)]: as calculated with MEDICI for, e.g., a Si cap thickness split, gate-stacks with lower $|V_{\rm th0}|$ have higher channel Fermi level energy [Fig. 9(b)] and therefore benefit from the reduced interaction between holes and oxide defects.

We note that the proposed representation of the defect levels as Gaussian distributions is a mere assumption serving the sole purpose of simplifying the mathematical treatment of the model. Different energy distributions of the defects in the dielectric layer might exist in reality. Nevertheless, a similar

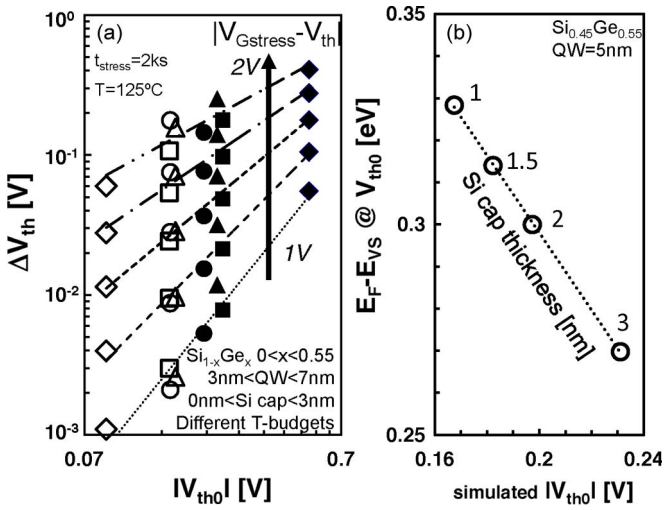

Fig. 9. A clear correlation between the initial $V_{\rm th0}$ and NBTI-induced $\Delta V_{\rm th}$ is consistently observed on SiGe devices with different process parameters: devices with lower initial $V_{\rm th0}$ always showed reduced $V_{\rm th}$-instability, at any given stress condition $(|V_{\rm Gstress} - V_{\rm th0}|)$. This is typically not observed for Si devices when benchmarking NBTI as a function of the overdrive voltage. (b) A lower device $V_{\rm th0}$ corresponds to a higher channel Fermi level energy (E_F) with respect to the Si valence band $(E_{\rm VS})$, as shown with MEDICI simulations. The higher Fermi level in the channel is beneficial for reducing the carrier-trap interaction, according to the model proposed here (cf. Fig. 8).

beneficial effect by shifting up the Fermi level energy in the channel would hold for a very general class of defect level distributions [e.g., even for a uniform energy distribution of defect levels, a fraction of defects would become unfavorable for holes at the (Si)Ge channel Fermi level]. We also note that an additional contribution to the enhanced NBTI for gate stack with thicker Si caps could be related to a spill-over of inversion holes into the cap at high oxide fields. According to the proposed model, holes at the valence band of the Si cap would be favorably trapped in the dielectric defects and therefore the benefit of using a Ge-based channel would be partially lost.

Finally we highlight that the experimental observations and the proposed model would suggest maximized reliability for SiGe devices without a Si cap (i.e., *maximum energy shift*). Indeed we have shown in [15] very good reliability for SiGe devices with low Ge fraction (25% and 45%) and without a Si cap (i.e., direct oxidation of the SiGe surface). However the use of a thin Si cap is an integration scheme necessary to obtain sufficient interface quality and mobility in SiGe devices with Ge fraction $> 45\%$ [9], as discussed in Section VIII.

VI. Process- and Architecture-Independent Results

As shown in Fig. 4, the proposed (Si)Ge gate stack optimization with a high Ge fraction, a thick QW and a reduced Si cap thickness was demonstrated to boost NBTI reliability both in a Metal-Inserted Poly-Si (MIPS) and a Replacement Metal Gate (RMG) process flow, with reproducible results for different thermal budgets. These process-independent results already suggest the reliability improvement to be an intrinsic property of this device family.

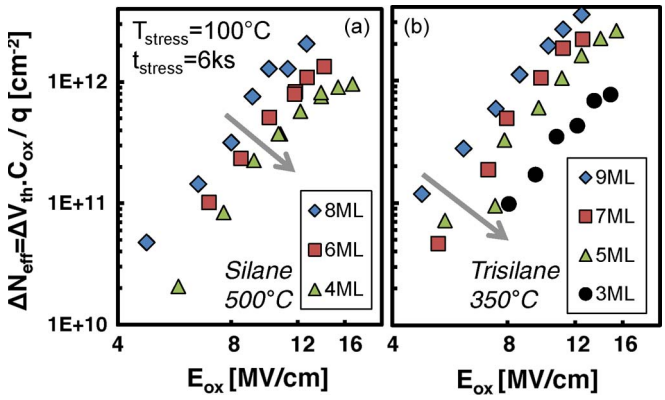

Fig. 10. A decreased thickness of the Si passivation layer improves the NBTI robustness of relaxed-Ge pMOSFETs, independently of the Si cap epi-process used, (a) silane 500 °C, or (b) trisilane 350 °C.

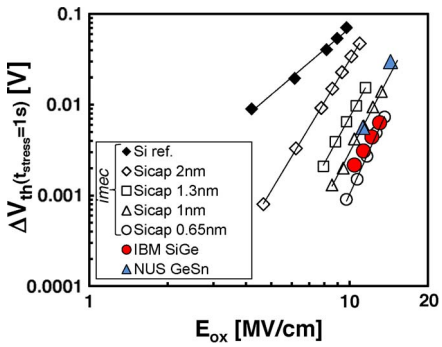

Fig. 11. Re-plotted NBTI data published by IBM [7] for SiGe pMOSFETs and by NUS [37] for GeSn pMOSFETs with SiO_2/HfO_2 dielectric stack compare well with the data shown already in Fig. 5(c) for SiGe devices with reduced Si cap thickness. Note the confirmed key signature of the higher field acceleration as compared to Si ref. devices. (In order to estimate $E_{\rm ox}$ from published data plotted vs. $V_{\rm ov}$. the $T_{\rm inv}$ value for the IBM 32 nm was taken from [38]).

Moreover, the experiment with varying Si cap thickness was repeated on pure Ge channel pMOSFETs with 4, 6, and 8 Si mono-layers (ML) epi-grown from silane precursor at 500 °C. A reduced thickness of the Si-layer again resulted in a reduced NBTI at fixed stress conditions (electric field, stress time, stress temperature, sensing delay): 4 MLs devices degrade $\sim 4\times$ less than 8 MLs devices [Fig. 10(a)]. The same trend was also observed for Si-caps grown using a 350 °C epi-growth from trisilane precursor: a $\sim 8\times$ NBTI reduction is observed when reducing the Si from 9 to 3MLs [Fig. 10(b)], suggesting the result to be independent also of the precursor used for the Si passivation.

Other groups have recently confirmed improved NBTI reliability of similar MOS systems consisting of a Ge-based channel and SiO_2/HfO_2 gate stack: interestingly the key signature of the stronger field-acceleration w.r.t. Si devices can be found in the data recently published by IBM for SiGe channel pMOSFET [7] and by the National University of Singapore (NUS) for GeSn channel pMOSFETs [37] (Fig. 11). The maximum operating overdrive voltages for these devices extrapolated from published data are plotted in Fig. 12 together with several Ge-based IMEC devices. As can be seen, the IBM SiGe data compare very well with our data for SiGe devices with a reduced Si cap thicknesses. The NUS GeSn also show a similar

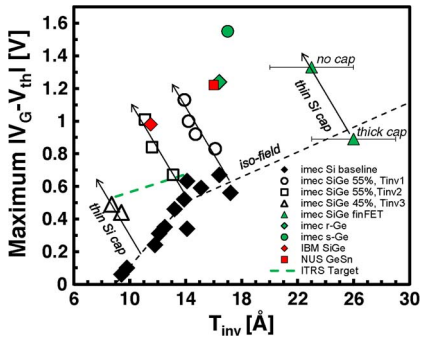

Fig. 12. Benchmark plot of the maximum operating overdrive for several Ge-based channel device families with SiO_2/HfO_2 dielectric stack, including SiGe devices with varying Si cap and IL thicknesses already shown in Fig. 3. The IBM SiGe channel 32 nm technology [7] well compares with the IMEC planar SiGe channel with reduced Si cap thickness (Note: IBM data were rescaled from a failure criterion of $\Delta V_{\rm th} = 50$ mV to our failure criterion of $\Delta V_{\rm th} = 30$ mV to allow cross-comparison). NUS GeSn devices [37] also show similar $V_{\rm op}$, which well compares with IMEC relaxed-Ge. Further reliability improvement is obtained in strained-Ge channel devices [39], thanks to additional valence band offset [40]. Wrapped SiGe channel pFinFETs also show improved reliability when a thick Si cap is not used [13].

$V_{\rm op}$, which favorably compares with relaxed-Ge IMEC data. While the epitaxial growth of a *pure* Ge channel on a Si wafer typically yields a relaxed layer due to the excessive lattice mismatch, strained-Ge devices can be fabricated by growing a *pure* Ge channel layer on a SiGe strain-relaxed buffer. We have recently shown [39] that further reliability improvement can be obtained with this structure (see solid circle in Fig. 12) since a larger valence band offset is obtained for increasing strain [40].

Finally the improved reliability is observed to be also architecture-independent: preliminary results on novel SiGe wrapped-channel bulk pFinFETs [41] show improved NBTI lifetime w.r.t. Si planar ref. when removing the Si cap (see green triangles in Fig. 12).

All these process- and architecture-independent results suggest that *the reduced NBTI is an intrinsic property of the MOS system consisting of a Ge-based channel and a* SiO_2/HfO_2 *dielectric stack*, further emphasizing its potential use in future CMOS technology nodes.

VII. Time-Dependent Variability

With ever decreasing device size, the number of dopant atoms, but also the number of defects, in each device reduces to numerable levels [21]. This results in increased time-zero (i.e., as-fabricated) variability, but also considerable time-dependent variability (i.e., reduced reliability) [19], [20]. We and others have recently shown that the properties of individual charged gate oxide defects can be observed in the NBTI $\Delta V_{\rm th}$ relaxation transients [20]. A representative set of typical NBTI relaxation transients recorded on nanoscale SiGe devices is shown in Fig. 13(a). Several observations can be made:

1) the total $\Delta V_{\rm th}$ observed after the same NBTI stress strongly varies from device to device;
2) single carrier discharge events are visible [19], [20], each causing a discrete $\Delta V_{\rm th}$ step;

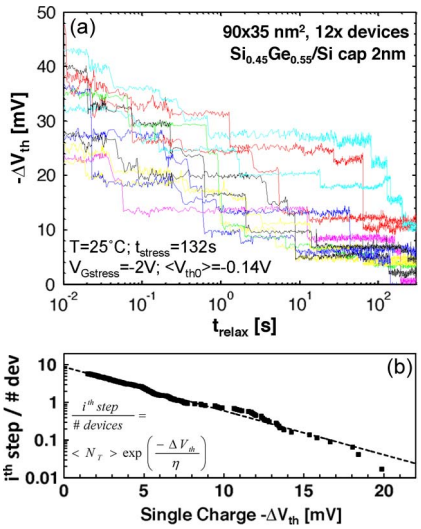

Fig. 13. (a) NBTI relaxation transients recorded on individual nanoscaled SiGe devices. For each device, multiple single defect discharge events are visible. (b) Weighted complementary Cumulative Distribution Function plot of the individual $\Delta V_{\rm th}$ step heights observed on multiple (41) devices. Despite the intentionally undoped epitaxially grown SiGe channel, the $\Delta V_{\rm th}$ step heights appear to be exponentially distributed [20], with an average value $\eta \approx 3.9$ mV. The average number of defects per device, $\langle N_T \rangle$, can be easily read in this plot as the intersection of the distribution with the y-axis [42].

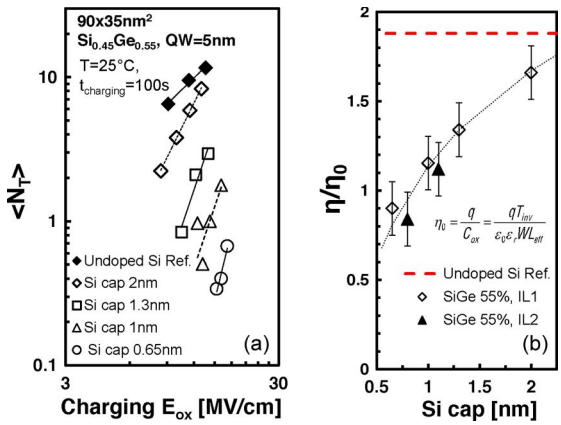

Fig. 14. (a) Consistently with large area device data [cf. Fig. 5(c)], nanoscaled SiGe channel pMOSFETs with a reduced Si cap thickness show reduced average number of charging/discharging defects per device $\langle N_T \rangle$, and a stronger field acceleration. (b) Extracted average $\Delta V_{\rm th}$ step heights η for SiGe devices with different Si cap and for undoped Si channel devices, after a charging phase at $E_{\rm ox} \approx 12$ MV/cm. The extracted values of η are normalized for the charge sheet approximation for the electrostatic of a single charge ($\eta_0 = q/C_{\rm ox}$). SiGe devices with the thinnest Si cap show a significantly lower $\eta(\sim 2\times)$. The observation is confirmed on SiGe devices with two different SiO_2 interfacial layer thicknesses. The red dashed line demarcates the benchmark value experimentally estimated on undoped Si channel ref. devices. The error bars on the estimated η values are related to the lower $\langle N_T \rangle$ observed for SiGe.

3) each device shows a different number of charging/discharging events (i.e., a different number of active oxide traps, N_T);
4) the $\Delta V_{\rm th}$ step heights appear to be approximately exponentially distributed [Fig. 13(b)], with average value η (i.e., the slope of the exponential distribution) but with some single charged oxide defects easily causing gigantic $\Delta V_{\rm th}$ [20].

Such anomalous large $\Delta V_{\rm th}$ are commonly ascribed to the percolative nature of the current in nanoscale devices associated with channel potential nonuniformity induced by variability sources (e.g., random Dopant Distribution, Line Edge Roughness, Metal Gate Granularity, etc.) [21].

SiGe pFETs with a reduced Si cap thickness showed a $\sim 10\times$ reduced average number of charge/discharge events per device, i.e., a reduced average number of active defects $\langle N_T \rangle$ [Fig. 14(a)] and a $\sim 2\times$ reduced average $\Delta V_{\rm th}$ step height η [Fig. 14(b)] with respect to their Si counterparts. These two experimental observations are readily explained with the model already discussed in Section V (cf. Fig. 8): fewer oxide defects are energetically favorable for SiGe channel holes (reduced average number of *accessible* defects $\rightarrow$ reduced $\langle N_T \rangle$), with the accessible defects located preferentially toward the gate side of the dielectric, resulting in a reduced electrostatic impact on the channel (i.e., reduced average $\Delta V_{\rm th}$ impact per charged defect).

We have previously shown [20] that the median NBTI-induced $V_{\rm th}$-shift in a population of nominally identical nanoscale devices can be estimated as $\langle \Delta V_{\rm th}(t) \rangle = \langle N_T(T) \rangle^* \eta$, with the $\Delta V_{\rm th}$ variance being $\sigma^2 \Delta_{\rm Vth} = 2\eta^2 \langle N_T(t) \rangle$. Thanks to the reduced $\langle N_T \rangle$ and η, the optimized (Si)Ge channel technology promises a significant reliability improvement

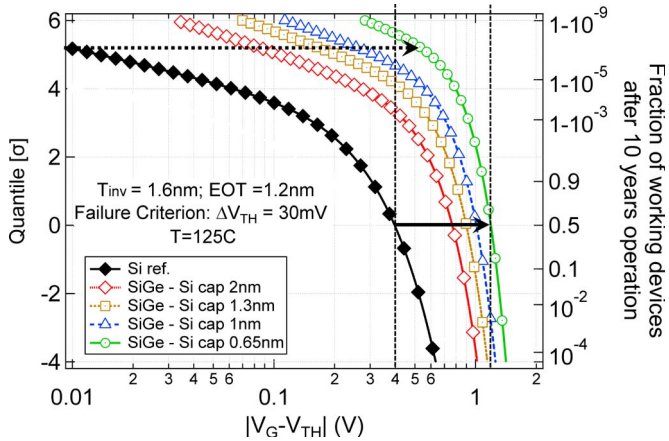

Fig. 15. Calculated fractions of working devices after 10 years continuous operation at varying operating voltages [42] for the different gate stacks studied here. A dramatic improvement of the distributions is apparent for SiGe devices with reduced Si cap thickness. Note: large area device lifetime would appear in this plot as a vertical dashed line (whole population fails above maximum allowed operating voltage, while it passes for lower voltages) with same median value (Probit $= 0$) of the respective nanoscaled device distribution. The reliability improvement observed in large area SiGe devices (demarcated by the solid arrow at Probit $= 0$) is expected to be magnified at high percentiles (demarcated by the dotted arrow, at $\sim$1 ppb).

when considering a realistic population of billions of devices, as illustrated in Fig. 15 [42].

VIII. Performance vs. Reliability

We have shown above that a reduced Si cap thickness is the key for improved reliability. However, previous work reported reduced hole mobility for SiGe devices with a reduced Si cap thickness [9]. This mobility loss was ascribed to poorer interface passivation: with a thinner Si cap more Ge from

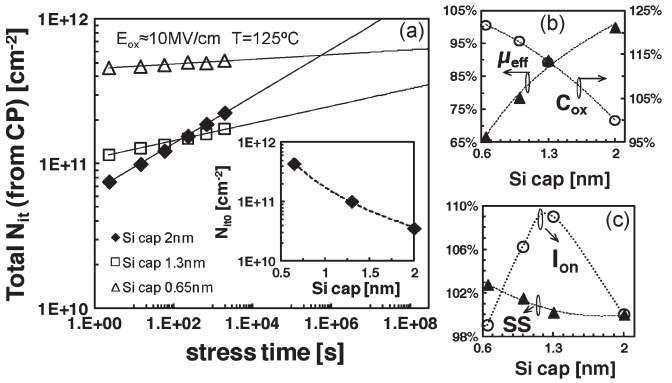

Fig. 16. (a) A reduced Si cap thickness yields a higher interface state density on the fresh device ($N_{\rm it0}$, inset). However, the larger NBTI-induced $\Delta N_{\rm it}$ on a 2 nm thick Si cap sample [see Fig. 6(b)], causes the total $N_{\rm it}$ to soon overtake the values measured on a medium-thick Si cap sample. (b) Thinner Si cap samples show reduced mobility due to poorer interface passivation, but also increased $C_{\rm ox}$ thanks to reduced hole displacement [see Fig. 1(b)]. (c) This trade-off (mobility vs. $C_{\rm ox}$) yields an optimum $I_{\rm ON}$ for a medium Si cap. The sub-threshold swing is almost independent of the Si cap, thanks to the higher $C_{\rm ox}$ reducing the effect of a poorer interface passivation for thin Si caps.

the channel segregates to the interface [30], causing a higher density of pre-existing interface states. This can be seen in the inset of Fig. 16(a), where $N_{\rm it0}$ values extracted from CP measurements are reported for three different Si cap thickness.

However, it is worth emphasizing that the higher $\Delta N_{\rm it}$ observed during NBTI stress for devices with thicker Si caps [see Fig. 6(b)] is projected to quickly cause the interface quality of these samples to become worse than the one of the devices with reduced Si cap thickness [Fig. 16(a)].

Furthermore, it is worth noting that a thinner Si cap, while causing a mobility reduction, increases the gate stack $C_{\rm ox}$ thanks to reduced hole displacement [reduced $T_{\rm inv}$, see Fig. 1(b)], as shown in Fig. 16(b). When looking at the $I_{\rm ON}$ performance of SiGe devices with different Si cap thickness, the best performance is typically obtained for a medium thickness Si cap of around 1.2 nm, where a trade-off between lower $T_{\rm inv}$ and reduced mobility is obtained [Fig. 16(c)]. However, the $I_{\rm ON}$ stays within a $\pm 5\%$ range for the whole Si cap thickness range considered here. Looking at the sub-threshold swing of the devices (which ultimately determines the $I_{\rm OFF}$ figure of merit, when combined with the device $V_{\rm th0}$), a very small increase is observed for the thinnest Si cap [$< 3\%$, Fig. 16(c)], thanks to the higher $C_{\rm ox}$ (i.e., lower $T_{\rm inv}$) reducing the detrimental effect of a poorer interface passivation [see Fig. 16(a) inset].

In conclusion, the Si cap shows an overall limited impact on the $I_{\rm ON}/I_{\rm OFF}$ device metrics while it has a dramatic impact on the device reliability. Therefore, when implementing a (Si)Ge channel process we suggest to perform a Si cap thickness optimization based on performance/leakage metrics first, and then reduce this thickness slightly as to meet the NBTI reliability specifications.

IX. Conclusion

We have discussed the NBTI reliability of Ge-based channel pMOSFETs with SiO_2/HfO_2 dielectric stack. The results clearly show significantly improved NBTI reliability for this family of high-mobility channel devices. A reliability-oriented gate-stack optimization, with a high Ge fraction, a sufficiently thick quantum well and reduced Si cap thickness was developed to demonstrate ultra-thin EOT SiGe devices with 10 years NBTI reliability at operating $V_{\rm DD}$. The NBTI reduction was ascribed to a reduced availability of interface precursor defects, and to a favorable alignment shift of the Fermi level in the (Si)Ge channel with respect to pre-existing defect energy levels in the dielectric layers.

Owing to this beneficial effect, a reduced time-dependent variability of nanoscaled (Si)Ge pFETs is also expected. In particular, we reported a significant reduction of the average number of active oxide defects $\langle N_T \rangle$ causing charge/discharge events, and of the average impact on the device characteristic per each trapped charge (η). Finally, it was shown that the reliability improvement is obtained not to the detriment of the device performance.

The superior NBTI reliability was noted to be process- and architecture-independent by comparing different families of devices, and by comparing with data published by other groups. *The reduced NBTI can be therefore considered an intrinsic property of the MOS structure consisting of a Ge-based channel and a* SiO_2/HfO_2 *dielectric stack*, further emphasizing this system as a leading candidate for future CMOS technology nodes.

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