(LATE)

Reliability and Performance Considerations for NMOSFET Pass Gates in FPGA Applications

B. Kaczer[1,*], C. S. Chen[2,†], J. T. Watt[2], K. Chanda[2], P. Weckx[1,3], M. Toledano Luque[1], G. Groeseneken[1,3], T. Grasser[4]

[1]imec, Kapeldreef 75, B-3001 Leuven, Belgium; [2]Altera Corp., USA; [3]ESAT KULeuven, Belgium; [4]TU Wien, Austria

[*]e-mail: kaczer@imec.be; [†]e-mail: chrchen@altera.com

***Abstract*—The NMOSFET-only pass gates used in some digital CMOS applications, such as the Field-Programmable Gate Arrays (FPGAs), are apparently vulnerable to Positive Bias Temperature Instability (PBTI). Here we discuss the impact of PBTI frequency and workload on high-k/metal-gate NMOSFETs in terms of Capture-and-Emission Time (CET) maps and quantitatively explain the degradation of our test circuit. From individual trapping events in deeply-scaled NMOSFETs we then project PBTI distributions at 10 years. Finally, we show that at increased supply voltage the pass gate speed degradation is outweighed by signal transfer speedup, resulting in a net performance improvement.**

Keywords—reliability; performance; pass gate; PBTI

I. Introduction

Reliability of the more conservative CMOS technologies of the past has been guaranteed at the technology level. The continuous downscaling resulted in reduced reliability margins, rendering the functionality of some CMOS circuit topologies potentially susceptible to device aging [1]. Thorough examination and certification of reliable operation throughout the entire application lifetime is therefore nowadays required during design. Specifically, the NMOSFET-only pass gate used in some digital CMOS applications, such as the Field-Programmable Gate Arrays (FPGAs), appears particularly vulnerable to Positive Bias Temperature Instability (PBTI)—a simple SPICE simulation of a NMOSFET-pass gate discussed here shows the NMOSFET threshold voltage shift ΔV_{th} of ~10 mV causes ~10% stage delay loss at operating voltage.

At the same time circuit designers strive to increase the performance of their designs by different means, notably by increasing supply voltages [2]. This almost always occurs at the expense of design reliability. The reliability engineer's task is then finding and guaranteeing the optimum balance between performance and reliability. For the specific case of the NMOSFET-pass gate discussed here we, however, find that increasing the supply voltage increases its overall performance (speed) even after its PBTI aging is factored in.

We first characterize the impact of PBTI on NMOSFET pass gates in a custom-designed test circuit. We then describe the instability in individual devices in terms of Capture-and-Emission Time (CET) maps and discuss the frequency and workload dependences within this framework. Within the same framework of PBTI we then successfully quantitatively explain the degradation of the test circuit. Subsequently, we study individual trapping events in deeply scaled devices of the same technology and we use this information to project time-dependent PBTI distributions at 10 years. Finally, we show that at increased supply voltage the pass gate speed degradation is outweighed by signal transfer speedup, resulting in net performance gain at no PBTI reliability expense.

II. Experimental

The custom-designed test circuit, depicted in Fig. 1a, [3] as well as individual NMOSFET devices, summarized in Table I, were fabricated in the scribe lines of a commercial 28 nm high-k/metal gate technology wafer. The ring-oscillator circuit allows simultaneously stressing NMOSFET pass gates (V_{gate}) placed between inverter stages and measuring the resulting impact on delay per stage through change in the oscillation frequency.

All measurements were performed at a specified elevated temperature. Because of the limited number of devices per (large) die, evaluation had to be performed over the entire 300 mm wafer, adding some across-wafer variability to the presented results.

NMOSFET	L (nm)	W (nm)
large	~1000	~1000
short	~28	~1000
small	~28	~100

Table I: Single NMOSFET devices used in this work.

III. Results and Discussion

The relation between stage delay and the NMOSFET pass gate threshold voltage shift ΔV_{th} in Fig. 1b is obtained from SPICE simulations. Note that the ΔV_{th} impact on stage delay increases exponentially as V_{gate} is lowered toward V_{CC}, documenting the potential vulnerability of NMOSFET-only pass gates toward degradation.

The measured change in the stage delay at stress V_{gate} and nominal V_{CC} is shown in Fig. 1c. We now show that this measurement can be excellently *quantitatively* explained by PBTI in the pass gate. PBTI is discussed entirely in terms of the corresponding CET maps.

A. PBTI in CET map

The CET map allows describing the entire PBTI degradation process in terms of the probability density of capture and emission times of the responsible gate-oxide defects [4]. The map, as extracted from an extended Measure-Stress-Measure (eMSM) sequence on a single NMOSFET device (Fig. 2a), is agnostic of the underlying physical model [5,6]. A large device has been used to avoid variability due to single-carrier events [7,8]. The "raw" map

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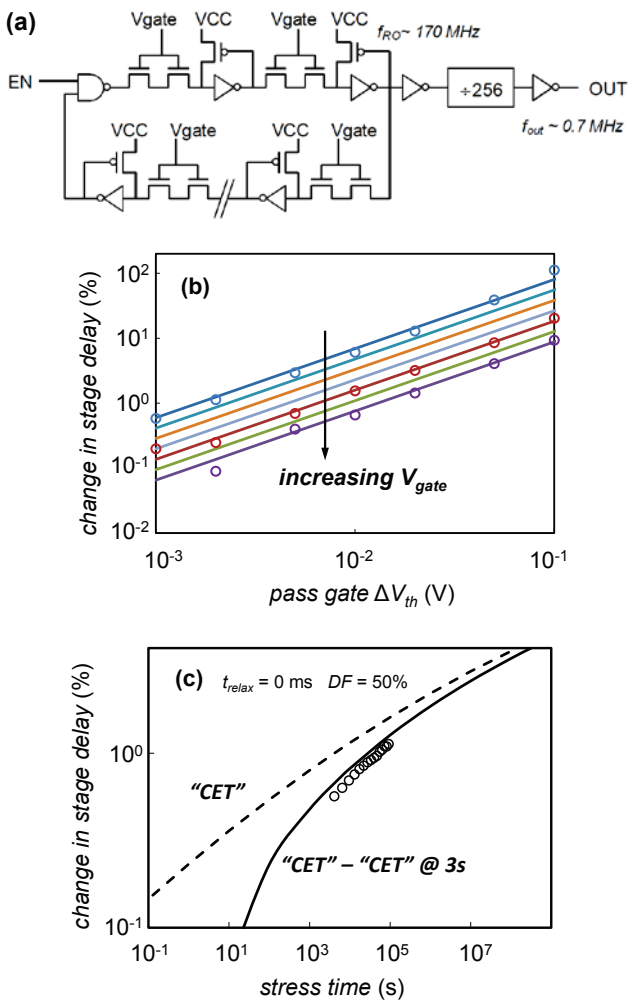

Fig. 1: (a) The ring oscillator (RO) test circuit consists of 127 stages and oscillates at ~170 MHz at operating conditions [3]. NMOSFET-only pass-gates are placed between each RO stage and are controlled by a separate terminal V_{gate}. (b) SPICE-simulated change in stage delay (symbols) as a function of the pass gate threshold voltage shift ΔV_{th}. The dependence is parametrized (lines). (c) Change in RO frequency (symbols; normalized to the first reading in 3 s), converted into change in delay per stage, measured at stress V_{gate}, is excellently matched by considerations based on the PBTI CET map (lines).

data were fitted with a single bi-variate Gaussian distribution, allowing both smoothing and extrapolating from the measurement window towards both very short (clock cycle) and long (application lifetime) times [4].

Fig. 3a illustrates how the CET map is used to construct the time dependence of DC PBTI degradation of a single NMOSFET. Only traps in the rectangle delimited by $\tau_{capture} \in [0, t_{stress}]$ and $\tau_{emission} \in [t_{relax}, \infty]$ are contributing to the device's ΔV_{th}. A simple integration thus reproduces the original data in Fig. 2a as well as shorter eMSM measurements performed at different overdrive voltages $V_{ov} = V_{gate} - V_{th}$ (Fig. 3b). Note in Fig. 3b that the projection based on the CET map is not a perfect power law, resulting in a more optimistic projection of degradation at 10 years.

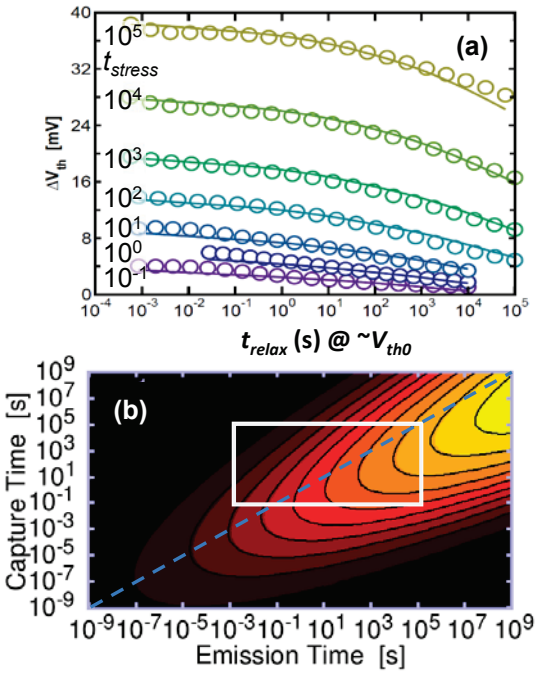

Fig. 2: (a) Threshold voltage shift ΔV_{th} of an individual large NMOSFET as a function of stress and relaxation times measured with the eMSM technique [5]. The measurements (symbols) are back-fitted with the CET map in (b) (lines). (b) The data in (a) converted into a CET map (measured data in white rectangle extrapolated using a bi-variate Gaussian distribution [4]). The map represents (is proportional to) the probability of finding charged defects with given capture $\tau_{capture}$ and emission $\tau_{emission}$ times.

Fig. 4 then illustrates how the same CET map describes the *AC* PBTI degradation; specifically it shows which traps are charged (occupied) traps and contributing to ΔV_{th} [9]. This is possible provided PBTI process is first order (traps exist in a single charged state and a single discharged state) [4]. Integration over the occupied traps gives ΔV_{th} independent of high frequencies, which is also reproduced experimentally on large devices (Fig. 5a) [10]. The most revealing confirmation of the CET map-based approach is however in Fig. 5b—the experimentally observed workload dependence is excellently reproduced.

Note that, in contrast to NBTI [5], the degradation at *DF* = 50% is ~90% of the DC (i.e., *DF* = 100%) value. This is because the PBTI traps are slow to discharge (emit), as documented in Fig. 2b—the peak maximum is below the $\tau_{capture} = \tau_{emission}$ line.

The pass gates in the test circuit in Fig. 1a are, however, based on *short* NMOSFET devices. Fig. 6 documents that short devices degrade less. This is likely due to thicker gate oxide (and the resulting lower electric field), as discussed e.g. in [11].

PBTI frequency independence is confirmed in short devices in Fig. 5b, allowing us to apply the same CET approach to scale short device PBTI degradation to ~100 MHz and excellently quantitatively reproduce the change in stage delay measured in Fig. 1b.

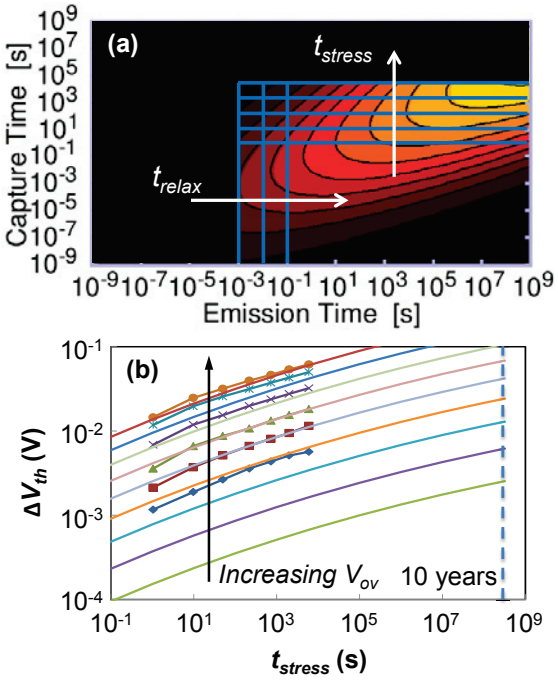

Fig. 3: (a) The CET map overlaid with an occupancy map representing a shorter, DC-stress eMSM measurement. Only traps in the region delineated by blue vertical and horizontal lines are occupied and thus are contributing to ΔV_{th}. The largest rectangle corresponds to the maximum stress time (6,000 s, cf. (b)) and the shortest relaxation time (~1 ms) used in the measurement. (b) Measured ΔV_{th} at t_{relax} = 1 ms as a function of stress times at different stress overdrives (symbols) fitted by integrating the CET map in (a) (lines). Voltage scaling is done as per Fig. 6.

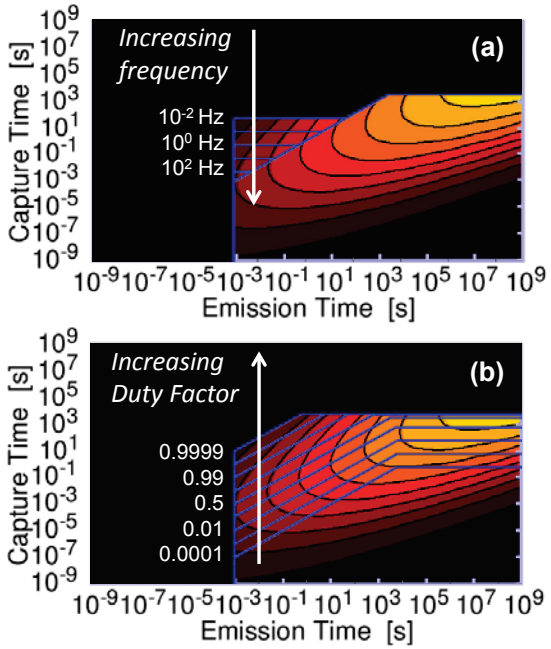

Fig. 4: Analogously to Fig. 3a, the CET map overlaid with an occupancy map allows representing stress at (a) different frequencies and (b) duty factors. (a) A weak frequency f dependence is expected at low frequencies [10]. At higher frequencies the occupancy tends toward beveled rectangle delimited by t_{stress} and t_{relax}. (b) The beveled-rectangle region is increasing with increasing Duty Factor (f = 1 kHz).

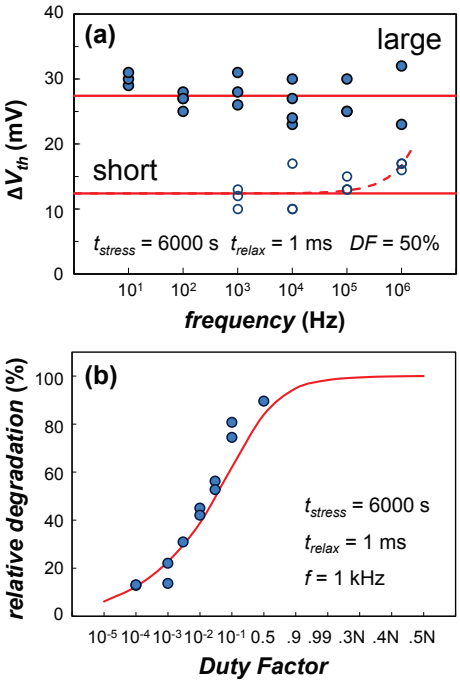

Fig. 5: (a) Frequency-independent threshold voltage shifts and (b) the relative decrease of ΔV_{th} at low duty factors are well predicted by integrating the corresponding areas shown in Figs. 3a and 3b, respectively. Solid circles: device data, solid lines: CET map integration. Dashed line: Increase at higher frequencies f traced to an overshoot in the leading edge of V_{gate} AC waveform, thus $\Delta V_{th} = \Delta V_{th,low\text{-}f} + a f$.

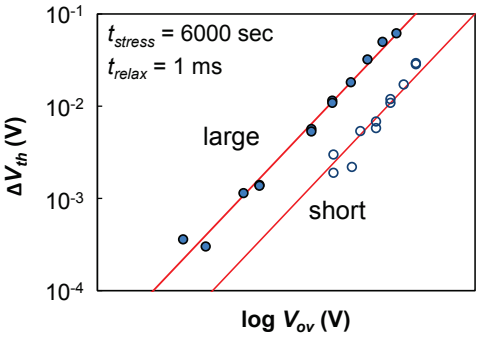

Fig. 6: Voltage acceleration of large and short devices. Short devices degrade less.

B. Reliability and performance projections

Single electron trap discharge events were studied in the *small* devices in Time-Dependent Defect Spectroscopy (TDDS) experiments (not shown) [8]. As in [12], a bimodal exponential distribution of single electron ΔV_{th}'s was observed with expectation values η of 0.7 and 4 mV, respectively. The following time-dependent variability analysis was based on the latter, i.e., the wider distribution, since these steps were present at multiple stress voltages.

Fig. 7a shows the projection of distributions of threshold voltage shifts [7] of the NMOSFET-pass gates with areas used in an actual product at 10 years with varying operating V_{CC} and the specified temperature. The mean ΔV_{th} values

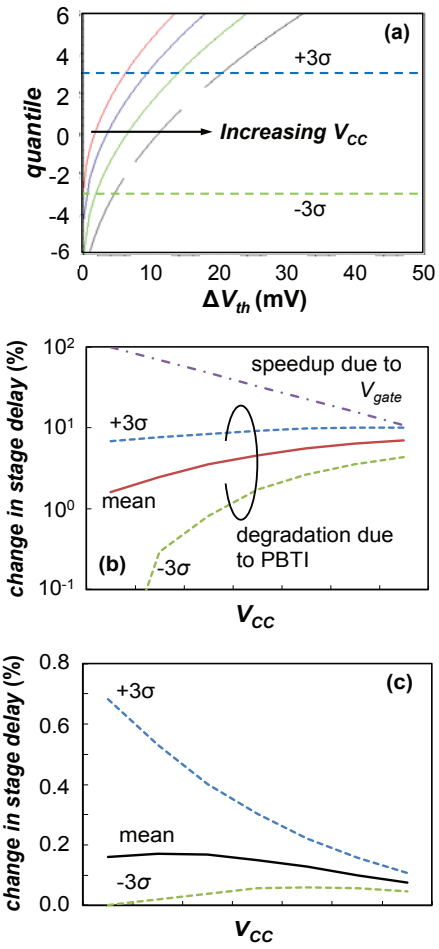

Fig. 7: (a) The threshold voltage shifts V_{th} in individual pass gates in an actual application will be distributed. The distributions at varying V_{CC}'s are based on 10-year projected mean value $<\Delta V_{th}>$ and η = 4 mV. (b) The evolution of distributions in (a) described through the ±3 σ and mean depenences on V_{CC}. The threshold voltage shifts are converted into relative stage delays through Fig. 1b. Also shown is the relative stage speedup due to increased V_{gate}. (c) With increasing V_{CC}, the relative stage delay will degrade due to increased BTI but will simultaneously improve due to speedup (cf. (b)). The overall effect of increasing V_{CC} will thus be positive, while, at the same time, the variability will decrease.

were projected as in Fig 3b (for the short devices; not shown). Fig. 7a illustrates that although the pass gates are expected to shift little *on average*, a small fraction of devices is expected to shift many multiples of the mean value. This time-dependent variability thus needs to be taken into consideration already during the application design phase.

The mean and the ±3σ ΔV_{th} values from Fig. 7a were converted into the change in stage delay (Fig. 1b) and replotted vs. varying V_{cc} in Fig. 7b (assuming $V_{gate} = V_{CC}$). As expected (cf. Fig. 6), higher pass gate stress results in more severe degradation of the stage delay. However, higher V_{cc} also results in faster operation of the pass gate, as calculated with SPICE and also shown in Fig. 7b. The overall change in pass gate delay will be the product of these two effects, shown in Fig. 7c. The figure shows that the speedup due to increased V_{CC} outweighs the PBTI degradation. Moreover, the projected time-dependent variability will also decrease at higher V_{CC}. We therefore conclude the performance of the pass gate can be increased without any PBTI penalty. Since SPICE simulations show hot carrier degradation is not an issue in NMOSFET pass gates (not shown) we expect maximum V_{CC} will be limited by gate oxide breakdown.

IV. Conclusions

PBTI frequency and workload dependences in high-k/metal-gate NMOSFET-only pass gates have been discussed within the CET map framework, allowing to quantitatively explain the degradation of our test circuit. Furthermore, it has been shown the pass gate performance can be increased at no PBTI reliability penalty.

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