Understanding Correlated Drain and Gate Current Fluctuations

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***Abstract*— Recently, some experimental groups have observed the occurrence of correlated drain and gate current fluctuations, which indicate that both currents are influenced by the charge state of the same defect. Since the physical reason behind this phenomenon is unclear at the moment, we evaluated two different explanations: The first model assumes that direct tunneling of carriers is affected by the electrostatic field of the charged defect. Interestingly, this model inherently predicts the gate bias and temperature dependences observed in the experiments and is therefore quite promising at a first glance. In the second model, our multi-state defect model is employed to describe trap-assisted tunneling as a combination of two consecutive nonradiative multi-phonon transitions — namely hole capture from the substrate followed by hole emission into the poly-gate. The latter transition is found to be in the weak electron-phonon coupling regime, which requires the consideration of all band states instead of only the band edges. Our investigation shows that the electrostatic model must be discarded since it predicts only small changes in the gate current while the extended variant of the multi-state defect model delivers quite promising results.**

INTRODUCTION

As a consequence of the continuous miniaturization of MOS devices, fluctuations in the drain currents have become increasingly pronounced and even reached a level that can seriously affect device operation. Therefore, the random telegraph noise (RTN) in the drain current has become a well studied phenomenon over the years [1–5]. It has been established that the drain current noise originates from charge capture and emission events into and out of oxide defects, where the charge transfer between the substrate and the defects is described by nonradiative multi-phonon (NMP) processes [6, 7]. In the context of drain current noise, the multi-state defect model [8] has been proposed, which can give an explanation for a variety of interesting features, including temporary and anomalous RTN.

Andersson *et al.* [9] observed that also the gate current can show an RTN signal, and ascribed this phenomenon to trap-assisted tunneling (TAT). Interestingly, recent studies [10–13] have revealed that the drain current noise is at least sometimes correlated to the gate current noise in the latest generation of deeply scaled MOSFETs (cf. Fig. 1). This behavior has been observed for both pFETs as well as nFETs (see Tab. 1). While hole capture is found to *increase* the gate current in pFETs (case D), both variants have been observed in nFETs: Toledano *et al.* [11] observed oxide traps, which *reduce* the gate current upon electron capture (case A). By contrast, Chen *et al.* [10] found an increased gate current upon electron capture (case B), which is the analogous behavior to what has been seen in pFETs (case D). Interestingly, the correlation of

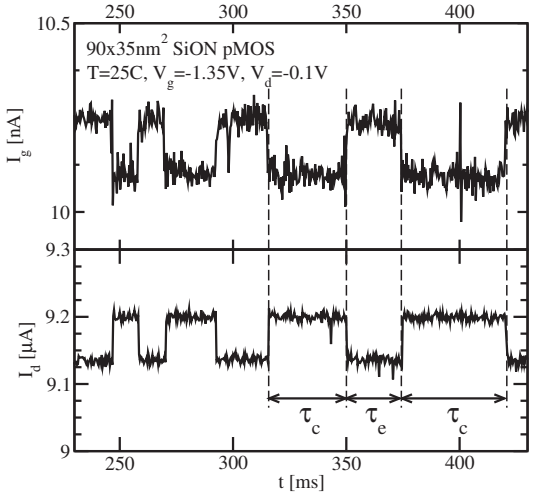

Fig. 1: Simultaneously recorded I_g (upper panel) and I_d traces (lower panel) [11]. Upon the hole capture (after a time period of τ_c), the charged defect reduces I_d to a lower level for electrostatic reasons. At the same time a significant increase in I_g is observed, meaning that an additional conductive path over the defect has been opened. When the hole is emitted after a time period of τ_e, the conductive path is closed again and I_d returns to its previous level.

Case	$\Delta\lvert I_\mathrm{d}\rvert/\Delta\lvert I_\mathrm{g}\rvert$	Oxide Material	$\lvert\Delta I_\mathrm{g}/I_\mathrm{g0}\rvert$
nFET (A)	> 0	SiON [11]	∼70%
nFET (B)	< 0	HfO_2 [10]	∼3%
pFET (C)	> 0	not reported	
pFET (D)	< 0	SiON [11, 13]	∼8%, ∼5%

Tab. 1: Correlation between drain and gate current noise. Case C has not been reported yet.

case A allows for an interpretation based on an electrostatic effect that will be explained later. As such, this observation is of considerable scientific interest and is therefore also included in the present study.

Microscopically, the correlation in current fluctuations indicates that the level of the gate current is linked to the charge state of the oxide defects. One possible explanation for this observation in nFETs can be given by an electrostatic model based on direct tunneling. An alternative explanation is built on our multi-state defect model, which describes the hole exchange with the substrate in BTI [14]. This model can be extended to describe the gate leakage current as TAT. In this work, we evaluate both models, thereby investigating the physical cause of the gate RTN as well as its link to drain RTN in MOS transistors.

978-1-4799-0480-8/13/$31.00

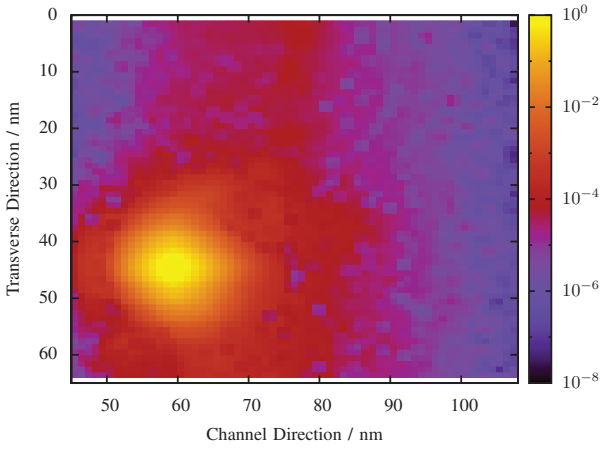

Fig. 2: The relative reduction (in percent) of the gate current density due to the charging of one defect in an nFET. For the simulations of the device in Fig. 1, the NEGF method [17, 18] was employed to accurately calculate the direct tunneling current through the gate oxide assuming several random dopant configurations. These simulations were performed for the cases when the defect is neutral and charged. The resulting reduction of the local tunneling current is displayed in the color map. However, an integration over the entire gate area yields a total change of less than one percent (for the worst-case dopant configuration) while a value around 75% is found experimentally [11]. This indicates that the simple electrostatic picture can not explain the observed gate current fluctuations.

Electrostatic Model

The gate leakage current is frequently traced back to direct tunneling, which is commonly known to vary weakly with temperature [15, 16]. Since the gate current fluctuations were also found to be temperature insenstive, it appears reasonable to link them to direct tunneling. This idea is reflected in the electrostatic model, which will be briefly discussed in the following: When a defect captures an electron from the substrate, the inversion layer is locally repelled by the trapped charge. Quantum mechanically, this means that the wavefunction around the defect is reduced in its amplitude and shifted away from the interface. As a consequence, the local direct tunneling current is reduced, which will be visible as steps in the gate current (case A). Interestingly, the gate current fluctuations in this model inherently follow the gate bias dependence of the overall gate tunneling current since they originate from the same kind of tunneling process as the gate current itself. This is quite remarkable as this gate bias behavior has also been observed experimentally.

For evaluating the electrostatic model, Baumgartner *et al.* [19] created large statistics of the change in the gate current due to charging one defect (see Fig. 2). These statistics are built upon numerous different random dopant configurations and trap locations and also include cases in which the charged defects are positioned such to have a large impact on the direct gate tunneling current. The device simulations were based on the density gradient method. The local direct gate tunneling current was calculated for one-dimensional cuts perpendicular to the interface using the non-equilibrium Green's function method. These simulations yield gate current fluctuations of less than 1% for the nMOS. As such, the electrostatic model can not account for the large gate leakage fluctuations seen in the experiments (75% in nFETs) and therefore must be ruled out.

An analogous behavior, i.e. a simultaneous drop in the drain and the gate current, has not been experimentally observed in the pFETs so far (case C). However, this is possibly due to the fact that the correlated current noise has not been intensively investigated and the analogous behavior in the pFETs has simply remained unnoticed so far. Therefore, the above investigations for the nFETs (case A) were repeated for pFETs (case C). But again, the gate fluctuations were limited to values less than 1%, much less than the experimentally observed values (see Tab. 1).

TAT Model

The fluctuations in the drain current noise are usually ascribed to charge capture and emission events. Interestingly, the same processes are also believed to play a central role in BTI. As such, drain current noise and BTI are regarded as two sides of the same coin. The latter can be well described by the multi-state defect model [8], which has been derived from the findings of time dependent defect spectroscopy (TDDS) [8, 20, 21]. This measurement technique provides strong experimental evidence for the existence of metastable configurations, which are essential for a series of experimental features [8, 20, 21]:

- The RTN/BTI capture (τ_c) and emission (τ_e) times of individual defects are decorrelated.
- The capture times exhibit a strong gate bias dependence that levels off towards higher gate biases.
- Furthermore, they also feature a pronounced frequency dependence.
- The individual defects show a different detrapping behavior, depending on whether they are fixed positive or switching oxide traps.
- The metastable configurations give rise to particular noise phenomena, such as temporary and anomalous RTN.

Since the multi-state defect model gives an explanation for all these features, it was extended to describe the gate current fluctuations based on TAT.

In this model the actual charge capture and emission processes rely on NMP transitions, which can be described at different levels of sophistication. For instance, Schanovsky *et al.* [22] presented a quantum mechanical formulation based on lineshape functions (LSF). Here, we employ the classical high-temperature limit of the NMP theory, which provides a good approximation at usual device operation temperatures [22]. The corresponding hole capture ($k_{0/+}$) and emission ($k_{+/0}$) rates are given by the energy integrals

$$k_{0/+} = k_0 \int D(E)\lambda_\mathrm{p}(E,x_\mathrm{t}) f_{0/+}(E-E_\mathrm{t}) f_\mathrm{p}(E)\mathrm{d}E \qquad (1)$$

and

$$k_{+/0} = k_0 \int D(E)\lambda_\mathrm{p}(E,x_\mathrm{t}) f_{+/0}(E_\mathrm{t}-E) f_\mathrm{n}(E)\mathrm{d}E \qquad (2)$$

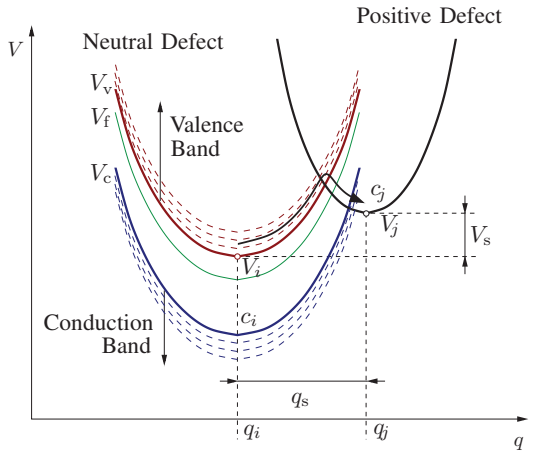

Fig. 3: Configuration coordinate diagram for hole capture. The defect is present in two charge states, labeled i and j here. The position of their adiabatic potentials are determined by their optimum coordinates q_i and q_j and their energies V_i and V_j in their equilibrium configurations. When the defect is neutral (state i), the hole involved in the charge transfer process is located in the semiconductor. There, it occupies one of the band states, which corresponds to different carrier energies E and are represented by the dashed parabolas. Note that the energy integrals in the equations 3 and 4 run over all band states E, where each of them is associated with one parabola. V_c and V_v corresponds to the adiabatic potentials for the case when the hole occupies the conduction or the valence band edge, respectively.

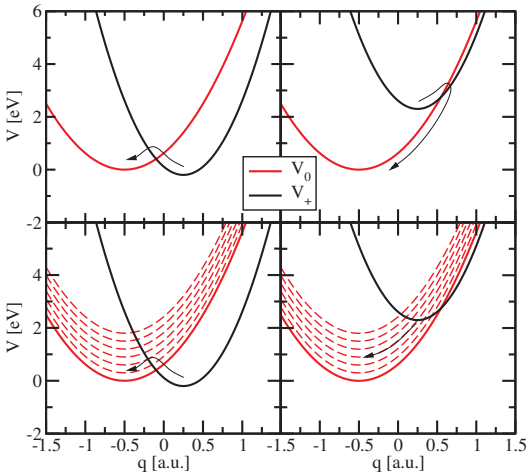

Fig. 4: Configuration coordinate diagram for the exemplary case of hole emission. In the left panels, we assumed strong electron-phonon coupling. In this case the intersection point of the two parabolas must be located between their two energy minima. By contrast, the right panels show the case for weak electron-phonon coupling, where the intersection point must lie outside the two energy minima. In the upper panels only the valence band edge (red solid curve) is taken into account while in the lower panels all valence band states are incorporated. Note that for the case of weak electron-phonon coupling the dominating transition (indicated by the arrows) changes when considering all band states.

with E being the carrier energy. $D(E) = D_{\mathrm{n}}(E) + D_{\mathrm{p}}(E)$ is composed of the conduction (D_{n}) and the valence (D_{p}) band density of states. Note that this formulation of the NMP transition rates allows to describe a charge exchange with the substrate or the gate by choosing the respective density of states. $f_{\mathrm{p/n}}(E)$ corresponds to the hole/electron occupancy, which is in thermal equilibrium for small drain biases and therefore follows Fermi-Dirac statistics. $\lambda_{\mathrm{p}}(E, x_{\mathrm{t}})$ denotes the electron/hole WKB factor with E_{t} and x_{t} being the thermodynamic trap level and the trap depth, respectively. $f_{0/+}$ and $f_{+/0}$ denote the LSF, which can be evaluated using

$$f_{i/j}(V_{\mathrm{s}}) = \frac{1}{2}\sqrt{\frac{c_i\beta}{\pi}}\frac{\mathrm{e}^{-\beta V_{i/j}(V_{\mathrm{s}})}}{|c_i\Delta q_1 - c_j(\Delta q_1 - q_{\mathrm{s}})|} \tag{3}$$

and

$$V_{i/j}(V_{\mathrm{s}}) = \frac{c_i q_{\mathrm{s}}^2}{(\frac{c_i}{c_j}-1)^2}\left(1 \pm \sqrt{\frac{c_i}{c_j} + \frac{V_{\mathrm{s}}(\frac{c_i}{c_j}-1)}{c_j q_{\mathrm{s}}^2}}\right)^2 \tag{4}$$

with $i, j = 0, +$. The LSF gives the probability for an vibrational transition from an initial (i) to a final (j) charge state of the defect [14]. Importantly, it is governed by the shape of the corresponding adiabatic potential energy surfaces. These potentials are usually described by harmonic oscillators (see Fig. 3), whose parabolic shapes are defined by their curvatures c_i and c_j, their spatial displacement q_{s}, and their energy separation ΔE ($\Delta E = E - E_{\mathrm{t}}$ for hole capture and $\Delta E = E_{\mathrm{t}} - E$ for hole emission). In the classical high-temperature limit, the NMP transition takes place at the intersection point. Hence, the defect must be thermally excited to this intersection so that a transition can occur. Thereby, the defect has to overcome a transition barrier $V_{i/j}(V_{\mathrm{s}})$ defined by equation (4).

It is emphasized that the energy integral in equation (3) incorporates NMP transitions into and out of all band states. For hole trapping in BTI, we have only encountered the case of strong electron-phonon coupling so far (see Fig. 4). There, the overall transition is always dominated by hole capture and emission into and out of the valence band edge while the other band states can be neglected to first order. Accordingly, the NMP transitions rates can be simplified as published in [8]. However, when facing the situation of weak electron-phonon coupling, the dominant transition is hole emission into one of the band states and one has to carry out the integration over the whole valence band. In this case the NMP transitions rates (1) and (2) must be chosen.

The traps in the multi-state defect model can be either neutral (state 1) or positively charged (state 2) and are described by the shape of their adiabatic potentials. Motivated by the findings of the TDDS [8], they are assumed to feature one stable and one metastable configuration for each charge state. This bistability results in a double well shape of their adiabatic potentials as shown in Fig. 5. The hole capture process follows the transition pathway from the neutral state 1 to the positive state 2 over the metastable state $2'$ while the respective emission process simply proceeds in the opposite direction. Their respective rates can be calculated using the first passage times [5]

$$\tau_{\mathrm{c}}^{2'} = \frac{k_{12'} + k_{2'1} + k_{2'2}}{k_{12'}k_{2'2}} \tag{5}$$

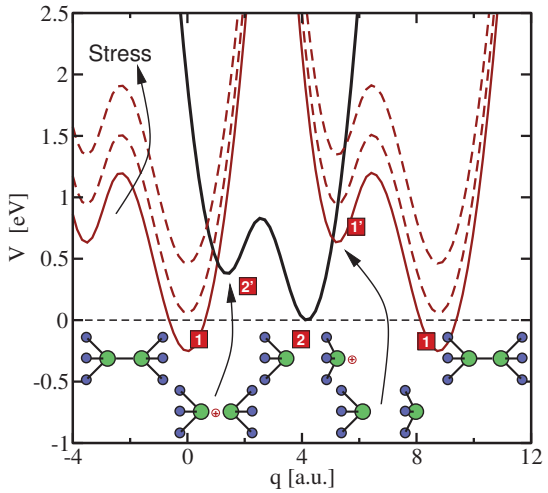

Fig. 5: A schematic of the configuration coordinate diagram for a bistable defect. The solid red and the black curves represent the adiabatic potentials for a defect in its neutral $(1, 1')$ and positive $(2, 2')$ charge state, respectively. The energy minima correspond to the stable or metastable defect configurations, labeled by $i = 1, 1', 2, 2'$. Note that the metastable states are marked by a prime $(1', 2')$. The NMP transitions $1 \leftrightarrow 2'$ and $2 \leftrightarrow 1'$ occur between different charge states while the thermal transitions $1 \leftrightarrow 1'$ and $2 \leftrightarrow 2'$ only involve same charge states. The latter transitions are associated with a structural rearrangement of the defect and are modeled using Arrhenius-type expressions [8].

$$\tau_{\mathrm{e}}^{2'} = \frac{k_{22'} + k_{2'2} + k_{2'1}}{k_{22'} k_{2'1}} \ . \tag{6}$$

The gate current fluctuations are caused by the defect when it is in its secondary configuration (states $1'$ and 2). There, the defect opens an additional gate current path through the oxide due to TAT. This process consists of two consecutive NMP transitions, namely hole capture from the substrate and hole emission into the poly. In order to define such a TAT current, one has to distinguish whether the hole is located in the substrate (s) or the poly-gate (p). As a consequence, the state $1'$ must be split into the substates $1'_{\mathrm{s}}$ and $1'_{\mathrm{p}}$, resulting in the refined state diagram illustrated in Fig. 6. In this state diagram, the gate current is then represented by the transition chain $1'_{\mathrm{s}} \leftrightarrow 2 \leftrightarrow 1'_{\mathrm{p}}$. A generalized formulation of TAT involves the NMP transition rates $k_{1'_{\mathrm{s}}2}$, $k_{21'_{\mathrm{s}}}$, $k_{1'_{\mathrm{p}}2}$, and $k_{21'_{\mathrm{p}}}$, all of which determine the electron occupancy of the traps f_{t} according to the equation

$$\partial_t f_{\mathrm{t}} = (k_{21'_{\mathrm{s}}} + k_{21'_{\mathrm{p}}})(1 - f_{\mathrm{t}}) - (k_{1'_{\mathrm{s}}2} + k_{1'_{\mathrm{p}}2}) f_{\mathrm{t}} \ . \tag{7}$$

Assuming steady state conditions ($\partial_t f_{\mathrm{t}} = 0$), the trap occupancy reads

$$f_{\mathrm{t}} = \frac{k_{21'_{\mathrm{s}}} + k_{21'_{\mathrm{p}}}}{k_{1'_{\mathrm{s}}2} + k_{21'_{\mathrm{s}}} + k_{1'_{\mathrm{p}}2} + k_{21'_{\mathrm{p}}}} \ . \tag{8}$$

Inserting the above expression into

$$I_{\mathrm{g}} = q_0 \big(k_{21'_{\mathrm{p}}} (1 - f_{\mathrm{t}}) - k_{1'_{\mathrm{p}}2} f_{\mathrm{t}} \big) \tag{9}$$

yields the TAT current

$$I_{\mathrm{g}} = q_0 \frac{k_{1'_{\mathrm{s}}2} k_{21'_{\mathrm{p}}} - k_{1'_{\mathrm{p}}2} k_{21'_{\mathrm{s}}}}{k_{1'_{\mathrm{s}}2} + k_{21'_{\mathrm{s}}} + k_{1'_{\mathrm{p}}2} + k_{21'_{\mathrm{p}}}} \ . \tag{10}$$

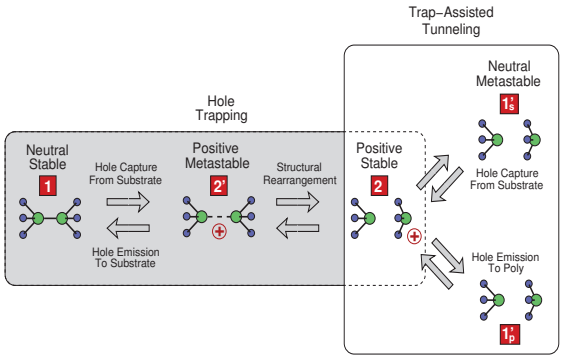

Fig. 6: Refined state diagram of the multi-state defect model. Hole capture and emission still occur as transitions between the states 1 and 2 over the metastable state $2'$. However, the state $1'$ has to be split in order to differentiate whether the hole lies in the substrate (s) or the poly-gate (p). With this modification in the state diagram, one can define a TAT process in which the hole is transferred from the substrate into the poly-gate and can therefore contribute to a gate current.

We remark that different formulas for the TAT current rates were applied in the literature [15, 23], however, they can lead to non-vanishing gate currents for a zero gate bias under certain circumstances.

Since a single defect is assumed to carry a large TAT current, the NMP transition rates $1'_{\mathrm{s}} \leftrightarrow 2$ and $1'_{\mathrm{p}} \leftrightarrow 2$ must be large compared to $1/\tau_{\mathrm{c}}$ and $1/\tau_{\mathrm{e}}$. Consequently, the trap occupancy is controlled through the trapping dynamics of the TAT current when the defect is in its secondary configuration. As the defect must be in state 2 for hole emission, the corresponding emission time must be correctly rewritten by

$$\tau_{\mathrm{e}}^{2'} \rightarrow \tau_{\mathrm{e}}^{2'} / (1 - f_{\mathrm{t}}) \ . \tag{11}$$

Results

In this section the multi-state defect model was tested for its ability to correctly predict the gate leakage fluctuations. For this purpose, the model was evaluated against the experimental data for the nanoscaled pFET investigated in [11]. The used model parameters[1] are listed in Tab. 2, where the meanings of the quantities follow the nomenclature in [14]. This study covers the gate bias and temperature dependence of both the heights of the gate current fluctuations ΔI_{g} as well as the capture and emission times of the drain current noise.

The simulated NMP transitions include the bandstates in the conduction and the valence band from the substrate and the poly gate, respectively (see Fig. 7). Furthermore, the energy integrals (3) and (4) were numerically integrated. Since their integrands sharply peak around a certain energy, they had to be quite finely discretized and thus become computationally expensive. In order to speed up the computation of these integrals, we employed an adaptive quadrature method. The results were obtained using an optimizer based on least square fits to the experimental data and are presented in Fig. 8.

[1] Note that the value of the thermal barrier $\varepsilon_{11'}$ is chosen such that the transition rates between the states 1 and $1'$ are negligible.

Transition $1 \leftrightarrow 2'$		Transition $1 \leftrightarrow 2'$	
E_t	-0.27 eV	E'_t	0.15 eV
c_1	1.00 eV/Å^2	$c_{1'}$	0.71 eV/Å^2
$c_{2'}$	1.64 eV/Å^2	c_2	1.00 eV/Å^2
$q_{12'}$	0.90 Å	$q_{1'2}$	1.39 Å
Other Parameters			
$\varepsilon_{\mathrm{T}2}$	0.65 eV	$\varepsilon_{2'2}$	0.10 eV
m_t	0.95	$\varepsilon_{11'}$	10.0 eV

Tab. 2: Model parameters used in Fig. 8 and 9. The shapes of the parabolic adiabatic potentials can be also given by the quantities $S\hbar\omega = 0.81$ eV, $R = 0.61$, $S'\hbar\omega = 1.37$ eV, and $R' = 0.71$.

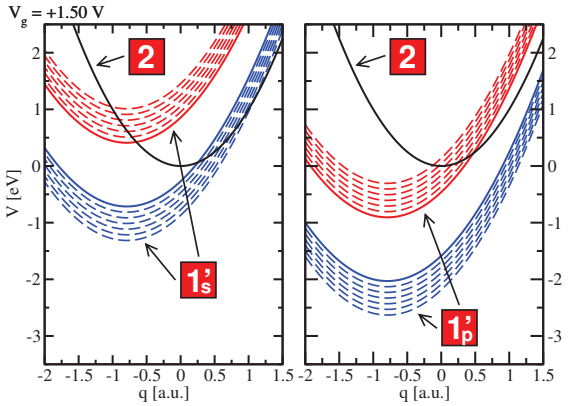

Fig. 7: Adiabatic potential energy surfaces extracted from the fits to the experimental data for the pFET in [11]. Our simulations consider NMP transitions from all conduction (blue) and valence (red) band states involving charge carriers from the substrate (left) and the poly gate (right). Note that the hole exchange with the substrate valence band is in the strong electron-phonon coupling regime as it is usually assumed for hole capture and emission in BTI. However when the defect exchanges holes with the poly-gate, weak electron-phonon coupling is found. Furthermore, the defects do not communicate with the conduction band in strong inversion, since hole capture ($1'_{\mathrm{s/p}} \rightarrow 2$) proceeds over a too large barrier and hole emission ($2 \rightarrow 1'_{\mathrm{s/p}}$) is blocked by the empty states in the conduction band.

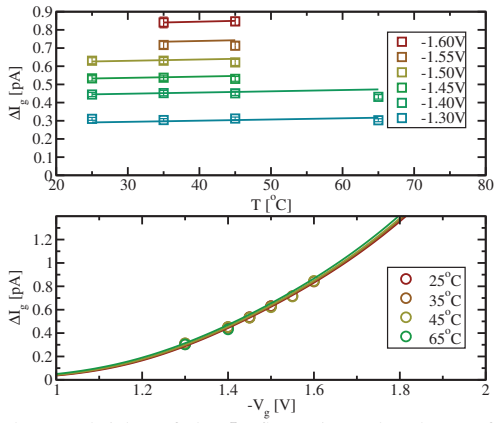

Fig. 8: The step heights of the I_g fluctuations plotted as a function of temperature (upper panel) and the applied gate bias (lower panel). The experimental data (symbols) show virtually no temperature dependence — a fact that is usually not associated with a transition over an NMP barrier. Nevertheless, the fit (lines) to the experimental data demonstrates that the multi-state defect model is capable of explaining this surprising behavior for reasons given in Fig. 9.

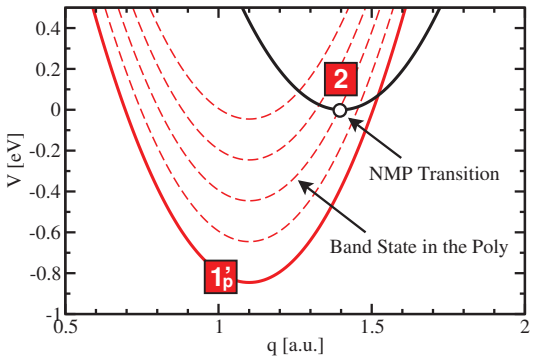

Fig. 9: Schematic configuration coordinate diagram for the transition $2 \rightarrow 1'_\mathrm{p}$. The red and the black parabola correspond to the case where the hole is located in the poly or at the defect, respectively. When the full width of valence band states (dashed parabolas) is taken into account, there always exists one parabola $U_{1'_\mathrm{p}}$ that intersects the minimum of state U_2. Then the NMP transition proceeds without a barrier and therefore shows no temperature dependence. Note, however, that for different gate biases different band states become dominant, which affects the WKB factor and in consequence gives rise to the observed gate bias dependence in Fig. 8.

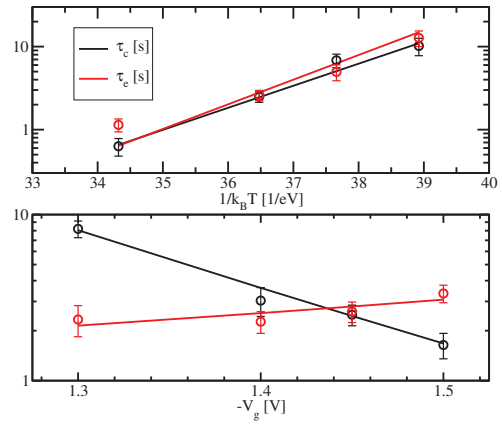

Fig. 10: Comparison of measured (symbols) and simulated (lines) for τ_c and τ_e. Good agreement with the experimental data is obtained for the temperature (upper panel) and the gate bias (lower panel) dependence.

The multi-state defect model can reproduce the temperature and gate bias dependence very well. Interestingly, the experimentally measured gate current fluctuations exhibit virtually no temperature activation. This behavior is usually associated with direct tunneling and not with an NMP transition over a thermal barrier. However, the defect in our fits is located close to the substrate interface ($x_\mathrm{t} = 4$ Å) so that the hole exchange rates with the substrate occur on much shorter timescales than the hole emission into the poly gate. Consequently, the gate leakage is controlled by the corresponding hole emission rate into the poly gate $2 \rightarrow 1'_\mathrm{p}$. The configuration coordinate diagram in Fig. 7 reveals that the respective NMP transitions are in the weak electron-phonon coupling regime. As schematically demonstrated in Fig. 9, the energy integral (4) has its dominant contributions from the band states that intersect the parabola U_2 around its minimum. These transitions feature negligible NMP barriers so that the overall transition k yields no temperature activation.

The multi-state defect model also yields a good agreement for the capture and emission times extracted from the noise measurement in [11] (see Fig. 10). The simulations were carried out for the set of parameters used in Fig. 8 in order to ensure that the model explains both the gate leakage and the trapping phenomenon at the same time.

It has to be mentioned that the correlation between the drain and the gate current noise can actually be shown by only a small fraction of strategically located oxide traps. However, these particular traps emit holes into the poly-gate during the TAT processes while other traps seen in BTI measurements communicate with the substrate only. As such, they do contain additional valuable information about the microscopic physics involved in the trapping and detrapping processes. For instance, it has been found that the trap is located close to the substrate interface and hole emission into the poly-gate is found to be in the weak electron-phonon coupling regime.

Conclusions

The multi-state defect model has previously only been applied to situations, such as the BTI and the drain current noise, where the trapping dynamics are governed by the substrate. However, the general framework of this model incorporates hole trapping and detrapping with the substrate as well as the gate and can therefore be used to describe TAT currents employing a few small extensions. In this paper, it has been demonstrated that the correlated gate/drain current fluctuations can be consistently explained by TAT within the multi-state defect model. As such, this study is also understood as an additional benchmark of the multi-state defect model, which can be regarded as a comprehensive description of oxide defects in reliability issues.

Acknowledgements

This work has received funding from the Austrian Science Fund (FWF) project n°23390-N24 and the European Community's FP7 n°261868 (MORDRED).

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