Novel Non-Volatile Magnetic Flip Flop

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Due to the ever increasing demand for cheap bulk logic and memory, scaling flash and CMOS technology in general will reach its fundamental limits soon. For instance, the stand-by power has become bigger than the switching power [1]. In order to tackle this problem a feasible solution is to introduce non-volatility into devices. Thus the whole circuit can be without power and energy is only required for changing a logic state or readout. Since all relevant information is kept without power, no initialization procedure like a boot routine is needed and true instant on applications are feasible. Flip flops constitute basic building blocks for such a non-volatile information processing system. Zhao et al. [2] gave an overview related to design of MRAM based logic circuits and their application. However, even though the flip flops shown by Zhao et al. [2] are non-volatile, the incorporated MTJs are used as auxiliary elements, while the logic operation takes place in the CMOS domain which suffers under scaling. Therefore, we propose a new type of non-volatile magnetic flip flop to further improve circuit density, device speed, and leakage loss. This is realized by a set of three MRAM stacks (two spin valve stacks for input and one MTJ stack for readout) with a common shared free layer exhibiting two magnetic stable states. The polarity of the input pulses is mapped to the two logic states and the result is stored via the magnetization orientation of the common free layer. By applying a current pulse through an input stack a spin torque is exerted on the common free magnetic layer in the corresponding stack and a spin disturbance is generated. The spin disturbance travels through the common free layer, until it reaches the opposite end of the layer where it is reflected and heads back to its origin and gets pushed back again. For low damping and high enough spin torque the excited local precessions start to build up, until they pass the energy barrier and relax into the other stable state. By applying synchronously two current pulses in the input stacks two spin disturbances are generated. If the spin torques in the input stacks exhibit the same orientations (same pulse polarity) the excited disturbances posses no phase shift and superimpose constructively, while for opposing torques (opposing pulse polarities) the disturbances posses a 180° phase shift and superimpose destructively. The resulting sequential logic writes logic “0” or “1” for identical pulse polarities and holds its state for non-matching polarities. If one of the inputs is inverted, RS flip flop logic without forbidden input combinations is achieved. We confirmed functionality by an extensive simulation study assuming 10nm, 20nm, and 30nm wide; 40nm, 80nm, and 120nm long; and 3nm thick common free layers exhibiting a magnetization saturation of 4. 10^5 A/m; an out-of-plane uni-axial crystal anisotropy of 10^5 J/m^3; an exchange constant of 2.10^{-11} J/m; and a spin current polarization of 0.3. The devices were found to be operational between $\approx 4\ 10^{10}$ A/m^2 and $\approx 10^{12}$ A/m^2. The switching speed depends on the applied current density and ranges from tens of nanoseconds to picoseconds.

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[1] N.S.Kim, et al., Computer, vol. 36, pp. 68-75, 2003.

[2] W. Zhao, et al., GLSVLSI’11, May 2–4, 2011, Lausanne, Switzerland

[3] M. Donahue, et al., OOMMF user’s guide, Interagency Report NISTIR 6376, version 1.0.

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