Electromigration Reliability of Solder Bumps

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Abstract

Characteristic of solder bumps is that during technology processing and usage their material composition changes. We present a model for describing a growth of intermetallic compound inside a solder bump under the influence of electromigration. Simulation results based on our model are discussed in conjunction with corresponding experimental findings.

I. Introduction

For the realization of modern three-dimensional (3D) integrated circuits new interconnect structures such as through-silicon-vias (TSVs) and solder bumps, together with complex multi-level 3D interconnect structures are gaining importance. The application of new structures and materials inevitably introduces new reliability issues. The interconnect reliability is affected by degradation processes induced by thermal gradients, electromigration (EM), and stressmigration. Solder bumps are important components for 3D integration, because they enable vertical stacking of wafers. Pure Sn has been identified as the best Pb-free solder for ultra fine pitch solder bumps for advanced 3D interconnect applications due to its baseline advantages of being electrodeposited and exhibiting a low melting temperature. Failure analyses have shown that

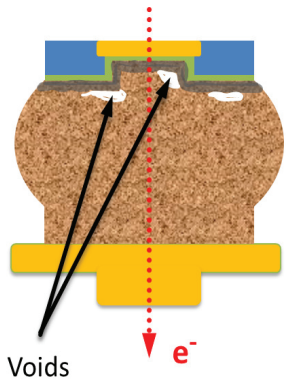

Fig. 1. EM failure is caused by voids which are formed between Ni under bump metalization (UBM) and Sn solder bump.

failures in Sn bumps occur by EM induced voiding at the interface between the intermetallic compound (IMC) and the solder (cf. Fig. 1). EM in Sn-based solder bumps is much more complicated than EM in copper due to the presence of impurities. The development of a failure in a copper interconnect takes place in two distinctive phases: a void nucleation phase and a void evolution phase. During the first phase practically no resistance increase can be measured. The situation is quite different in the case of EM failure development in a Sn bump, where an IMC layer is also present [1]. From the beginning of EM stressing a continuous growth of the bump resistance (cf. Fig. 2) is observed. After a certain period of EM stressing, the bump resistance starts to rise with a significantly steeper slope. Chen *et al.* [1] assume that the two slopes of

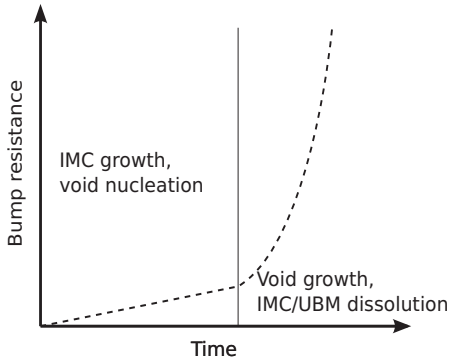

Fig. 2. Resistance change due to IMC growth and voiding with two different slopes.

the resistance growth represent two different stages of failure development: void nucleation combined with IMC growth and void propagation with IMC dissolution. The investigation of the physical mechanisms behind such a failure behavior is the main subject of this work.

Important for the layouts attached to the solder bumps is an under bump metallization (UBM), which separates the Sn bump from the surrounding metallization. The solder bump with UBM has a lower maximum current density and peak temperature in the solder, which contributes to longer EM lifetimes.

II. Physics of Intermetallic Compound Growth

The solder bump itself is usually designed and realized as an alloy, for example as SnAg, SAC405 (Sn-4% Ag-0.5% Cu) [2]. A solder bump interface to the UBM, which is usually made of Ni, is also a reason for the development of alloys in solder bumps. At this interface an IMC is formed, which is a thin layer consisting of alloys with Sn as the principal component.

Until now several attempts have been published to model EM induced IMC development [3], [4], however, none of them is applicable for numerical simulation. The growth of the IMC is determined by atomic fluxes of different material components ($\vec{J}_{Sn}$, $\vec{J}_{Cu}$, and $\vec{J}_{Ni}$). The fluxes are driven by gradients of chemical potentials (μ_{Sn}, μ_{Cu}, and μ_{Ni}) and EM. In each of the chemical potentials an impact of the local mechanical stress and the local concentration of the corresponding atom type is contained [5]:

$$\vec{J}_{Sn} = -\frac{C_{Sn}}{k_B T}\mathbf{D}_{Sn}(\nabla\mu_{Sn} - |Z^*_{Sn}|e\nabla\varphi), \tag{1}$$

$$\vec{J}_{Cu} = -\frac{C_{Cu}}{k_B T}\mathbf{D}_{Cu}(\nabla\mu_{Cu} - |Z^*_{Cu}|e\nabla\varphi), \tag{2}$$

$$\vec{J}_{Ni} = -\frac{C_{Ni}}{k_B T}\mathbf{D}_{Ni}(\nabla\mu_{Ni} - |Z^*_{Ni}|e\nabla\varphi). \tag{3}$$

$\mathbf{D}_{Sn}$, $\mathbf{D}_{Cu}$, and $\mathbf{D}_{Ni}$ are the tensorial diffusivities [6]. After Cu and Ni atoms are injected in a Sn bump, the chemical

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reactions described by the following equations take place:

$$\frac{\partial C_{Sn}}{\partial t} = -\nabla \cdot \vec{J}_{Sn} - \kappa_1 C_{Sn} C_{Cu} - \kappa_2 C_{Sn} C_{Ni} \quad (4)$$

$$\frac{\partial C_{Cu}}{\partial t} = -\nabla \cdot \vec{J}_{Cu} - \kappa_1 C_{Sn} C_{Cu} \quad (5)$$

$$\frac{\partial C_{Ni}}{\partial t} = -\nabla \cdot \vec{J}_{Ni} - \kappa_2 C_{Sn} C_{Ni} \quad (6)$$

$$\frac{\partial C_{\text{IMC1}}}{\partial t} = \kappa_1 C_{Sn} C_{Cu} \quad (7)$$

$$\frac{\partial C_{\text{IMC2}}}{\partial t} = \kappa_2 C_{Sn} C_{Ni} \quad (8)$$

(4)-(8) describe a consummation of Sn, Cu, and Ni, respectively, and a production of two types of IMCs (IMC1 = Cu_6Sn_5 and IMC2 = Ni_3Sn_4). This process is schematically illustrated in Fig. 3. The rates of the chemical reactions κ_1 and κ_2 are thermally activated parameters according to an Arrhenius law. The model assumes that all transport processes take place

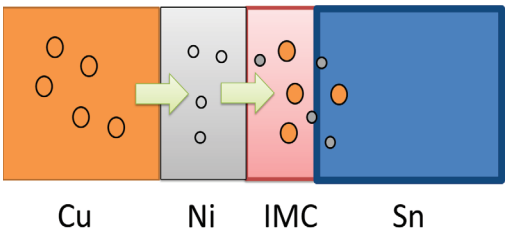

Fig. 3. EM of Cu and Ni atoms into Sn bump and the forming of IMC.

in Sn, i.e. Sn is the only transport medium in the model. However, when a thin layer of IMC is formed, impurities migrate through this layer in order to reach the Sn region, where the chemical reaction which produces the IMC occurs. Migration through the IMC for both Cu and Ni is characterized by specific diffusion coefficients and effective valences.

A. Model Parameterization and Properties of Sn

The Sn solder bump microstructure plays an important role in interconnect reliability. Compared to Cu, Sn crystallization produces 100-1000 times larger grains. Correspondingly, the role of grain boundaries as fast diffusivity paths is much more pronounced. Sn solder bumps often consist of several large Sn grains, such that most solder bumps exhibit one or at most a few Sn grain orientations [7].

Sn has a bulk tetragonal crystal structure which exhibits highly anisotropic diffusional, electrical, mechanical, thermal, and electrical properties [8].

A clear dependence of the thermo-mechanical response of a Sn solder bump on microstructure and Sn grain orientation was also observed [7]. The coefficient of thermal expansion is higher in the c-axis direction than in the a- or b-axis directions.

The isotropic diffusivity coefficient in Ni is [9]

$$D_{Ni} = 2.9 \exp\Big(-\frac{2.88\,eV}{k_B T}\Big)\frac{\text{cm}^2}{s}. \quad (9)$$

The effective valence for self-EM in Ni is, to the best of our knowledge, not available in the literature. Therefore, we use a simple estimate from the ballistic EM model [10]

$$Z^* = -n_0 l \sigma_{tr}, \quad (10)$$

where n_0 is the electron concentration, l is the electronic mean free path, and σ_{tr} is the transport cross section of the atom evaluated at the Fermi energy. By taking the values for n_0, l, and σ_{tr} from [11] we obtain an estimated $Z^*_{Ni} \approx -10$.

Measurements of self-diffusion in Sn clearly show an anisotropic atomistic transport. From [12] we have

$$D_{c,Sn} = 3.7\,10^{-8} \exp\Big(-\frac{0.25\,eV}{k_B T}\Big)\frac{\text{cm}^2}{s}, \quad (11)$$

$$D_{a,Sn} = D_{b,Sn} = 8.4\,10^{-4} \exp\Big(-\frac{0.45\,eV}{k_B T}\Big)\frac{\text{cm}^2}{s}. \quad (12)$$

The value of the self-EM effective valence in Sn has been obtained experimentally in [12]: $Z^*_{Sn} \approx -79$.

Diffusion of Ni in Sn is studied in [13] and the following values are obtained:

$$D_{c,Ni(Sn)} = 1.99\,10^{-2} \exp\Big(-\frac{0.19\,eV}{k_B T}\Big)\frac{\text{cm}^2}{s}, \quad (13)$$

$$D_{a,Ni(Sn)} = D_{b,Ni(Sn)} = 1.87\,10^{-2} \exp\Big(-\frac{0.56\,eV}{k_B T}\Big)\frac{\text{cm}^2}{s}. \quad (14)$$

For effective valence of Ni in Sn we have $Z^*_{Ni(Sn)} \approx -67$ [12].

The diffusivity coefficients (11)-(14) build diffusivity tensors which are used in (1), (2), and (3). The basic structures of the diffusivity tensors are given by

$$\bar{\bar{D}}_{Sn} = \begin{bmatrix} D^a_{Sn} & & \\ & D^b_{Sn} & \\ & & D^c_{Sn} \end{bmatrix}, \quad (15)$$

$$\bar{\bar{D}}_{Ni(Sn)} = \begin{bmatrix} D^a_{Ni(Sn)} & & \\ & D^b_{Ni(Sn)} & \\ & & D^c_{Ni(Sn)} \end{bmatrix}. \quad (16)$$

From (11)-(14) at $T = 150°\text{C}$ we have

$$\frac{D_{c,Sn}}{D_{a,Sn}} \approx 174, \quad \frac{D_{c,Ni(Sn)}}{D_{a,Ni(Sn)}} \approx 10^4. \quad (17)$$

The anisotropy of Ni diffusion in Sn is much more pronounced than the anisotropy of Sn self-diffusion.

The configurable parameters of the model are the rates of chemical reactions κ_1 and κ_2. All others parameters are obtained from measurements or theoretical calculations. The model itself allows to compute the time-dependent change of bump resistance and the thickness of the IMC layer which can also be experimentally determined and used for model calibration.

B. Intermetallic Compound Resistivity

The bump resistance increases due to void formation and microstructure changes during EM can be precisely measured with Kelvin bump probes [1]. IMCs such as Cu_6Sn_5 and Ni_3Sn_4 have a higher resistivity than pure Sn. In the case of Cu_6Sn_5, the resistivity is approximately 60% higher and in the case of Ni_3Sn_4 it is even 160% higher than the resistivity of Sn at room temperature (see Table I).

TABLE I. MATERIAL PROPERTIES AT 20 °C

Materials	Resistivity (nΩm)	Thermal conductivity (WK/m)
Cu	16.8	403.0
Ni	69.3	76.0
Sn	110.0	67.0
Cu_6Sn_5	175.0	34.1
Ni_3Sn_4	285.0	19.6

III. Simulation Results and Discussion

Model (1)-(8) has been implemented in an in-house three-dimensional simulation tool. For the EM reliability analysis

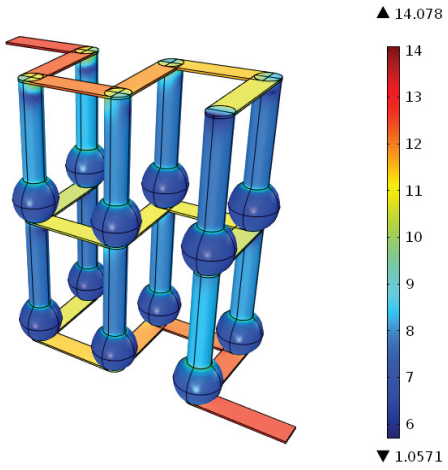

Fig. 4. Multilevel interconnect for 3D integration. Presented is the current density distribution on the logarithmic scale ($\times 10^3$A/cm^3). Wafers are removed from the picture. The copper TSV length is 100μm and the diameter chosen 25μm. The UBM thickness is 2.5μm and the bump diameter is 40μm. Due to the chosen geometry the lowest calculated current density is inside the bumps (2.66 10^3A/cm^2).

we use a multilayer interconnect structure, similar to the one usually used for wafers' stacking (cf. Fig. 4). The first step

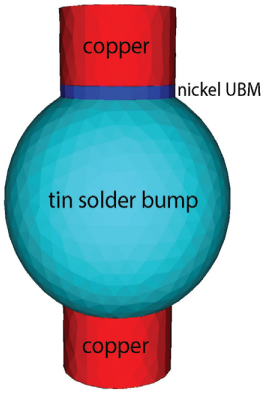

Fig. 5. Structure of the solder bump used for the study. On the top of the Sn bump a Ni UBM is placed.

is the determination of the maximal current density which is reached in some particular bump for given operating conditions (voltage, temperature) of the whole interconnect structure. In the second step the EM in a single solder bump is analyzed. In our study we have considered Ni_3Sn_4 as the primary IMC. The bump structure used in our simulation is sketched in Fig. 5.

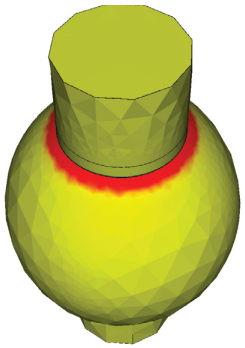

Fig. 6. IMC layer formed at the interface between a nickel UBM and a Sn solder bump.

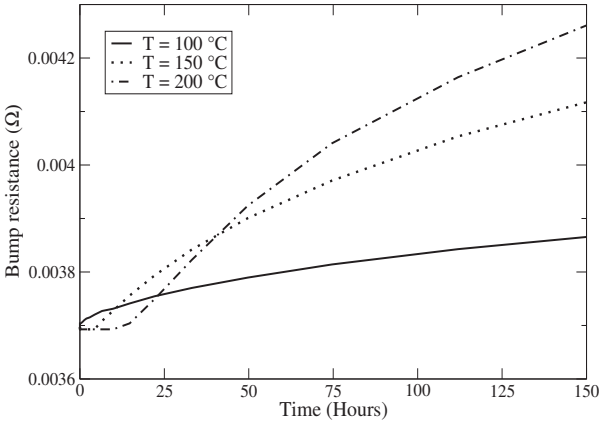

Fig. 7. Initial phase of solder bump resistance growth for three different temperatures.

The formation and growth of the IMC at the interface between the UBM and the Sn (cf. Fig. 6) is caused by several physical mechanisms. In the initial phase both Cu and Ni penetrate into the Sn bump and segregate just below the UBM/bump contact surface. Corresponding to this initial phase of EM stressing, there is an increase of the IMC's resistance as shown in Fig. 7. As expected the dynamics of IMC growth is enhanced at elevated temperatures and it is determined by the following mechanisms:

- Diffusion and EM of Cu and Ni in Sn
- Chemical reactions which convert Cu, Ni, and Sn into IMC (e.g. Cu_6Sn_5 and Ni_3Sn_4)
- Diffusion and EM of IMC in Sn

All these processes are thermally activated following Arrhenius law. Simulation allows to observe and study the interplay between the above mechanisms. As we can see in Fig. 7, in the first hours of EM stressing the resistance increase at 100°C is higher than at 150°C and 200°C. Both, migration and chemical reaction are enhanced at elevated temperature, but it seems obvious that in the early phase, migration keeps the concentration of impurities below the threshold necessary

for an IMC production which would cause an observable resistance increase. The delay in the IMC formation process can also be observed in Fig. 8.

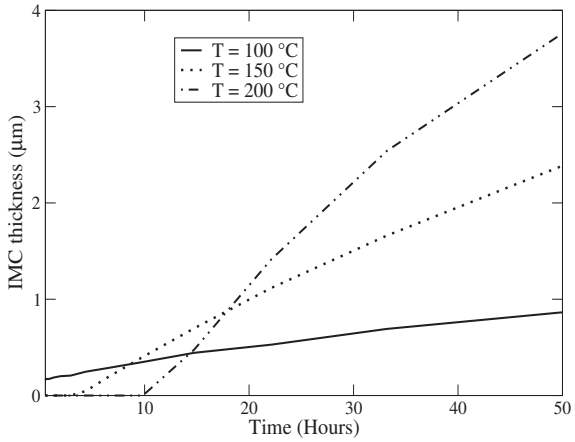

Fig. 8. Growth of IMC thickness in time. Fast migration of Cu and Ni at 150°C and 200°C prevents IMC emergence for several hours of stressing.

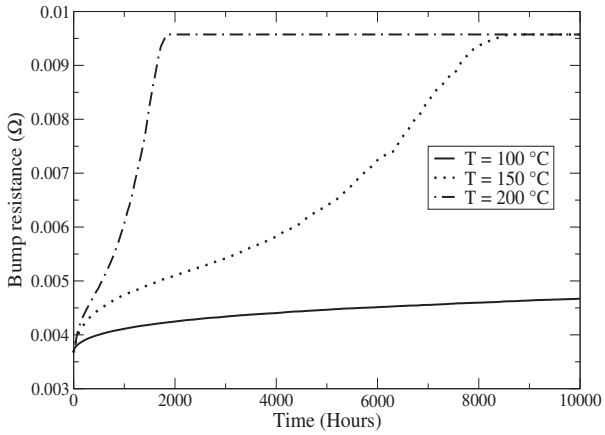

Fig. 9. Late phase of the resistance growth. The resistance of the solder bump increases, until the whole Sn is converted into IMC.

EM of vacancies ultimately leads to void formation and failure of the bump, a scenario which is most commonly observed in EM experiments [1]. However, simulation also permits to study a situation, where no void nucleation takes place but EM stressing proceeds, until the whole Sn of the solder bump is converted into an IMC. As we can see in Fig. 9 the bump resistance rises with a gradually increased slope, until the whole bump consists only of IMC (Ni_3Sn_4). From our simulation, we conclude that a much steeper second slope (cf. Fig. 2) observed by Chen *et al.* [1], which appears abruptly after approximately 100h of stressing, can only be caused by an emergence of the new phase between the IMC and the Sn layer. We support the findings of Chen *et al.* [1] that this "second phase" is actually the beginning of void evolution.

IV. Conclusion

The development of an IMC phase inside of Sn-based solders bump represents a reliability risk for interconnect structures used for realization of 3D ICs. In this work we have presented a model for IMC growth in Sn solder bumps. The model includes a description of the Cu and Ni migration into the Sn bump and the chemical reaction which produces two different types of IMCs. Simulations based on our model predict 3D profiles of the IMC, time-dependent resistance change, and time dependent change of the IMC thickness. The obtained results are utilized for explanation and discussion of experimental observations and measurements.

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