A Single-Trap Study of PBTI in SiON nMOS Transistors: Similarities and Differences to the NBTI/pMOS Case

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***Abstract*—To identify the physical mechanism behind the recoverable component of the bias temperature instability (BTI), the time dependent defect spectroscopy (TDDS) has been recently proposed and used extensively. The TDDS makes use of the fact that in nano-scale devices the recovery proceeds in discrete steps. By analyzing the statistical properties of the steps, valuable information about the BTI degradation mechanisms can be obtained. So far, most single-defect studies have focused on NBTI in SiON devices as well as PBTI in high-k gate stacks. In order to deepen our understanding of the traps responsible for this detrimental phenomenon, we focus here on PBTI in SiON nMOSFETs, which have not been studied in great detail so far. From large-area devices it is known that PBTI/nMOS is about one order of magnitude lower than NBTI/pMOS. Unlike pMOSFETs, where hole trapping is responsible for BTI, in the case of nMOSFETs electron traps have to be considered. We show here that defects causing PBTI in nMOSFETs have a similar individual trapping behavior and dependence on the bias and temperature as observed for hole traps in previous NBTI/pMOS studies. Interestingly, like in pMOSFETs, we observe switching and fixed charge traps, which allows us to adapt our previously suggested model for hole capture to electron capture in nMOSFETs.**

I. Introduction

Recent progress in semiconductor device technology has lead to nano-scale metal-oxide-semiconductor transistors (MOSFETs). As a consequence of MOSFET scaling, the bias-temperature instability (BTI) has become a major reliability issue and is observed in both pMOS and nMOS transistors whenever a positive/negative gate voltage stress (PBTI/NBTI) is applied [1, 2]. To study the recovery behavior ensuing right after the termination of stress, the recently proposed time-dependent defect spectroscopy (TDDS) is used to gain detailed insight into single defect statistics [3, 4]. Contrary to large-area MOSFETs the number of defects in nano-scale devices are reduced to a countable number [5, 6]. This allows for the analysis of individual traps using the TDDS. So far the focus of such TDDS studies has been put on defects in SiON pMOS devices [2, 4] and these defects have already been well characterized. In high-k gate stacks PBTI has been investigated at the single-defect level as well [5, 7, 8].

In our previous experiments on pMOS devices the capture and emission process were both found to be thermally activated. While all analyzed defects show a pronounced field-dependence in their capture times, their emission times can be gate bias sensitive or gate bias insensitive. The bias-dependent time constants are explained by *switching oxide traps*, whereas the bias-independent time constants are associated with so called *fixed oxide traps*. These findings raise the question whether the defects causing PBTI in nMOSFETs show a similar response to the variation of the bias conditions and temperature or not. In this work we settle this question by applying the TDDS technique to characterize electron traps in pMOSFETs.

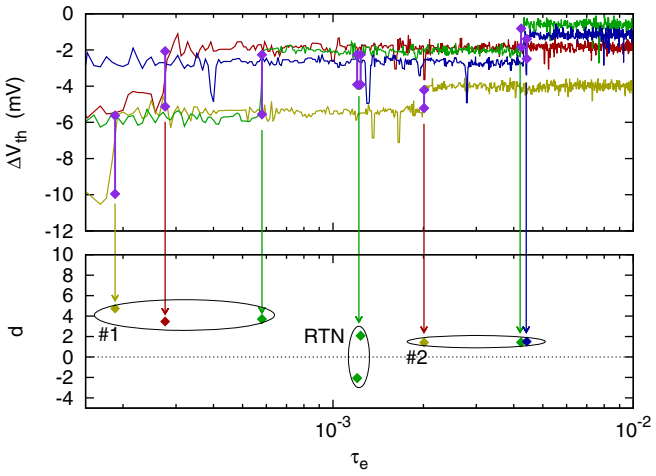

Fig. 1: In nano-scale devices the recovery after BTI stress shows discrete steps stemming from carrier capture and emission events of individual defects. The mapping of these discrete events into the (τ_e, d) plane gives the spectral map. In the spectral map the formation of clusters for each particular defect is observed. Each of the single clusters acts as a fingerprint of one individual defect. When random telegraph noise (RTN) is observed, two bands symmetrically aligned to the abscissa become visible in the spectral maps.

In contrast to large-area devices, the recovery process in nano-scale devices is of a discrete nature as single electron capture and emission events are visible as discrete steps in the drain-source current I_{DS}, which are collected in the (τ_e, d) plane called spectral map (see Figure 1). In order to gather sufficiently large statistics, the spectral maps include the detrapping events of 100 relaxation traces recorded at constant stress/recovery time, constant temperature and constant stress/recovery voltage. Within the obtained spectral maps carrier emission events of single defects, and in the case of random telegraph noise (RTN) signals also carrier capture events, are visible as clusters or as bands symmetrically aligned around the abscissa. To study the single-defect behavior within the framework of TDDS, the stress and recovery conditions are varied within wide ranges (for instance $100\,\mu\mathrm{s} \leq t_s \leq 100\,\mathrm{s}$ and $1.4\,\mathrm{V} \leq V_s \leq 2.4\,\mathrm{V}$). Quite interestingly, at certain

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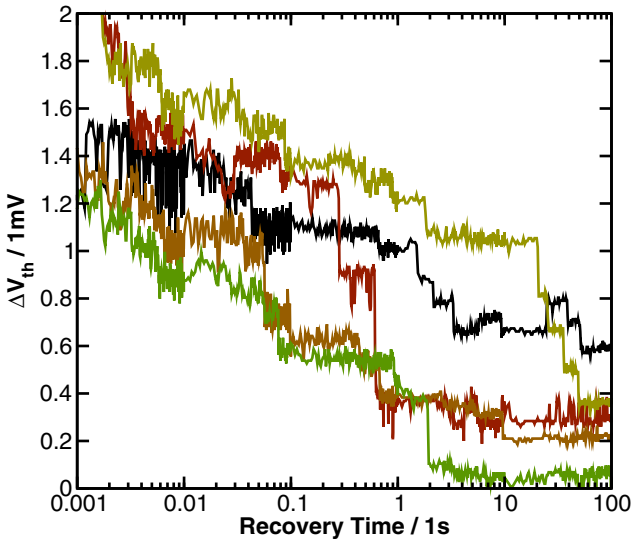

Fig. 2: Five selected recovery traces with each discrete step corresponding to the emission of a single electron. The traces are recorded on an nMOS device ($W = 0.16\mu$m, $L = 2\mu$m) after BTI stress with $t_s = 100$ s and $V_s = 2.2$ V. As clearly visible, for the investigated device the heights of the discrete steps are in the range of $\Delta V_{th} \approx 0.2$ mV and lower, a consequence of the relatively large device area. Such step heights are equivalent to drain-source current fluctuations below 1 nA and increase the experimental effort. As in the NBTI/pMOS case, both capture and emission events are visible as discrete steps in the recovery traces and are distributed over a large time scale.

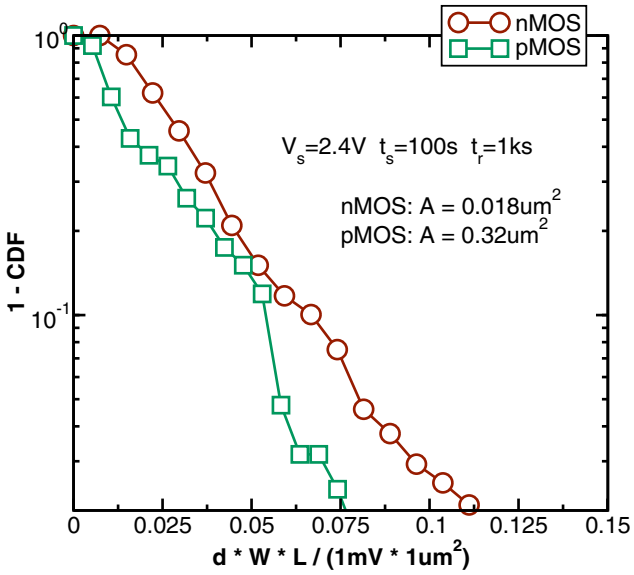

Fig. 3: The complementary cumulative distribution function of the step heights multiplied by the gate area $A = W \times L$ is depicted for nMOSFETs and pMOSFETs of the same technology (SiON oxide with an EOT of 2.2 nm). The CDFs of the normalized step heights have a similar shape so that the defects in both devices are expected to have the same spatial depth distribution within the oxide. As a further consequence, traps causing PBTI in nMOSFETs have a similar electrostatic impact on the conducting channel as observed in pMOSFETs when NBTI is studied. The above statistics are extracted from recovery traces with $t_r = 1$ ks of several devices after oxide stress conditions of $V_s = 2.4$ V for $t_s = 100$ s.

temperatures and bias conditions single defects start to produce RTN when the carrier capture and emission times τ_c and τ_e are about the same order of magnitude, $\tau_c \approx \tau_e$. This allows to predict the conditions for RTN from the extracted capture and emission time constants at that particular voltage [9].

II. Experimental

The most important requirement for the devices which can be used for the purpose of studying single defects with TDDS is that they have to show just a handful of defects. This is necessary for the separation of the individual emission events belonging to different defects in the recovery traces. As a very high number of defects are present in large-area devices the single electron emission events can not be resolved in a measurement. It has been reported, that pMOSFETs show a higher trap density than their nMOSFET counterparts ($N_{pMOS} \approx 10 \times N_{nMOS}$) [2, 10]. As a consequence, just a few carefully selected nano-scale nMOSFETs would show a reasonable number of defects visible in the recovery traces. To efficiently apply the TDDS for our PBTI/nMOS measurements we choose a device with a larger gate area of $A_{pMOS} \approx 10 A_{nMOS}$ compared to our previous studies [11–13]. It has to be noted, however, that the larger the gate area the smaller the threshold voltage shift ΔV_{th} due to single capture or emission events becomes, as visible in the traces recorded on a larger area device from Figure 2.

In the following the response of electron traps to PBTI stress conditions is studied in a nano-scale nMOSFET (W = 160 nm, L = 2000 nm, EOT = 2.2 nm) for various bias conditions and temperatures in detail. The stress voltages are varied in the range of $1.4\,\text{V} \leq V_s \leq 2.2\,\text{V}$, the stress times between $100\,\mu\text{s} \leq t_s \leq 100\,\text{s}$, and the device temperature from 50°C up to 80°C. In order to collect a statistically relevant amount of data, the device is repeatedly stressed and the recovery behavior, see Figure 2, is recorded and analyzed [14].

To check the statistical relevance of the different observed step heights, the cumulative distribution function (CDF) of several different nMOSFETs (W = 160 nm, L = 2000 nm) and pMOSFETs (W = 150 nm, L = 120 nm) of the same technology have been contrasted in Figure 3. To account for the dependence of the step heights on the geometry, the CDF distribution of the step heights is multiplied by the gate area $A = W \times L$.

In order to cope with the small steps in ΔV_{th} a high measurement resolution is required. Our TDDS setup has a very high current measurement resolution (down to approximately 10 pA) which allows us to analyze devices even up to $A = 0.6\,\mu\text{m}^2$ at $V_{DS} = 100$ mV down to $V_r = 200$ mV. The setup developed to record the recovery traces measures the drain-source current I_{DS}. In a post-processing step the initial ΔV_{th} traces are obtained by converting the I_{DS} using the $I_D\,(V_G)$ characteristics.

Furthermore, the CDF in Figure 3 demonstrates that the step heights in nMOS SiON transistors also roughly follow an

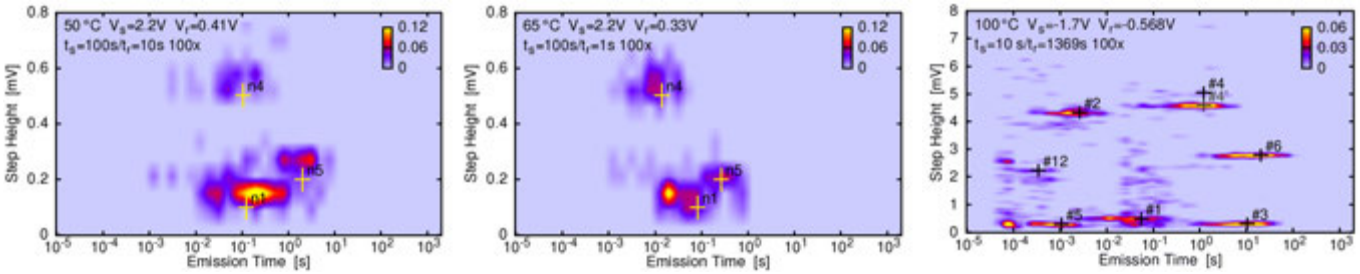

Fig. 4: The nMOS transistor (W = 160 nm, L = 2000 nm) used for this study shows a handful of defects. The individual defects identified by clusters in the above spectral maps move towards lower emission times when the device temperature is increased (50°C **left**, 65°C **middle**). Compared to previous studies on NBTI/pMOS (W = 150 nm, L = 120 nm) [15] (**right**), defects observed in PBTI/nMOS experiments show a similar response to the device temperature. Note that the single defects show very small step heights due to the investigated device area posing a challenge to the experimental design. From the three defects identified (n_1, n_4, n_5), n_1 and n_4 are studied in more detail here.

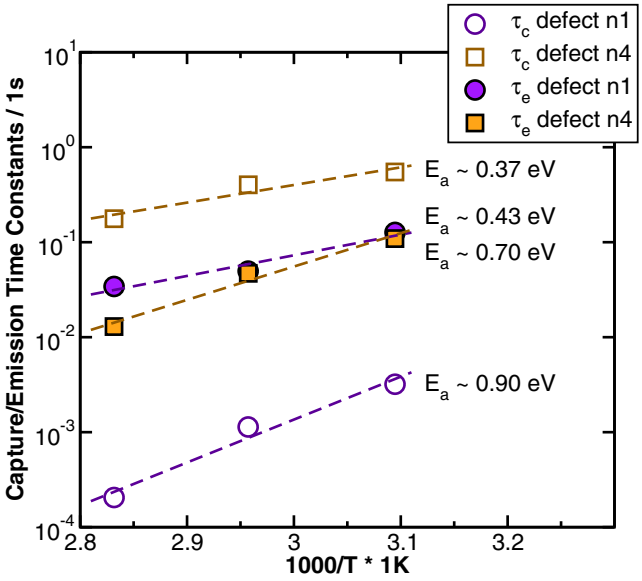

Fig. 5: The temperature dependent capture and emission time constants recorded after BTI stress with $V_s = 2.2$ V and $t_s = 10$ s are visualized in an Arrhenius plot. Just like in pMOSFETs, the temperature dependence of the capture and emission times of the selected defects n_1 and n_4 are extracted by approximation of the behavior by an Arrhenius law. The particular activation energies E_a assume similar values compared to those observed for pMOSFETs. [13].

exponential distribution, similar to defects causing NBTI in pMOS transistors. As a consequence, the defects in nMOS and pMOS devices are expected to have a similar spatial distribution within the oxide.

III. Results

In the investigated pMOSFET, three defects, namely n_1 with $\tau_e \approx 100$ ms and $d \approx 0.15$ mV, n_4 with $\tau_e \approx 100$ ms and $d \approx 0.48$ mV, and n_5 with $\tau_e \approx 1$ s and $d \approx 0.26$ mV could be identified in the spectral map of Figure 4 at 50°C, at a recovery voltage of $V_r = 0.41$ V after stressing the device at $V_s = 2.2$ V. Both the capture and emission processes are found to be temperature dependent. This is visible in Figure 4 where the single clusters move towards lower emission times for increasing temperature, c.f. Figure 4 left and middle. Additionally, new defects can be shifted into the measurement window at higher temperatures. This is in agreement with the fact that electron emission is strongly thermally activated, similarly to NBTI/pMOS experiments [4]. From the spectral maps from Figure 4 it can be concluded that a very high measurement resolution is necessary. This is especially the case for defect n_1 with a step height of $d \approx 0.15$ mV.

In Figure 5 the Arrhenius plot of the defects n_1 and n_4 is shown when the device temperature T is varied between 50° C and 85°C. The thermally induced change of the capture and emission times of the defects n_1 and n_4 are approximated by an Arrhenius law with activation energies E_a in the range of $0.37\,\text{eV} \leq E_a \leq 0.9\,\text{eV}$ for both electron capture and emission. In previous studies [4] activation energies E_a for pMOSFETs have been found to be within the same range. This indicates, that defects causing PBTI on nMOSFETs follow the same temperature-activated mechanism as the defects causing NBTI on pMOSFETs.

IV. Modeling

We have recently proposed a four-state non-radiative multiphonon (NMP) model to explain the complex capture and emission behavior of single defects in pMOSFETs [4]. In particular, this model, c.f. Figure 6, correctly predicts the response of these defects to various stress and recovery conditions. In our initial efforts, this hole trapping model was developed around the oxygen vacancy, one of the most studied defects in silica [16]. The chemical nature of the BTI defect is still controversial [17–19] and many possible defect candidates have been suggested over the years. For NBTI the oxygen vacancy must be discarded as a possible hole trap due a too low trap level [19]. Nevertheless, this defect might be an electron trap in PBTI as shown in the DFT studies of Kimmel et. al. [20].

Basically, the four-state NMP model consists of two stable states 1 and 2 and two metastable states $1'$ and $2'$. The metastable states provide an explanation for the bias-independent emission times (state $2'$), as observed for *fixed charge traps*, as well as the *switching trap* behavior (state $1'$) showing bias-dependent emission time constants. To account for electron trapping instead of hole trapping the two positively charge states $2'$ and 2 are now considered negatively

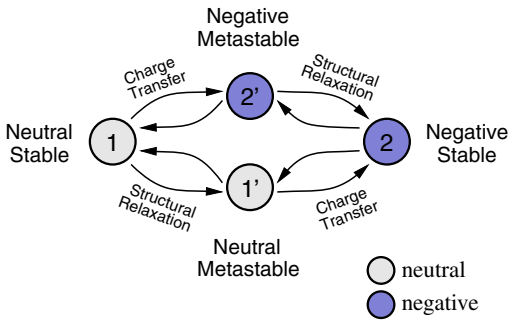

Fig. 6: The four-state non-radiative multiphonon (NMP) model consists of two stable states 1 and 2 (orange) and two metastable states $1'$ and $2'$ (grey). Charge transfer reactions are modeled using non-radiative multiphonon theory and correspond to the actual charge capture and emission processes ($1 \rightarrow 2'$ and $1' \rightarrow 2$). These charge transfer reactions are always accompanied by thermal transitions ($1 \rightarrow 1'$ and $2' \rightarrow 2$). Therefore the full capture and emission process involves the metastable states $1'$ and $2'$ which give an explanation for the bias-dependent as well as the bias-independent emission times, respectively.

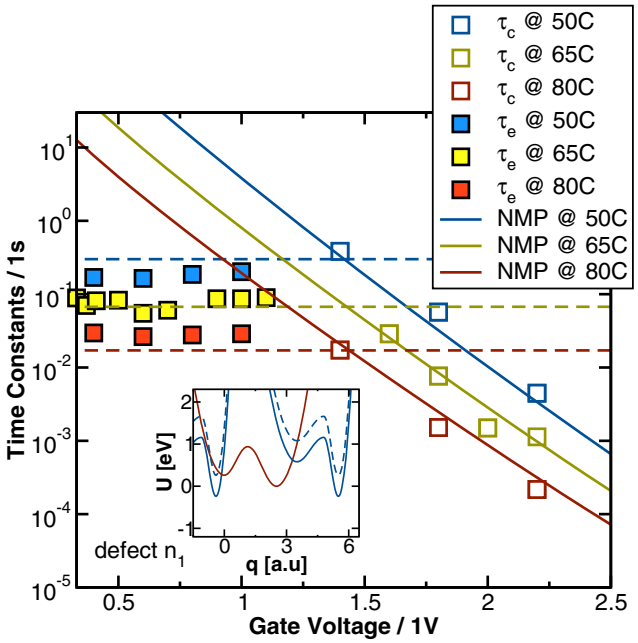

Fig. 7: The gate voltage dependence of the capture time τ_c and the emission time τ_e for defect n_1. The emission time appears to be independent of the applied bias (fixed charge trap) whereas the capture time shows a significant dependence. Good agreement between data (symbols) and model (lines) is obtained. The inset shows the configuration coordinate diagram of the NMP model.

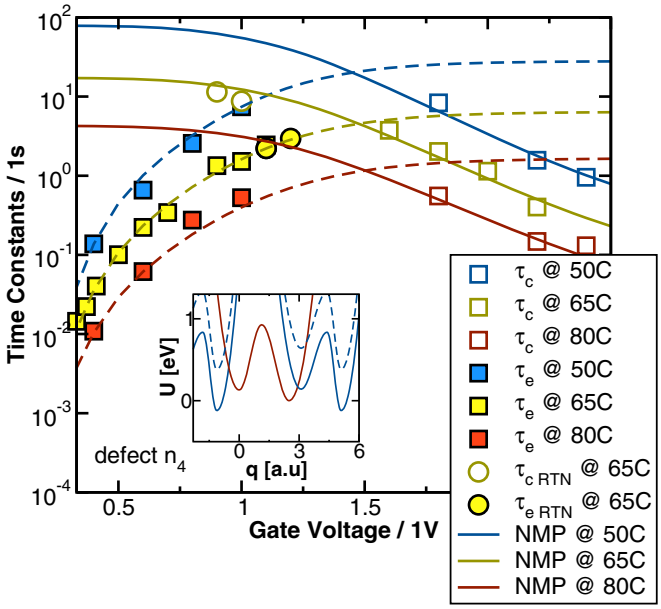

Fig. 8: Contrary to defect n_1, the emission time of defect n_4 shows a very strong dependence on the gate voltage (switching trap). Just like the fixed charge trap behavior, the switching trap behavior can be well explained by the four-state NMP model (lines). The inset shows the configuration coordinate diagram of the NMP model.

charged. Apart from this modification the trapping dynamics are described by the same set of rate equations.

For nMOSFETs, the electron capture and emission events are described by a transition from the neutral stable state 1 to the negatively charged metastable state $2'$. From there, a field independent but thermally activated structural relaxation leads to the negatively charged stable state 2. Electron emission can proceed in the opposite direction from state 2 to state 1, where the two-step transition can take the pathway over the state $1'$ or $2'$. In the voltage regime of interest, the transition $2 \rightarrow 2' \rightarrow 1$ is gate bias-independent, while the transition $2 \rightarrow 1' \rightarrow 1$ is gate bias sensitive. This transition back to state 1 involves an electron emission event, visible as a discrete step in I_{DS}, i.e. the ΔV_{th}.

Out of the three identified defects, c.f. Figure 4, two defects, namely n_1 and n_4, are studied in detail. The first defect n_1 shows a bias-independent emission time which is characteristic for a *fixed charge trap* while defect n_4 shows the typical *switching trap* behavior with a gate bias-dependent emission time at small recovery voltages V_{r}. For the latter one the emission time becomes bias-independent towards higher recovery voltages, c.f. Figure 8.

An evaluation of the model against the experimental TDDS data is given in Figure 7 and Figure 8. The capture time τ_c of the defects n_1 and n_4 depends exponentially on the stress recovery gate voltage V_{r} and shows a strong temperature dependence. However, the emission times of the defects n_1 and n_4 show a completely different response to varying recovery voltages. On varied temperature both defects n_1 and n_4 show a similar temperature activation, c.f. Figure 5, Figure 7, and Figure 8. The emission time of n_1 is independent of the applied recovery bias and remains constant over a wide recovery voltage range, c.f. Figure 7. Quite to the contrary, the observed emission times of defect n_4 show a strong recovery voltage dependence. Towards higher gate voltages the emission times τ_e saturate and become bias-independent.

As recoverable BTI and random telegraph noise (RTN) is apparently caused by the same defects [21, 22], the bias-conditions under which RTN from particular defects is expected, becomes predictable [4, 9]. As mentioned previously, only defects having emission times τ_e within the measurement window t_r ($\tau_e < t_r$), can be studied using TDDS. In order

to observe RTN, both the capture and emission time τ_c and τ_e and also their sum have to be smaller than the TDDS measurement window $\tau_c + \tau_e \ll t_r$. Otherwise the electron capture and emission events of the RTN signal do not lie inside the measurement window. For instance, for defect n_4 the capture time constants in the gate voltage range of $1.0\,\mathrm{V} \leq V_G \leq 1.2\,\mathrm{V}$ at $T = 65°\mathrm{C}$ (yellow circles from Figure 8) are extracted from an RTN signal. These RTN signals are observed for $\tau_e \approx \tau_c$. That is the case near the intersection point of the capture and emission times estimated by the NMP model.

V. Conclusions

By studying PBTI on SiON nMOSFETs at the single-defect level we have demonstrated a number of similarities between electron trapping in nMOS and hole trapping in pMOS transistors. Particularly noteworthy are the strong bias-dependence of the capture and emission times, *switching* vs. *fixed charge* behavior, as well as relatively large thermal activation energies. This suggests that NBTI and PBTI originate from the same physical process in nMOSFETs and pMOSFETs. As a result, the different magnitude of degradation must be ascribed to the different trap concentration or due to energetically lower trap levels. Finally, we showed that the kinetics of electron capture and emission can be well described by our four-state defect model previously employed for hole capture in pMOSFETs.

VI. Acknowledgment

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