Effects of Sidewall Scallops on the Performance and Reliability of Filled Copper and Open Tungsten TSVs

Lado Filipovic, Roberto Lacerda de Orio, and Siegfried Selberherr
Institute for Microelectronics, Technische Universität Wien
Gußhausstraße 27-29/E360, 1040 Wien, Austria
{filipovic|orio|selberherr}@iue.tuwien.ac.at

Abstract

The effects of the presence of scallops along the sidewalls of filled (copper) and open (tungsten) TSVs are studied. The Bosch process is used in order to generate highly vertical deep trenches; however, the process results in scallops along the etched sidewalls. A model for the Bosch process is implemented in an in-house level set simulator in order to generate various TSV structures with small and large sidewall scallops. The resulting geometries are imported into a finite element tool in order to analyze the performance and reliability of the devices. The electrical parameters of the TSVs are shown to vary when scallops are present for both types of TSVs. In addition, the maximum thermo-mechanical stress increases in the presence of scallops, while the average stress along the interfaces remains relatively unchanged. Electromigration analyses were also performed on the structures in order to determine stress development during the early stages of operation. It was found that the filled TSV with scalloped sidewalls experiences a higher current density and suffers from increased stress, while the sidewall scallops do not cause variation in the stress of open tungsten TSVs. The open tungsten TSVs experience most Electromigration-induced stress in the connecting metal layers and not along the sidewall.

I. Introduction

The microelectronics manufacturing industry has aggressively scaled devices with "more Moore" integration over the last decades. The increased process equipment and factory costs for scaling are expected to limit scaling at the 6nm node [1]. Recently, a great amount of effort has been directed towards adding more functionality to applications beyond memory and logic, deemed "more than Moore" integration. A major development in this direction is the through-silicon via (TSV), a three-dimensional integration technology which allows for the fabrication of systems connecting various technologies, dense device packing, lower power consumption, and reduced RC delay [2]. The two main methods to etch the silicon layer for TSV implementation are the Bosch process and plasma etching [1].

Each silicon etching method has its own flaws and reliability concerns. Problems specific to the Bosch process are a rough, scalloped TSV sidewall, notch formation at the TSV bottom, and potential step coverage issues relating to depositing layers on a scalloped wall [3]. The etching of deep trenches using an ion-enhanced plasma, such as SF_6/O_2, results in significant sidewall tapering, making the formation of deep vertical trenches a challenge [4]. This work compares, through simulations, the electrical and reliability properties of filled copper TSVs with an aspect ratio of 1:11 as well as open tungsten TSVs with a geometric aspect ratio of 1:3. The effects of the scallops along the length of the TSV sidewalls for each type of via is analyzed using simulations of electrical performance, thermo-mechanical stress after a 300°C temperature drop, and the electromigration (EM) induced stress while operating at a current of 1A for an extended period of time. Non-scalloped structures with the same aspect ratios have been used in order to extract model parameters which successfully replicate experimental measurements.

II. Silicon Etching using the Bosch Process

In order to generate the TSV profiles, an in-house process simulator is used. The simulator is implemented using the level set framework and it is capable of simulating a sequence of processing steps, including etching and deposition [5]. The Bosch process is performed in order to etch deep trenches in silicon using multiple cycles of polymer deposition and polymer/silicon etching.

The first step of a Bosch process cycle involves the deposition of a thin chemically inert polymer layer, usually in a C_xF_x gas environment. The subsequent etching step is performed in an ion-enhanced plasma environment, usually using SF_6 gas. The polymer protects the structure from the chemical etching, while the ions attack the polymer layer at the trench bottom. This results in an exposure of the substrate at the bottom, where chemical etching can then proceed, while the sidewalls are still protected.

TABLE I. ETCH PARAMETERS FOR THE TWO TYPES OF TSVS IN ORDER TO GENERATE SMALL AND LARGE SCALLOPS ALONG THE SIDEWALL

			Cycle time (sec)	
	Rate	**Etch ratio**	**Small**	**Large**
Deposition	10nm/sec	-	4	12
Si etch isotropic	39nm/sec	Si:mask 80:1 Si:poly 13:1	11.2	33.6
Si etch directional	20nm/sec	Si:mask 80:1 Si:poly 2:1		
Resulting scallop height:			480nm	1.45μm
Total number of dep/etch cycles (Cu):			120	40
Total number of dep/etch cycles (W):			520	173

The parameters used to investigate the etched profile of the TSVs are listed in Table I. For both types of TSVs two simulations are performed in order to generate structures with small and large sidewall scallops, with scallop heights of 48nm and 1.45μm, respectively. The filled copper TSVs have a depth of 58μm, requiring 120 and 40 cycles for a complete etch, while the tungsten TSVs have a 250μm depth, requiring 520 and 173 cycles, in order to generate the small-scalloped

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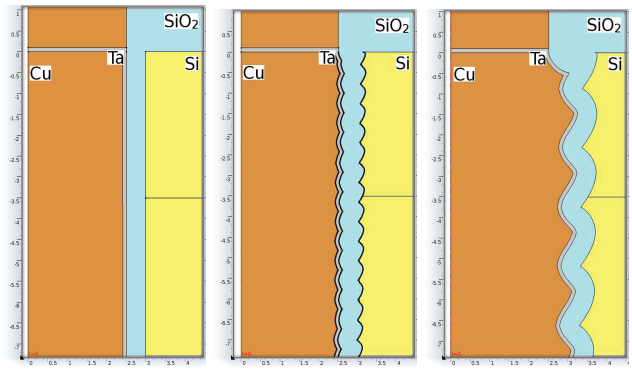
and large-scalloped structures, respectively. Each structure is imported into a finite element simulator, where its performance is compared to that of an ideal, flat-sidewalled TSV.

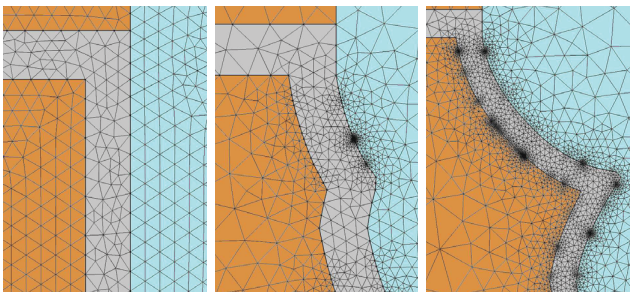
A. Generating the Filled Copper TSVs

After the silicon etching step, several deposition steps are necessary to generate the full TSV. For the filled copper TSVs, an isotropic model is implemented in order to deposit a 500nm layer of SiO_2 along the etched walls for electrical isolation. In addition, a 100nm layer of tantalum is deposited to serve as a barrier to potential copper diffusion into the substrate. The resulting size of the TSV is approximately $5\mu m \times 58\mu m$, which can be filled without appearing seam voids, using electrochemical deposition of Cu with chemical vapor deposition of tungsten and a sputter TiW/Cu seed layer [6]. A profile of the top of the TSV structure is shown in Fig. 1, while an enlarged section showing the mesh used for finite element analysis is shown in Fig. 2. The meshed structure is imported into a finite element tool for electrical and reliability analysis.



(a) Flat sidewalls (b) Small scallops (c) Large scallops

Fig. 1. Materials at the top of the three filled copper TSVs. The backside (bottom) of the structure is also connected to a copper layer, through a tantalum liner.

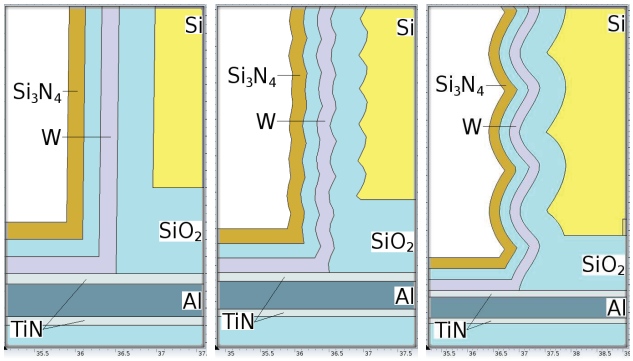


(a) Flat sidewalls (b) Small scallops (c) Large scallops

Fig. 2. Mesh at the top of the three filled copper TSVs. The image is an enhanced section from Fig. 1 where the oxide, copper, and tantalum layers are visible.

B. Generating the Open Tungsten TSVs

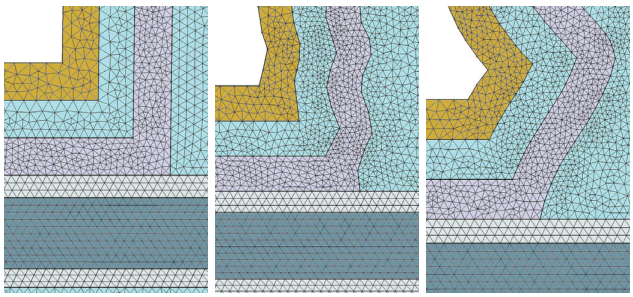
The open TSV does not require an electrochemical deposition step, but several material depositions are needed along the trench surface in order to generate the final TSV structure. For the tungsten TSVs a 500nm layer of SiO_2 is deposited along the etched walls for isolation, followed by a 100nm layer of tungsten, an additional 100nm layer of SiO_2, and a 100nm Si_3N_4 liner. An isotropic model is once again used for the deposition steps. The resulting sizes of the TSVs are approximately $80\mu m \times 250\mu m$. The bottom profile of the tungsten TSV structure is shown in Fig. 3.



(a) Flat sidewalls (b) Small scallops (c) Large scallops

Fig. 3. Bottom of the three open tungsten TSVs with materials labeled. A variation in sidewall scallop height and width is evident.

A very fine mesh is required in order to properly simulate the device performance using finite element methods. An enhanced section of the TSV bottom, where the thin material layers of silicon nitride, oxide, tungsten, titanium nitride, and aluminum can be seen with their meshed elements, is shown in Fig. 4.



(a) Flat sidewalls (b) Small scallops (c) Large scallops

Fig. 4. Mesh at the bottom of the three filled copper TSVs. The image is an enhanced section from Fig. 3 where the oxide, tungsten, titanium nitride, aluminum, and silicon nitride layers are visible.

It is worthwhile noting that the structures generated with small scallops experience a slight sidewall tapering (89%) while the large-scalloped structures show almost perfectly vertical walls. Therefore, when comparing the structures to ideal flat-sidewalled TSVs, it is important to differentiate which characteristics are influenced by the sidewall tapering and which are influenced by the sidewall scallops themselves. Additionally, the large-scalloped structures experience more lateral etching, making the trench wider than the flat, ideal, cylindrical trench.

C. Electromigration - Void Nucleation Model

The model used in order to calculate the electromigration-induced stress through the TSV metal layers is given in [7]. The stress is used to detect early failures in metal lines, when compared to a critical stress, which is a material-dependent property. The total vacancy flux is given by

$$\vec{J_v} = -D_v \left(\nabla C_v + \frac{eZ^*}{kT} C_v \rho \vec{j} - \frac{Q^*}{kT^2} C_v \nabla T + \frac{f\Omega}{kT} C_v \nabla \sigma \right), \quad (1)$$

where D_v is the vacancy diffusivity, C_v is the vacancy concentration, e is the elementary charge, Z^* is the effective charge, ρ is the metal resistivity, $\vec{j}$ is the current density, Q^* is the heat of transport, f is the vacancy relaxation ration, Ω is the atomic volume, and σ is the hydrostatic stress.

The accumulation and depletion of vacancies is found according to the continuity equation

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J_v} + G, \quad (2)$$

where G is a given surface function which models vacancy annihilation and generation. The vacancy transport results in the creation of mechanical strain

$$\frac{\partial \varepsilon}{\partial t} = \Omega \left[(1-f) \nabla \cdot \vec{J_v} + fG \right], \quad (3)$$

where ε is the trace of the strain tensor, which is applied to a mechanical simulation using a linear elastic model for copper. The stress resulting from the mechanical simulation, with the strain applied, gives the EM-induced stress.

III. Performance and Reliability of the Copper TSVs

Using finite element tools, the performance and reliability of the simulated TSVs have been analyzed. The parasitic capacitance between the metal layer and the bulk silicon for each TSV is shown in Fig. 5. Even though the TSVs' depths are identical and the deposited oxide thickness is 500nm for each structure, there is some variation of the low-frequency capacitance values. However, at high frequencies, as the device enters the resistive mode of operation, the capacitance between the TSVs does not vary significantly.

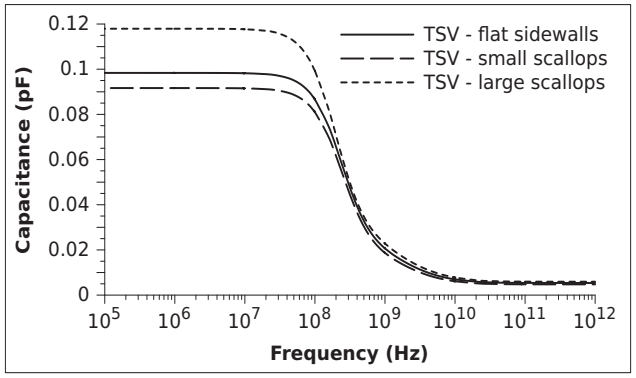


Fig. 5. Frequency-dependent capacitance (pF) for the three filled copper TSVs shown in Fig. 1.

The extracted capacitance, inductance, and TSV resistance are given in Table II. A copper electrical conductivity of 5.9987×10^7S/m (at 20°C) with a temperature-dependent resistivity of $0.0043°C^{-1}$ is used [8]. Relative permittivities of oxide and silicon, used for the capacitance simulation, are 4.2 and 11.7, respectively.

TABLE II. ELECTRICAL RESULTS INCLUDING RESISTANCE, CAPACITANCE, AND INDUCTANCE FOR THE FILLED COPPER TSV

	Flat	Small scallops	Large scallops
Resistance	116$\mu\Omega$	135$\mu\Omega$	98.8$\mu\Omega$
Capacitance	98.35pF	91.65pF	117.92pF
Inductance	3.88fH	3.25fH	5.06fH

The resistance appears to increase for the small-scalloped structure, which is due to the tapered sidewalls during etching. The tapering results in a smaller copper volume and less area through which the current flux can propagate. The structure with large scallops shows a reduced resistance, while capacitance is significantly increased. The reduced resistance is due to the longer lateral etching time during processing, which resulted in a larger TSV diameter. The increased capacitance can be attributed to the thinning which occurs during oxide deposition around the large scallops. As scallops switch between convex and concave during material deposition, there is not a uniform thickness throughout the oxide, but rather regions of slightly thinner and slightly thicker oxide around each scallop.

A. Thermo-Mechanical Stress

The thermo-mechanical stress was analyzed for each structure by applying a ΔT=300°C (temperature drop from 320°C to 20°C). Assuming a stress-free temperature of 320°, this analysis is meant to simulate the structure cooling after a thermal processing step. The stress builds up in the structures due to the variation in the coefficient of thermal expansion (CTE) between adjoining materials. The variations in the CTEs between different materials relevant for both the filled copper TSV and open tungsten TSV are shown in Table III. A linear elastic model is used for the metal layers during the mechanical simulation.

TABLE III. COEFFICIENTS OF THERMAL EXPANSION FOR ALL RELEVANT MATERIALS

Material	Cu	W	Ta	SiO_2	Si	Si_3N_4
CTE (10^{-6}/K)	16.5	4.5	6.3	0.5	2.6	2.3

The maximum stress increases in the presence of scallops, while the average stress along the interfaces remains relatively unchanged. Fig. 6 shows the stress distribution along one-dimensional radial cut lines through the middle depth of the TSVs. The peak stresses observed in the scalloped structures correspond to the pinched area between two scallops. The pinched region between scallops absorbs the stress from the surrounding area, so that the stress is not uniform, as in the case of the flat TSV. The top of Fig. 6 shows the stress through a one-dimensional cut line going through a location where the scallops at the copper/tantalum and tantalum/oxide interfaces are pinched. Therefore, the Cu/Ta and Ta/SiO_2 interfaces experience a spike in the thermo-mechanical stress. The bottom of Fig. 6 shows the stress where the scallops at the oxide and silicon interface are pinched. Similarly, the spike in thermo-mechanical stress is noted at the SiO_2/Si interface.

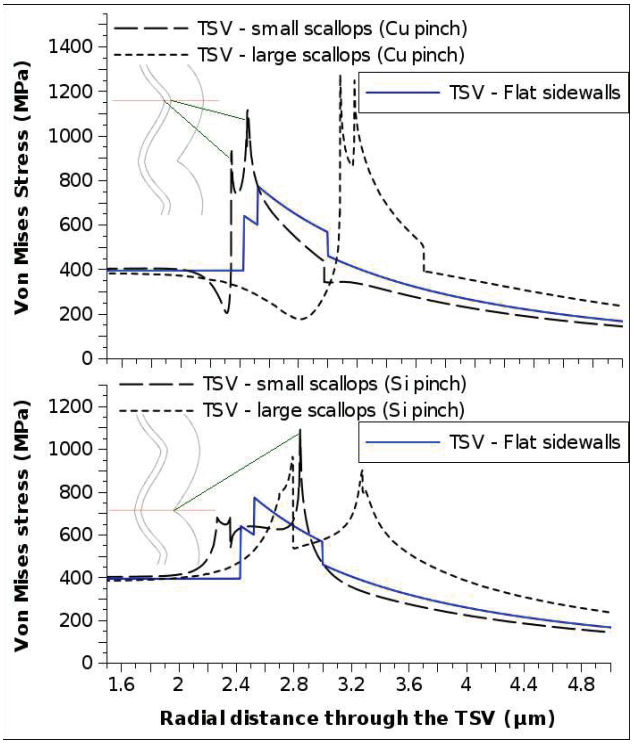
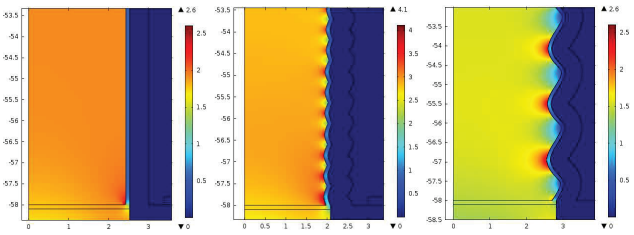


Fig. 6. Von Mises stress through the vertical middle of the filled copper TSVs assuming a drop from a stress-free temperature of 320°C to 20°C.

B. *Electromigration-Induced Stress*

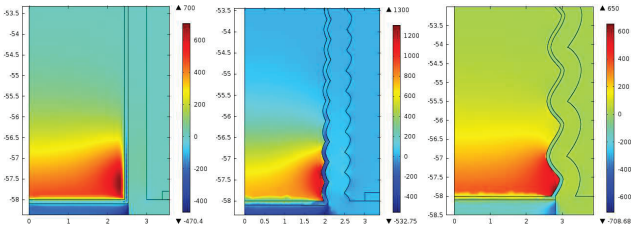
Electromigration analyses were performed on the structures using a model presented in [7], with the resulting current density and EM-induced stress through the structures shown in Fig. 7 and Fig. 8, respectively. The increased current density along the scallop edges can be attributed to the thinning of the metal structure at the sidewalls due to tapering during processing, forcing more current to flow around the scallops.



(a) Flat sidewalls (b) Small scallops (c) Large scallops

Fig. 7. Current density distribution (MA/cm^2) in the three filled copper TSVs when a 1A current is applied through the top of the structure.

The stress in Fig. 8 is generated after operating the device at 1A for approximately 700hrs. The growth of the maximum EM-induced stress during the time-dependent simulation is shown in Fig. 9. The EM weakness at the bottom of the structure is due to the current flow being directed from the top, while the ground node is at the bottom. The vacancies build up around the anode end of the TSV at Cu/capping layer



(a) Flat sidewalls (b) Small scallops (c) Large scallops

Fig. 8. Electromigration-induced stress (MPa) accumulation at the bottom of the three filled copper TSVs when a 1A current is applied through the top of the structure for 700hrs.

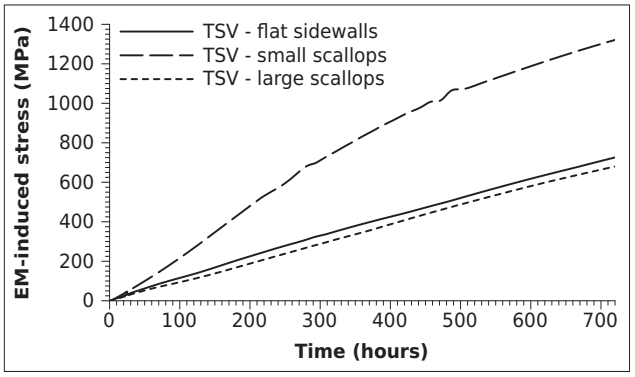


Fig. 9. Maximum EM-induced stress (MPa) through the filled copper TSVs during operation at a 1A current.

interface [9], which is at the TSV bottom in the given example.

The TSV with small-scalloped sidewalls experiences the highest current density through the copper because of the tapered sidewalls, resulting in a thinning metal layer. The increased current density leads to an increase in the vacancy concentration as given in (1), while the increased vacancy concentration results in an increased stress as given in (3). The flat TSV and the TSV with large-scalloped sidewalls display a very similar EM response. The large-scalloped TSV experiences the lowest stress due to its increased width, discussed earlier. The increased width results in a reduction in the current density, which in turn reduces the vacancy flux and stress generation.

IV. Performance and Reliability of the Tungsten TSVs

A similar analyses to that given for the performance and stress generation for filled copper TSVs is performed for open tungsten TSVs. The parasitic capacitance between the metal layer and the bulk silicon for each TSV is shown in Fig. 10. Once again, variation is observed in the low-frequency capacitance values, especially in the case of the large-scalloped TSV structure, while the high-frequency capacitance does not vary significantly.

The extracted capacitance, inductance, and TSV resistance are given in Table IV. The presence of scallops results in an increased resistance and inductance, with the values increasing further when the scallop size is increased. This increase occurs because the tungsten, which is deposited on top of a scalloped sidewall, will have a longer effective length through which

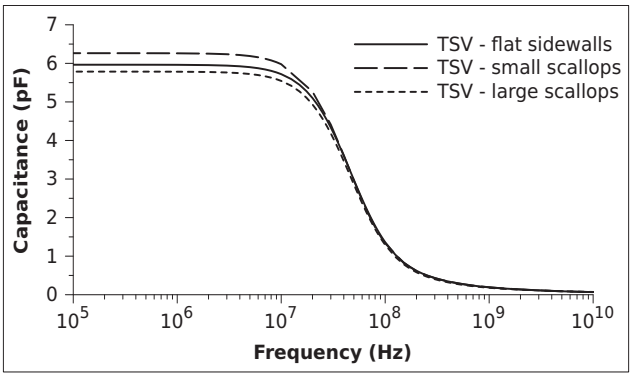


Fig. 10. Frequency-dependent capacitance (pF) for the three open tungsten TSVs shown in Fig. 3.

TABLE IV. ELECTRICAL RESULTS INCLUDING RESISTANCE, CAPACITANCE, AND INDUCTANCE FOR THE OPEN TUNGSTEN TSV

	Flat	Small scallops	Large scallops
Resistance	409mΩ	426mΩ	473mΩ
Capacitance	5.96pF	6.26pF	5.79pF
Inductance	3.49pH	3.61pH	3.86pH

current flows. The increased current path leads to an increased overall TSV resistance. The electrical conductivities of tungsten and aluminum used in this simulation are 1.3×10^7S/m and 3.5×10^7S/m, respectively. These values resulted in a good agreement with measured results for similar structures in [10]. The signal loss through the structure is also shown in Fig. 11, where no major variation can be observed between the tested structures as well as the structure measured in [10].

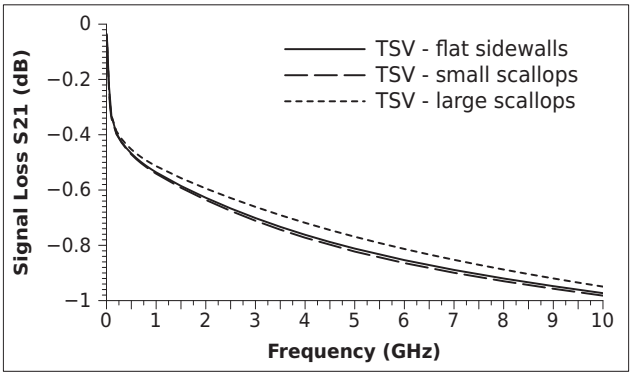


Fig. 11. Frequency dependence on the signal loss S21 (dB) for the three open tungsten TSVs. A higher loss is noted at high frequencies for the large-scalloped structure.

A. Thermo-Mechanical Stress

The thermo-mechanical stress build-up in the open tungsten TSV was also analyzed with a cool-down after a thermal processing step at a stress-free temperature of 320°C to 20°C. The CTEs for the relevant materials are given in Table III. The maximum stress once again increases in the presence of scallops, peaking at locations where two scallops meet, as shown in Fig. 12 by investigating the stress distributions along one-dimensional radial cut lines through the TSV middle. The highest stress is seen in the tungsten layer, while the lowest is observed through the oxide. The TSV structure with flat sidewalls experiences a homogeneous stress through each material layer. However, the scalloped structures show a peak, which is higher than that noted in the flat TSV, but also a minimum which is below that noted in the flat TSV. The scalloped structures in the top graph in Fig. 12 show the stress peak at the location where two scallops at the SiO_2 liner/W interface meet. The stress peaks shown in the bottom graph in Fig. 12 occur where a scallop has its longest width, at the W/SiO_2 isolation interface.

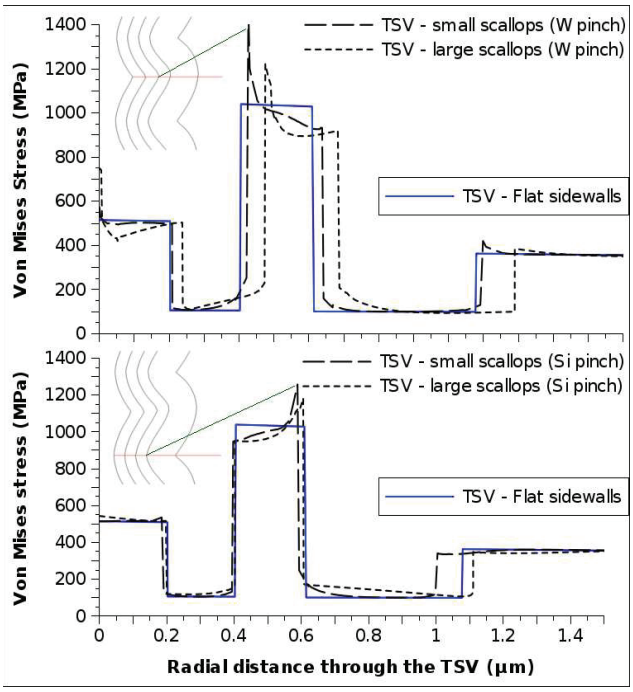
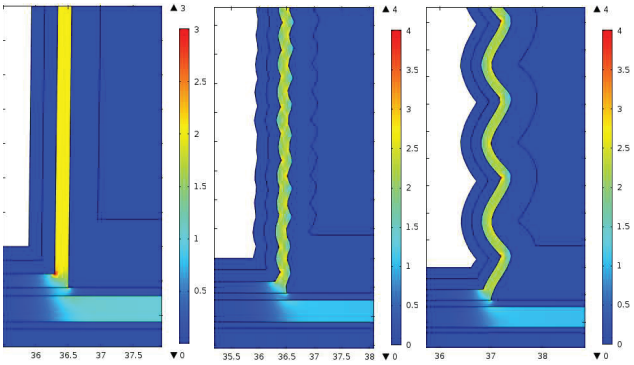


Fig. 12. Von Mises stress through the vertical middle of the open tungsten TSVs assuming a drop from a stress-free temperature of 320°C to 20°C.

B. Electromigration-Induced Stress

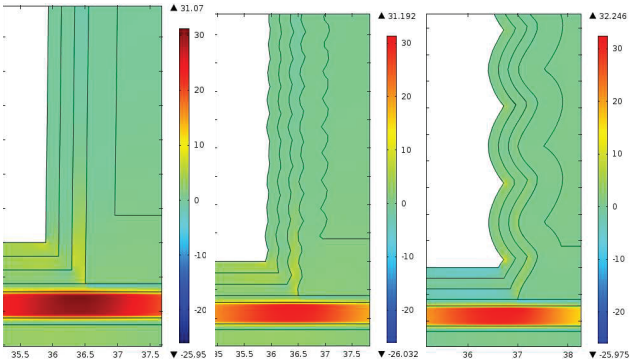
Electromigration analyses were performed on the structures using a model presented in [7], with the resulting current density and EM-induced stress through the structures shown in Fig. 13 and Fig. 14, respectively. There appears to be no major change in the current density distribution between the three structures, except for slight increases at locations where two scallops meet.

The stress in Fig. 14 is generated after operating the devices at 1A for approximately one year. The stress generated in the TSV is not affected by the scalloped sidewalls, because the aluminum layer is where EM effects are critical. The stress level after one year of operation is shown to be approximately 30MPa, which is significantly smaller than the levels seen for copper TSVs. This is mainly due to the large volume of aluminum used, which covers the entire bottom of the TSV. This ensures a low current density and low vacancy build-up in this layer. The thickness of the bottom aluminum layer plays a more significant role in determining the EM-induced stress,



(a) Flat sidewalls (b) Small scallops (c) Large scallops

Fig. 13. Current density distribution (MA/cm^2) in the aluminum layer of the three open tungsten TSVs when a 1A current is applied through the structure.



(a) Flat sidewalls (b) Small scallops (c) Large scallops

Fig. 14. Electromigration-induced stress (MPa) in the aluminum layer of the three open tungsten TSVs when a 1A current is applied through the structure for one year.

as shown in Fig. 15, where the stress build-up over time is shown. The use of a 20% thinner aluminum layer results in a 67% increase in the observed stress.

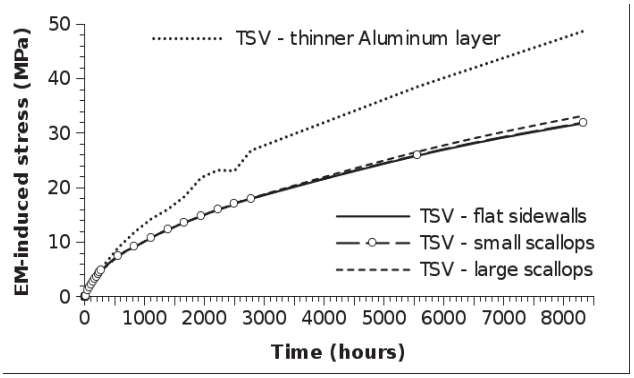


Fig. 15. Maximum EM-induced stress (MPa) through the aluminum layer in the open tungsten TSVs, while operating with a 1A current applied through the structure.

V. Conclusion

The performance of several TSVs has been tested through simulations. Two different TSV structures have been analyzed and the effects of sidewall scallops which are generated during TSV processing on the TSVs' performance and reliability have been shown. The simulated topographies of the structures were imported into a finite element simulator in order to compare the performances of the different devices. Electrical parameter extraction showed that the TSV resistance, inductance, and capacitance are affected by the scalloped walls. The thermo-mechanical stress is also shown to be influenced by the process, while the EM-induced stress for the open tungsten TSV is independent of the sidewall structure, due to the stress developing in the bottom aluminum layer. Filled copper TSVs with scalloped sidewalls only experience an incresed EM-induced stress due to sidewall tapering, suggesting that the scallops themselves do not influence the EM response significantly.

Acknowledgment

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