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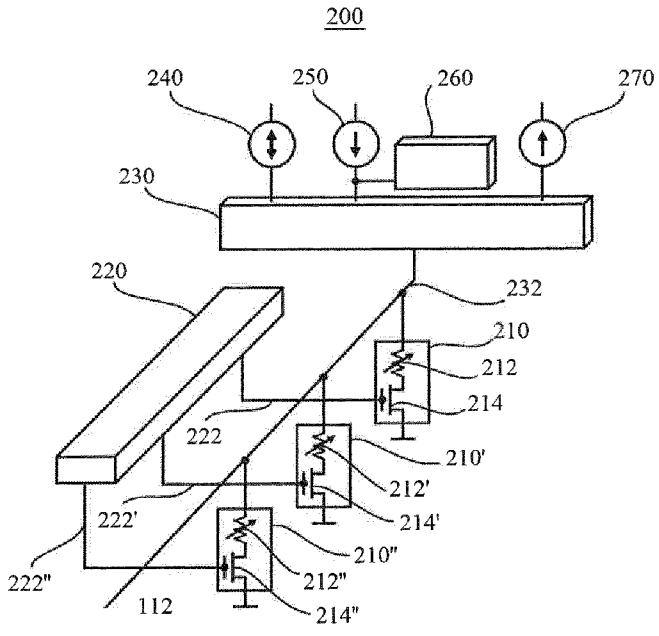

Figure 3

(57) Abstract: The invention relates to an electronic circuit (200, 400) comprising a plurality of bit cells (210, 410) arranged in an array and being selectable by row lines (222, 422) and column lines (232, 432), at least one row driver (220, 420), at least one column driver (230, 430), and a readout circuit (260, 460), wherein each bit cell (210, 410) comprises an access transistor (214, 414) and a non-volatile resistive- switching element (212, 412) with at least two resistance states, wherein, in order to write a new data (T_n+1) in a target bit cell (T), said new data depending on a data (S_n) of a source bit cell (S) and on a data (T_n) stored by the target bit cell (T) before sad writing, the row driver (220, 420) and the column driver (230, 430) are capable to simultaneously apply a first selecting voltage (V_s) to a first row line (222, 422) to select the target bit cell (210, 410), a secod selecting voltage (V_p-s) to a second row line (222', 422') to select the source bit cell (210', 410'), and a logic current (1 imp) to at least one column line (232, 432), wherein the first selecting voltage (V_s) is higher than the second selecting voltage (V_p-s), such that in response to the voltages applied to the target and source bit cells, the access transistor of the target bit cell ha a lower resistance than the access transistor of the source bit cell.

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RRAM IMPLICATION LOGIC GATES

The invention relates to an electronic circuit comprising a plurality of bit cells arranged in array and being selectable by row lines and column lines, at least one row driver, at least one column driver, and a readout circuit, wherein each bit cell comprises a non-volatile resistive-switching element and an access transistor.

BACKGROUND

At present, the most commonly used logic circuits consist of a memory unit for data storage and a separate logic unit for holding data and performing arithmetic and logic operations which are typically based on CMOS technology. On one hand, these CMOS-based logic circuits retain information as long as power is applied (volatility) and any power supply interruption can cause loss of information. On the other hand, as the dimensions of the CMOS transistors shrink down the leakage currents increase. As a result, the power consumption is nowadays an important limiting factor in scaling of the CMOS technology. For instance the standby power consumption in CMOS-based logic circuits has become comparable to the dynamic power consumption.

Introducing non-volatility into the circuits for which non-volatile memory elements are distributed among logic gates can solve the standby power problem described before. A configuration which combines logic and memory elements (so-called logic-in-memory), allows shortening interconnection delays by eliminating the need to transfer data into separate memory and logic circuits.

The logic-in-memory circuit disclosed in US 2005/0174837 A1 uses tunnel magnetoresistance (TMR) elements as non-volatile memory devices to provide memory inputs. It realizes the AND operation between one memory input (as stored data) and an external input which is a voltage signal. The operation result is provided by an IV converter as a voltage value.

The problem with this logic-in-memory configuration is that the realized AND operation is volatile and writing the generated output voltage signal into a non-volatile element requires additional circuitry for generating a writing magnetic field which increases delay and complexity. Furthermore, the configuration realizes only an AND operation and cannot perform OR and NOT operations and thus requires at least a CMOS-based NOT operation to be computationally complete.

The logic-in-memory circuit disclosed in US 7221600 B2 uses a variable resistance element as non-volatile memory device to provide a memory input and realizes AND and OR operations for which the memory device can be used also as the output in the case of destructive operations. With this configuration, a logic operation between different memory inputs cannot be performed. Therefore sensing amplifiers are required to read the memory data at each logic stage and providing the next stage with a voltage signal as an external input.

The magneto-logic circuit disclosed in US 7755930 B2 uses a magnetic memory element and a current driving circuit to realize logic operations on a plurality of input values which are voltage signals. The operation output is written into the magnetic memory element by applying a magnetic field generated by a current changing in accordance to the logic states of the input values.

However, a key limitation of these logic circuits is the necessity to have different kinds of inputs and outputs for which some inputs or outputs are voltage signals whereas the others are the resistance state of non-volatile memory elements. This mismatch causes the need for extra hardware including sensing amplifiers to read the memory data at each logic stage and providing the next logic stage with a proper voltage signal as an external input from the output of the previous logic stage. This increases the power consumption, time delay, and complexity.

The document US 8179716 B2 discloses non-volatile logic gates comprising Spin-Transfer Torque (STT)-operated magnetic tunnel junction (STT-MTJ) elements which are used as the main devices for logical computations (intrinsic logic-in-memory) for which the need of extra hardware (CMOS-based logic gates) is eliminated. After performing a logic operation the logic input and output values are stored in the resistance state of the input and output memory elements.

However, the logic inputs are determined by the polarity of the input currents applied to the input MTJ elements. Therefore the logic circuit requires sensing amplifiers to read the output data to provide an input current in proper direction for the next logic stage. Furthermore, the ferromagnetic free layers of the input and the output MTJ elements in each gate must be electrically connected via magnetostatic or physical coupling. This highly localizes the logical computations and limits the possibility of performing logic operations between different inputs MTJs of different gates. Thus, generalization of such non-volatile logic gates to large-scale logic circuits is problematic.

Therefore, in the state of the art, large-scale integration of complex logic functions cannot be realized using the non-volatile logic-in-memory concept due to the need for sensing amplifiers and intermediate circuitry. This causes a lack of flexibility because of hard linking between the inputs and output memory elements in a particular gate.

Therefore, the object of the invention is to provide an electronic circuit that combines the features of resistive memory devices with the features of logic devices, to enable the construction of a logic-memory-circuit that can execute logic operations without the need of adding conventional logic gates, sensor devices, or amplifiers.

SUMMARY OF THE INVENTION

To overcome the above-described problems, this invention discloses an electronic circuit comprising a plurality of bit cells arranged in an array and being selectable by row lines and column lines, at least one row driver, at least one column driver, and a readout circuit, wherein each bit cell comprises an access transistor and a non-volatile resistive-switching element with at least two resistance states, wherein the row driver and the column driver are capable to simultaneously apply a selecting voltage V_s to a first row line to select a target bit cell, a pre-selecting voltage V_p-s to a second row line to select a source bit cell, and a logic current I_imp to at least one column line, wherein the selecting voltage V_s is higher than the pre-selecting voltage V_p-s.

Based on the presented electronic circuit, it is possible to extend the functionality of a common non-volatile resistive memory to include performing logic operations for which the need for sensing amplifiers and distributing logic devices over the memory block is eliminated. Memory elements at different locations can be used to construct logic gates. Therefore the logical computation is not localized and fewer elements are required to realize logical functions. Due to non-local logic implementation on one hand and being computationally complete on the other hand, the disclosed logic-in-memory circuit is highly flexible and suited for large-scale non-volatile logic systems.

Furthermore, unlike the state-of-the-art logic-in-memory circuits, the disclosed logic-in-memory can use any memory element as both input and output element and offers an efficient, flexible, and simple circuit structure suited for large-scale non-volatile logic systems, which allows shortening interconnection delays and opens the door for innovations in computational paradigms by shifting away from the Von Neumann architecture.

According to the invention, the source bit cell modulates the current or voltage required to reach a critical current or voltage to switch a full-selected bit cell (target bit cell). The result depends on the initial state of the target bit cell. Depending on the initial states of both the source and the target bit cells a switching event is enforced to the target bit cell (desired switching event) or not.

A desired switching event is a high-to-low switching event which is enforced to the target bit cell only when both target and source resistive-switching elements are initially at high resistance states and for all three other possible combinations of the initial resistance states, both target and source resistive-switching elements are left unchanged and there is no undesired switching event. This initial state dependent switching corresponds to the basic Boolean operations called IMPLIES (IMP) and NOT IMPLIES (NIMP, negated IMP).

The initial logic state of the source and target bit cells act as the inputs and the final logic state of the target bit cell is the output of the logic operation. In combination with a writing operation (low-to-high resistance switching), the material implication forms a complete logic basis to compute any Boolean function.

The resistive-switching element according to the invention might require a critical current or voltage for switching between the high and the low resistance states. The switching of the resistance state can also be performed by a current pulse of sufficient duration. It can be provided that the resistive-switching element has a distinct low resistance state and a distinct high resistance state.

Respective resistive-switching devices could be realised, for example, as capacitor-like devices such as metal-oxide-interface which show oxygen ion/vacancy migration and formation/annihilation at the interface, phase change memory devices, or electron spin junctions. Some resistive-switching devices show a continuous change in resistance, for example a TiO2 memristive switch was shown where the resistance can be equal to any value between 100 Ohm and 10 kOhm. According to the invention, any resistive-switching device can be used which has at least two resistance states (low and high) configured for storing binary data and requires a critical current or voltage for switching between the high and low resistance states.

A resistive-switching device according to the invention can be unipolar or bipolar. For unipolar switching mechanism the low-to-high or high-to-low switching can occur both at the positive and negative current or voltage polarities and only the amplitude of the applied signal is important.

For bipolar switching in can be provided that the resistance state of the resistive-switching elements is changed from a first state to a second state by a current or voltage impulse in a first direction, and from the second state to the first state by a current or voltage impulse in the opposite direction, where a critical current I_H-to-L or critical voltage has to be applied for switching. The applied current or voltage can change the polarity to switch between different resistance states and the positive and negative signals may have the same (symmetric switching characteristics) or different (asymmetric switching characteristics) amplitudes.

It may be provided within the scope of the invention that the resistive-switching element has an asymmetric switching characteristic and the logic current I_imp has the same polarity as the current I_H-to-L required to switch the resistive-switching element.

It can further be provided that the resistive-switching element has a unipolar switching characteristic so that the resistance state of the resistive-switching elements is changed from a first state to a second state by a current or voltage of a first amplitude, and from the second state to the first state by a current or voltage impulse of a second amplitude, where a critical current I_H-to-L or critical voltage has to be applied for switching.

Preferably, the logic current I_imp can have an amplitude higher than the critical current I_H-to-L to enforce a desired switching event in the resistive-switching element of the target bit cell but small enough to prevent undesired switching events of the source or the target bit cell. The ratio of the current I_imp to the current I_H-to-L required to switch the resistive-switching element can preferably be between 1 and 2.

The logic current I_imp can also have the same amplitude as the current I_H-to-L and be applied at a pulse duration that is long enough to enforce a desired switching event in the resistive-switching element of the target bit cell and short enough to prevent undesired switching events of the source or the target bit cell. Preferably, the current pulse I_imp can be applied at a pulse duration that is 2 - 3 orders of magnitude longer than the pulse duration of the current I_H-to-L. To avoid undesired switching events, there can be a particular range for the amplitude and/or the pulse duration of the logic current I_imp.

The resistive-switching elements can be realized as magnetic tunnel junction (MTJ) devices, preferably Spin-Transfer-Torque (STT) MTJ devices, and the access transistors as conventional CMOS transistors.

The invention further relates to a method to perform the logic operation material implication (IMP) or negated material implication (NIMP) on a non-volatile resistive memory array comprising a plurality of bit cells being selectable by row lines and column lines, wherein each bit cell comprises a non-volatile resistive-switching element with at least two resistance states, and an access transistor, at least one row driver, at least one column driver, and a readout circuit, wherein simultaneously the row driver applies a selecting voltage V_s to a first row line to select a target bit cell and a pre-selecting voltage V_p-s to a second row line to select a source bit cell, wherein V_s is higher than V_p-s, and the column driver applies a logic current I_imp to at least one column line.

The logic current I_imp can have a higher amplitude than a critical current I_H-to-L required to switch the resistive-switching element of the target bit cell from a high resistance state to a low resistance state but small enough to prevent undesired switching events. Preferably, the ratio of the current I_imp to the current I_H-to-L can be between 1 and 2.

The logic current I_imp can also be applied at a pulse duration that is long enough to enforce a desired switching event in the resistive-switching element of the target bit cell, but still short enough to prevent undesired switching events. Preferably, the current pulse I_imp can be applied at a pulse duration that is 2-3 orders of magnitude longer than the pulse duration of the current I_H-to-L.

In a memory mode, the above mentioned logic-in-memory array utilizes the access transistors as on/off switches to read/write any bit cell. In a logic mode, an access transistor is used as a voltage-controlled resistor to pre-select a bit cell which acts as an input bit cell (source bit cell).

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a diagram of a common logic circuit comprising memory and logic units,

FIG. 1B is a diagram of a common logic-in-memory circuit,

FIG. 2 is a diagram of a common magnetic memory using spin transfer torque magnetoresistive random-access memory (STT-MRAM) technology,

FIG. 3 is a diagram depicting one embodiment of an intrinsic logic-in-memory array in accordance with the present invention,

FIG. 4A is a truth table of the realized basic logic operation NIMP using the intrinsic logic-in-memory circuit in accordance with the present invention,

FIG. 4B is a graph illustrating the high-to-low resistance switching dynamics of a resistive-switching element according to the invention,

FIG. 5A is a table showing subsequent steps required for performing the universal logic operation NOR in the logic-in-memory circuit according to the invention,

FIG. 5B is a truth table of the three-step process to perform the universal NOR operation in the intrinsic logic-in-memory circuit in accordance with the present invention,

FIG. 6A is a truth table of the realized basic logic operation IMP using the intrinsic logic-in-memory circuit in accordance with the present invention,

FIG. 6B is a truth table of the three-step process to perform the universal NAND operation in accordance with the present invention,

FIG. 7 is a diagram depicting a further embodiment of an intrinsic logic-in-MRAM (magnetoresistive random-access memory) using spin-transfer torque (STT) switching technology (STT-MRAM) according to the invention.

FIG. 1A shows a state-of-the-art logic circuit 10 including a logic unit 14 and a memory unit 12 which are connected through a data bus 17. The logical process in logic circuit 10 is performed by reading the data out from the memory unit 12 and transferring the data to the logic unit 14 through the data bus 17, performing logic operations in the logic unit 14, and transferring the operation results back to the memory unit 12 through the data bus 17. As more data has to be transferred in shorter time, the data bus turns out to be a major performance-limiting bottle neck of such a structure. In addition to that, leakage currents due to shrinking feature size of common CMOS components has become a top concern of the logic circuits used.

Logic-in-memory circuits have been proposed to solve this issue. In the state-of-the-art logic-in-memory circuit 20 shown in FIG. 1B, non-volatile memory elements 22 are distributed among logical elements 24 to construct local logical sub-circuits 21. This architecture can significantly reduce the standby power by holding the information in non-volatile memory elements. Refreshing pulses, which are critical for CMOS-based storage elements, can be avoided. Furthermore, the short data transfer path between the memory element 22 and the adjacent logical element 24 can significantly reduce the data transfer time and the data traffic on a main bus like the data bus 17, so that in effect interconnection delays are reduced. As a non-volatile technology, the magnetic tunnel junction (MTJ) is very promising for logic-in-memory circuits since it is CMOS-compatible, fast, low power, highly scalable and has excellent endurance. However, in the logic-in-memory circuit 20 the non-volatile memory elements (for example MTJs) are used only as ancillary devices for logical computations. They require readout schemes for reading the stored logical data as well as properly adjusted current or voltage signal levels to function with the logical elements 24. A seamless integration with the logical elements 24 is not possible. This limitation increases complexity, delay, and power consumption. Furthermore, as the logical computations are localized, the generalization of the common logic-in-memory circuits to large-scale logic systems is complicated.

FIG. 2 shows a diagram of a state-of-the-art magnetic non-volatile memory array using Spin-Transfer Torque (STT) Magnetoresistive Random-Access Memory (MRAM) technology. The electronic circuit 100 comprises a plurality of non-volatile bit cells 110 coupled to a column driver 130 through a plurality of column lines 132. Each bit cell 110 comprises a resistive-switching element 112 configured to store binary data and an access transistor 114 coupled in series. The resistive-switching element 112 is provided as a magnetic tunnel junction (MTJ) device, and the access transistor 114 as a CMOS (complementary metal-oxide semiconductor) transistor. In general, an MTJ element includes at least one ferromagnetic free layer and a ferromagnetic pinned layer separated by a nonmagnetic barrier layer. The electrical resistance of the MTJ element is low (high) when the magnetization directions of the free layer and pinned layer are parallel (antiparallel). In STT-MRAM technology, the free layer of the MTJ element switches from parallel to antiparallel alignment (or vice-versa) compared with the pinned layer when the torque exerted by spin-polarized electrons passing through the MTJ element (spin transfer torque) exceeds a threshold value. The access transistors 114 act as on/off switches which control the current flowing through the resistive-switching elements 112. The gate terminals of the access transistors are coupled to a row driver 120 via row lines 122 for applying proper voltage signals to switch on the access transistors 114 to select the resistive-switching elements 112 in a desired row for reading and writing operations.

During a reading operation, the row driver 120 selects the desired row line 122 and the column driver 130 applies a read current 150 (I_rd) to the desired column line 132 which will flow through the desired bit cell 110. Depending on the binary data stored in the desired bit cell 110, the desired resistive-switching element 112 is in a high or low resistance state. A readout circuit 160 is provided to read the logical value stored in the selected bit cell by sensing the generated voltage difference on the column line 132. The read current (I_rd) 150 must be low enough to prevent a read disturbance which results in an undesired switching.

During a writing operation, the row driver 120 selects the desired row line 122 and the column driver 130 applies a write current 140 to the desired column line 132 which will flow through the desired bit cell 110.

The write current is denominated I_H-to-L for high-to-low resistance switching or I_L-to-H for low-to-high resistance switching, depending on the desired binary data (logical 1 or 0) which should be written in the desired bit cell.

FIG. 3 illustrates an intrinsic logic-in-memory array in accordance with the present invention. The electronic circuit 200 comprises a plurality of non-volatile bit cells 210 coupled to a column driver 230 through a current carrying column line 232. Each bit cell 210 comprises a resistive-switching element 212 configured to store binary data and an access transistor 214 coupled in series. The resistive-switching element 212 is a two terminal device which has a variable resistance and the logical data can be stored in its low resistance state (LRS) or high resistance state (HRS).

A sufficiently high enough current or voltage in a first direction can switch the resistive-switching element to LRS. If applied in a second direction, a sufficiently high enough current or voltage puts the resistive-switching element in HRS. The resistive-switching element requires a critical current or voltage for switching and, for example, it can be a STT-MTJ, a phase-change memory, or a memristive switch based on ionic transport in a metal/oxide/metal structure, etc. For a resistive-switching element with bipolar switching characteristic (such as a STT-MTJ) the first and the second critical currents or voltages for LRS and HRS switchings have the opposite direction. The resistive-switching element may require the same (symmetric switching) or different (asymmetric switching) current or voltage pulse amplitudes for LRS and HRS switchings. For a resistive-switching element with unipolar switching characteristic (such as a phase-change memory) the first and the second critical currents or voltages for LRS and HRS switchings have different pulse amplitudes but can be in the same or in the opposite direction.

In a further embodiment of the invention not shown, the resistive-switching element can be switched from the LRS to the HRS by a current pulse of a specific first duration, and from the HRS to the LRS by a current pulse of a specific second duration different from the first duration.

The access transistor 214 controls the current which passes through the resistive-switching element 212.

The gate of the access transistor is coupled to a row driver 220 via a row line 222 for selecting or pre-selecting bit cells in a row line in order to read, write, or perform a logic operation. For reading the logical data stored in a bit cell 210', the row driver 220 selects the access transistor 214' by applying a select voltage V_s to the row line 222' and the column driver 230 drives a read current 250 to the column line 232. The read current 250 flows through the bit cell 210'. Depending on the binary data stored in the selected bit cell, the resistive-switching element 212' is in the high or low resistance state. Therefore a readout circuit 260 can detect the data by sensing the generated voltage difference on the column line 232. The read current 250 must be low enough to prevent a read disturbance which for example can be an undesired switching.

For writing logical data into a desired bit cell, for example bit cell 210', the row driver 230 selects the access transistor 214' by applying a select voltage V_s to the row line 222' and the column driver 230 applies a write current 240 to the column line 232. The write current 240 then flows through the bit cell 210'. The write current 240 can be of a first value I_H-to-L in a first direction for high-to-low resistance switching or of a second value I_L-to-H in the second direction for low-to-high resistance switching, depending on the binary data that shall be written.

In an embodiment not shown, the write current 240 is applied for a specific pulse duration to perform the switching of the bit cell 210'.

For performing the logic operation NIMP, the row driver 220 selects simultaneously a desired target bit cell 210 and pre-selects a desired source bit cell 210', and the column driver 230 applies a logic current 270 (further denominated as I_imp) to the column line 232. The logic current 270 has a higher amplitude than I_H-to-L and has the same polarity.

The row driver 220 utilizes the access transistors 214, 214' as voltage-controlled resistors and applies a selecting voltage V_s or a pre-selecting voltage V_p-s to any row line. The voltage V_s is higher than that of V_p-s. Therefore, the resistance of the selected transistor 214 is smaller than the resistance of the pre-selected transistor 214'.

The logic current 270 therefore divides between the target bit cell 210 and the source bit cell 210' and is inversely proportional to the total resistance of each bit cell 210, 210'. The total resistance of each bit cell 210, 210' is the sum of the resistances of the access transistors 214, 214' and the resistive-switching elements 212, 212'.
Since the resistance values of the resistive-switching elements 212, 212' depend on the stored logical values, the current division between the target bit cell 210 and the source bit cell 210' will depend on the logic states of the bit cells 210, 210'. Because the logic current 270 has the same polarity and a higher amplitude as I_H-to-L, it tends to put both selected and pre-selected resistive-switching elements 212, 212' into the low resistance state.

Fig. 4A shows a state diagram of the logic states of the source bit cell 212' (Source S_n) and the target bit cell 212 (Target T_n). Both bit cells can either be in a high resistance state (HRS, corresponding to a logic "1") or in a low resistance state (LRS, corresponding to a logic "0").

The cases 1 to 4 correspond to the 4 different initial states based on the initial resistance (logic) states. Depending on the current level through the target bit cell I_T1, I_T3, it switches from its initial states to its final states. The conditional switching behavior realizes a logic operation shown in Fig. 4A. The different switching events will be discussed below together with the discussion of the switching dynamics in Fig. 4B.

FIG. 4B shows the switching dynamics of a resistive-switching element according to the invention as a function of the current or voltage pulse amplitude. In FIG. 4B the horizontal axis 320 shows the current (or voltage) level applied to a resistive-switching element for a given time (equal to the pulse duration). The solid curve 330 indicates the high-to-low resistance switching dynamics of the resistive-switching element.

The vertical axis 310 represents the switching probabilities for a particular resistive-switching element (a STT-MTJ) with a stochastic switching model or a normalized internal state variable of the resistive-switching element (a metal/oxide/metal memristive switch) with a deterministic switching model.

On the right hand side, for the reliable switching region 370, the dashed line 322 represents the minimum reliable switching current (I_wr0) or a corresponding voltage. On the left hand side, the reliable non-switching region 380, the dashed line 323 represents the maximum reliable non-switching current (I_rd0) or a corresponding voltage. The maximum reliable non-switching current can be seen as the maximum current which does not cause an undesired switching event or a reading disturbance.

The logic current 270 (I_imp) divides between the target bit cell 210 and the source bit cell 210' as:

$$I\_imp = I\_Ti + I\_Si$$

$$I\_Ti = R\_Si \ (I\_imp / R\_Ti + R\_Si)$$

$$I\_Si = R\_Ti \ (I\_imp / R\_Ti + R\_Si)$$

I_Ti and I_Si are the currents passing through the target bit cell 210 and the source bit cell 210', respectively. R_Ti and R_Si are the total resistances of the target bit cell 210 and the source bit cell 210', respectively. Depending on the initial states, i indicates the Case number which can be 1, 2, 3, or 4 as shown in FIG. 4A. Since the logic current 270 has the same polarity as I_H-to-L, I_Ti and I_Si, it tends to put the target resistive-switching element 212 and the source resistive-switching element 212' into the low resistance state.

As shown in FIG. 4A, the source resistive-switching element 212' is already in the low resistance state in Case 3 and Case 4. Therefore a switching event in the source resistive-switching element 212' can only be enforced in Case 1 and Case 2, when the source resistive-switching element 212' is in the high resistance state. Since the source access transistor 214' is pre-selected, and the pre-selecting voltage V_p-s is lower than the selecting voltage V_s, its resistance is high. Therefore the currents passing through the source bit cell 210' in Case 1 (I_S1; source bit cell current 328) and Case 2 (I_S2; source bit cell current 329) are lower than the maximum reliable non-switching current 323 (I_rd0). No switching can occur. Thus in all Cases 1 – 4 the source resistive-switching element 212' is left unchanged.

The target resistive-switching element 212 is initially in a low resistance state in Case 2 and Case 4, therefore I_Ti can enforce a switching event to the low resistance state only in Case 1 and Case 3.

The difference between the currents passing through the target resistive-switching element 212 in Case 1 and Case 3, I_T1 and I_T3, is caused by the difference between the initial resistance states of the source resistive-switching element 212'. In Case 1 the source access transistor 214' is pre-selected and also the source resistive-switching element 212' is in its high resistance state.

Therefore the total resistance of the source bit cell 210' (R_S1) is higher than the total resistance of the target bit cell 210 (R_T1), so the majority of the logic current 270 (I_imp) flows through the target bit cell 210. The target bit cell current I_T1 is higher than the source bit cell current I_S1.

The target bit cell current I_T1 (reference numeral 325 in FIG. 4B) is higher than the minimum reliable switching current 322 (I_wr0) and it enforces a high-to-low resistance switching event in the target bit cell 210. During the switching the resistance of the target resistive-switching element 212 decreases while the resistance of the source resistive-switching element 212' remains unchanged. Therefore the current passing through the target resistive-switching element 212 (I_T1) increases. This generates a positive feedback which accelerates the switching.

In Case 3, although the source access transistor 214' is pre-selected, the source resistive-switching element 212' is in low resistance state. Therefore the current passing through the source bit cell 210' is higher as compared to Case 1 ($I_{S3}>I_{S1}$). This decreases the current I_T3 passing through the target bit cell 210 (reference numeral 326 in FIG. 4B) below the maximum reliable non-switching current 323 ($I_{T3}<I_{rd0}$).

This state dependent modulation of the current passing through the target bit cell 210 (double arrow 350 in FIG. 4B) realizes a conditional switching behavior which is equivalent to the basic logic operation shown in FIG. 4A. In combination with the low-to-high resistance state switching (writing logical 1; the operation TRUE), the realized logic

operation is called NIMP (NOT IMPLIES) and forms a complete logic basis to compute any other Boolean function.

Since the electronic circuit 200 is realized as a logic-in-memory circuit, the final states of the source and target bit cells 210', 210 can be directly used for storing logic data. There is no interface or driver electronics necessary, as in conventional memory circuits that are coupled to logic devices. Instead of first fetching an initial state from memory, computing the logic operation, and writing back the final state to memory, the logic operation is directly performed on the memory itself. Fetching and writing back becomes obsolete.

FIG. 5A shows a three-step implementation of the universal logic operation NOR using sequential TRUE and NIMP operations on three arbitrary bit cells like 210, 210', and 210" containing the logical values C, C', and C", respectively. In Step 1, the low-to-high resistance state switching is executed on the bit cell 210" by applying the current I_L-to-H to the bit line 232 and the selecting voltage V_s to the gate terminal of the access transistor 214".

In Step 2, the operation NIMP is executed between the bit cell 210 and 210" by applying the current 270 (I_imp) to the bit line 232, the pre-selecting voltage V_p-s to the access transistor 214, and the selecting voltage V_s to the access transistor 214". Therefore, 210 and 210" act as the source and the target bit cells, respectively, and the operation result will be written in 210".

In Step 3, the operation NIMP is executed between the bit cell 210' and 210" by applying the current 270 (I_imp) to the bit line 232, the pre-selecting voltage V_p-s to the access transistor 214', and the selecting voltage V_s to the access transistor 214".

Therefore, 210' and 210" act as the source and the target bit cells, respectively, and the final result will be written in 210". The final result is equivalent to the NOR operation between 210 and 210'. Since the operation NOR is a universal logic operation, any Boolean function can be performed by using a combination of NIMP and TRUE operations.

Opposite to the conventional definition, if the high and low resistance states (HRS and LRS) are defined as logical 0 and 1, the basic logic operation described in FIG. 4A will be equivalent to the fundamental logic operation IMP (IMPLIES) as shown in FIG. 6A ($T_{n+1} \leftarrow S_n$ IMP T_n). With this definition, the low-to-high resistance switching is equivalent to writing logical 0 (operation FALSE). In combination with FALSE, the operation IMP forms a complete logic basis to compute any Boolean function. With this definition, subsequent operations described in FIG. 5B will be corresponding to the universal NAND operation between 210 and 210' as shown in FIG. 6B.

As an example of the generalization of the intrinsic logic-in-memory array 200 to an intrinsic logic-in-random-access memory (logic-in-RAM) circuit by using STT-MTJs as non-volatile resistive-switching elements, the common STT-MRAM 100 can be upgraded to a logic-in-STT-MRAM (or briefly logic-in-MRAM) architecture with no need to add CMOS-based logic gates, arithmetic circuits, or buses.

FIG. 7 shows an intrinsic logic-in-MRAM circuit using STT-MRAM technology based on the intrinsic logic-in-memory array in accordance with the present invention. The electronic circuit 400 comprises a plurality of intrinsic logic-in-memory arrays coupled to a column driver 430 through a plurality of current carrying column lines 432. Each intrinsic logic-in-memory array comprises a plurality of non-volatile bit cells 410 for which each bit cell 410 comprises a resistive-switching element 412 realized as STT-MTJ element and an access transistor 414 realized as CMOS transistor coupled in series.

In the electronic circuit 400, similar to the electronic circuit 100 which acted as an electronic memory circuit and the electronic circuit 200 which acted as an intrinsic logic-in-memory array, the reading and writing operations of desired bit cells 410 can be performed by selecting the desired row using the row driver 420 through the desired row line 420 and applying the proper current pulse to the desired column line 432.

Since by selecting the desired row all access transistors 414 in the row are selected, parallel reading and writing operations are possible, if the column driver 430 can apply proper current pulses to more than one column at the same time and the readout circuit 460 can sense the voltage differences generated on all the columns simultaneously.

For performing the basic logic operation (IMP or NIMP) in accordance with the present invention, similar to the electronic circuit 200, the row driver 420 selects a desired row as the target row by applying the select voltage V_s and pre-select another desired row as the source row by applying the pre-select voltage V_p-s simultaneously, and the column driver 430 applies the logic current 470 (I_imp) to a desired column line 432. Since by selecting and pre-selecting the as target and source rows all access transistors in the rows are selected and pre-selected, respectively.

In the electronic circuit 400, since each row line gate terminals of the access transistors are coupled, parallel logic implementation in the columns is achieved if the column driver 430 applies logic current pulses I_imp to more than one column at the same time.

From a circuit point of view, the electrical signals required for performing the logic operation IMP or NIMP in a logic-in-MRAM circuit depends on the material composition, geometry, processing, layout/design, and so on. They are chosen based on experimental data for which the logic error Er_imp, defined as Er_imp = 1-P_T1 + P_S1 + P_S2 + P_T3 is minimized. Here, P_T1 is the switching probability of the target MTJ in Case 1 (desired switching even) which goes to unity, and P_S1, P_S2, and P_T3 are the switching probabilities of the source and target bit cells in Case 1, 2, and 3, respectively (undesired switching events) which go to zero.

Exemplary electrical data are discussed below for an exemplary embodiment of a logic-in-MRAM according to the invention, based on a one-transistor/one-MTJ (1T/1MTJ) state-of-the-art structure fabricated using 0.18 μm CMOS technology with a 4 level metal for tailored MTJ which has an oval shape of 115x155 nm including an anti-ferromagnetic (AF) pinning layer, a synthetic anti-ferromagnetic pinned layer, a tunnel barrier MgO layer, and a free magnetic layer, as reported by M. Hosomi et al., "A novel nonvolatile memory with spin torque transfer magnetization switching: spin-ram," Proc. IEDM, 2005.
The relationship between the critical switching current I_C and the pulse duration τ for pulse duration between 10 ns and 100 us is found to be $\tau=\tau_0 \exp [E/KT\times(1-I_C/I_{C0})]$, where τ_0 is 1 ns, E is the energetic barrier height, and I_{C0} is the critical switching current extrapolated to 1 ns.

For writing operations with a pulse duration between 10ns and 100 ns, a selecting voltage V_s in the range of 1.2 to 1.6 V should be applied to a row line 422 and a writing current pulse 440 in the range of 200 to 300 uA should be applied to a column line 432 in a first direction for high-to-low resistance switching (I_H-to-L) or a writing current pulse 440 in the range of 300 to 400 uA should be applied to the column line 432 in the opposite direction for low-to-high resistance switching (I_L-to-H).

For performing logic with a pulse duration between 10ns and 100 ns, a selecting voltage V_s in the range of 1.2 to 1.6 V should be applied to a first word line 422 to select a target bit cell, a pre-selecting voltage V_p-s in the range of 0.6 to 0.8 V should be applied to a second row line 422 to pre-select a source bit cell, and a logic current I_imp in the range of 340uA to 510uA should be applied to at least one column line 432. In order to compensate the current passing through the source bit cell, the logic current I_imp has a higher amplitude than the writing current I_H-to-L when they have the same pulse durations of 10ns to 100 ns.

For performing logic, when the logic current I_imp has the same pulse amplitudes as the writing current I_H-to-L, a pulse duration of 10us to 100us is required which is about 3 orders of magnitude higher than the pulse durations required for the writing operations. In fact at the cost of exponentially increasing the pulse duration, the pulse amplitude can be decreased.

From the device point of view, the tunneling magnetoresistance (TMR) ratio of the MTJ device is the most important parameter for reliability. It can be shown that for optimized electric signals, the Er_imp decreases exponentially with increasing the TMR ratio. For a TMR ratio higher than 250% the error is Er_imp<0.001 which means the desired switching probability P_T1 is higher than 99.9% and the undesired switching probability P_ S1 , P_ S2 , and P_ T3 are lower than 0.1%. The theoretical maximum TMR ratio is about 1000% and the highest TMR ratio obtained so far for MgO-barrier MTJs is about 500% which decreases the error to Er_imp<0.00001.

The invention is not limited to the described embodiments, but comprises as well further embodiments that fall within the scope of the claims. Individual features and characteristics of the invention shown in particular embodiments can be combined and the invention is not limited to the particular embodiments. In particular, the invention is not limited to a specific kind of non-volatile resistive-switching memory element or access transistor, as well as to a specific circuit layout or electrical signal range.

The work leading to this invention has received funding from the European Research Council under the European Union's Seventh Framework Programme (FP7/2007-2013) /ERC grant agreement n° 247056 MOSILSPIN.

List of reference numerals

10	Logic circuit
12	Memory unit
14	Logic unit
17	Data bus
20	Logic-in-memory circuit
21	Logical sub-circuit
22	Non-volatile memory element
24	Logical element
100, 200, 400	Electronic circuit
110, 210, 210', 210", 410, 410', 410"	Bit cell
112, 212, 212', 212", 412, 412', 412"	Resistive-switching element
114, 214, 214', 214", 414, 414', 414"	Access transistor
120, 220, 420	Row driver
122, 222, 222', 222", 422, 422', 422"	Row line
130, 230, 430	Column driver
132, 232, 432	Column line
140, 240, 440	Write current
150, 250, 450	Read current
160, 260, 460	Readout circuit
270, 470	Logic current
300	State diagram
310	Switching probability
320	Current or voltage level applied
322	Minimum reliable switching current I_wr0
323	Maximum reliable non-switching current I_rd0
325	Target bit cell current I_T1
326	Target bit cell current I_T3
328	Source bit cell current I_S1
329	Source bit cell current I_S2
330	High-to-low resistance switching dynamics
350	Modulation of target bit cell current
370	Reliable switching region
380	Reliable non-switching region

Claims

1. Electronic circuit (200, 400) comprising a plurality of bit cells (210, 410) arranged in an array and being selectable by row lines (222, 422) and column lines (232, 432), at least one row driver (220, 420), at least one column driver (230, 430), and a readout circuit (260, 460), wherein each bit cell (210, 410) comprises an access transistor (214, 414) and a non-volatile resistive-switching element (212, 412) with at least two resistance states,

characterized in that

the row driver (220, 420) and the column driver (230, 430) are capable to simultaneously apply a selecting voltage V_s to a first row line (222, 422) to select a target bit cell (210, 410), a pre-selecting voltage V_p-s to a second row line (222', 422') to select a source bit cell (210', 410'), and a logic current I_imp to at least one column line (232, 432), wherein the selecting voltage V_s is higher than the pre-selecting voltage V_p-s.

2. Electronic circuit (200, 400) according to claim 1, characterized in that the resistive-switching element (212, 412) has a low resistance state and a high resistance state.

3. Electronic circuit (200, 400) according to any of the preceding claims, characterized in that the resistive-switching element (212, 412) has a bipolar switching characteristic so that the resistance state of the resistive-switching elements (212, 412) is changed from a first state to a second state by a current or voltage impulse in a first direction, and from the second state to the first state by a current or voltage impulse in the opposite direction, where a critical current I_H-to-L or critical voltage has to be applied for switching.

4. Electronic circuit according to claim 3, characterized in that the resistive-switching element (212, 412) has an asymmetric switching characteristic and the logic current I_imp has the same polarity as the current I_H-to-L required to switch the resistive-switching element (212, 412).

5. Electronic circuit (200, 400) according to claims 1 or 2, characterized in that the resistive-switching element (212, 412) has a unipolar switching characteristic so that the resistance state of the resistive-switching elements (212, 412) is changed from a first state to a second state by a current or voltage of a first amplitude, and from the second state to the first state by a current or voltage impulse of a second amplitude, where a critical current I_H-to-L or critical voltage has to be applied for switching.

6. Electronic circuit according to any of the claims 3 to 5, characterized in that the logic current I_imp has an amplitude higher than the critical current I_H-to-L to enforce a desired switching event in the resistive-switching element (212, 412) of the target bit cell but small enough to prevent undesired switching events of the source or the target bit cell.

7. Electronic circuit according to claim 6, characterized in that the ratio of the current I_imp to the current I_H-to-L required to switch the resistive-switching element (212, 412) is between 1 and 2.

8. Electronic circuit according to any of the claims 3 to 5, characterized in that the logic current I_imp has the same amplitude as the current I_H-to-L and is applied at a pulse duration that is long enough to enforce a desired switching event in the resistive-switching element (212, 412) of the target bit cell and short enough to prevent undesired switching events of the source or the target bit cell.

9. Electronic circuit according to claim 8, characterized in that the current pulse I_imp is applied at a pulse duration that is 2 - 3 orders of magnitude longer than the pulse duration of the current I_H-to-L.

10. Electronic circuit according to any of the preceding claims, characterized in that the resistive-switching elements (212, 412) are magnetic tunnel junction (MTJ) devices, preferably Spin-Transfer-Torque (STT) MTJ devices, and the access transistors (214, 414) are CMOS transistors.

11. Method to perform the logic operation material implication (IMP) or negated material implication (NIMP) on a non-volatile resistive memory array comprising a plurality of bit cells (210, 410) being selectable by row lines (222, 422) and column lines (232, 432), wherein each bit cell (210, 410) comprises a non-volatile resistive-switching element (212, 412) with at least two resistance states, and an access transistor (214, 414), at least one row driver (220, 420), at least one column driver (230, 430), and a readout circuit (260, 460),

characterized in that

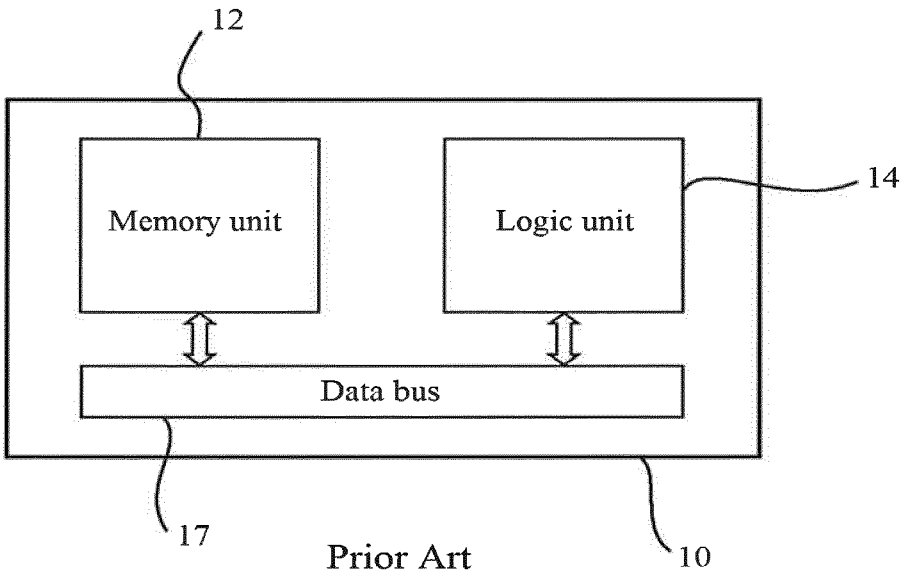
simultaneously the row driver (220, 420) applies a selecting voltage V_s to a first row line (222, 422) to select a target bit cell (210, 410) and a pre-selecting voltage V_p-s to a second row line (222', 422') to select a source bit cell, wherein V_s is higher than V_p-s, and the column driver (230, 430) applies a logic current I_imp to at least one column line (232, 342).

12. Method according to claim 11, characterized in that the logic current I_imp has a higher amplitude than a critical current I_H-to-L required to switch the resistive-switching element (212, 412) of the target bit cell from a high resistance state to a low resistance state but small enough to prevent undesired switching events.

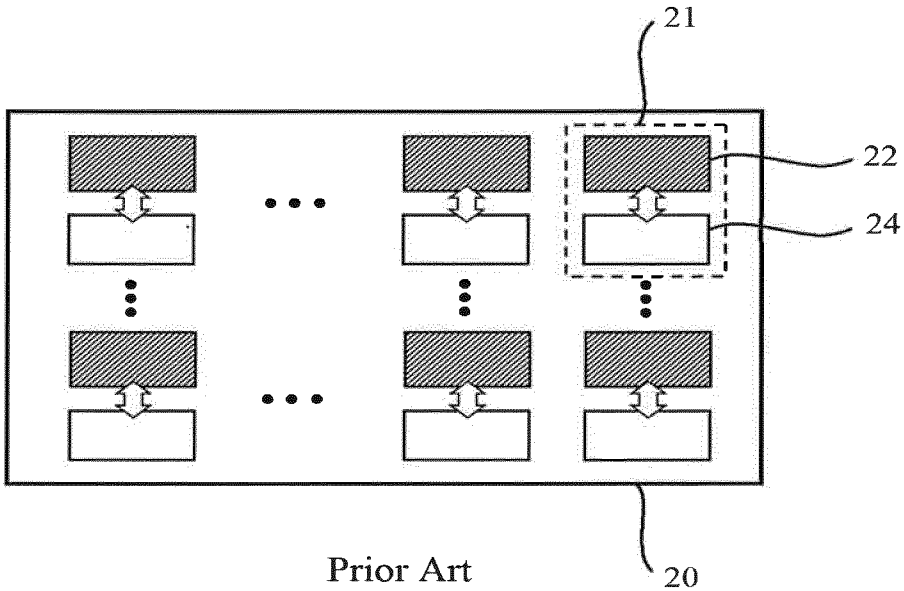
13. Method according to claim 12, characterized in that the ratio of the current I_imp to the current I_H-to-L is between 1 and 2.

14. Method according to claim 11 or 12, characterized in that the logic current I_imp is applied at a pulse duration that is long enough to enforce a desired switching event in the resistive-switching element (212, 412) of the target bit cell, but still short enough to prevent undesired switching events.

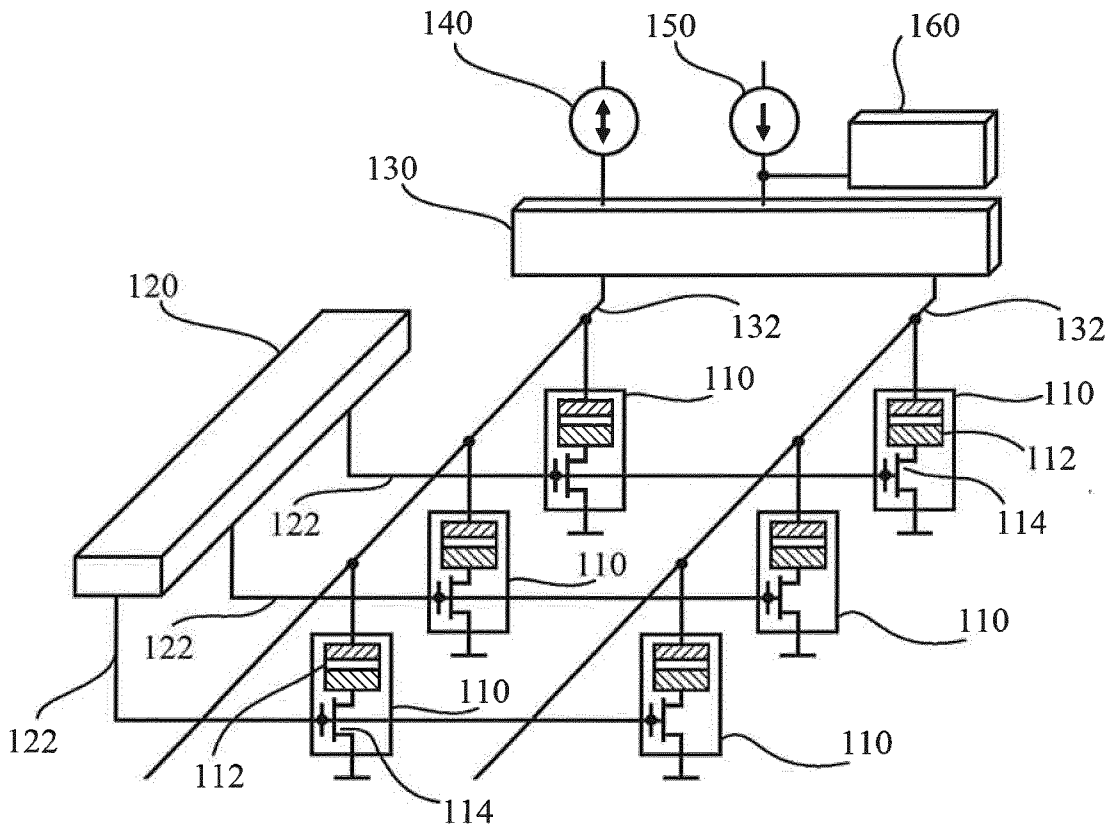
15. Method according to claim 14, characterized in that the current pulse I_imp is applied at a pulse duration that is 2-3 orders of magnitude longer than the pulse duration of the current I_H-to-L.



Prior Art
Figure 1A



Prior Art
Figure 1B



Prior Art
Figure 2

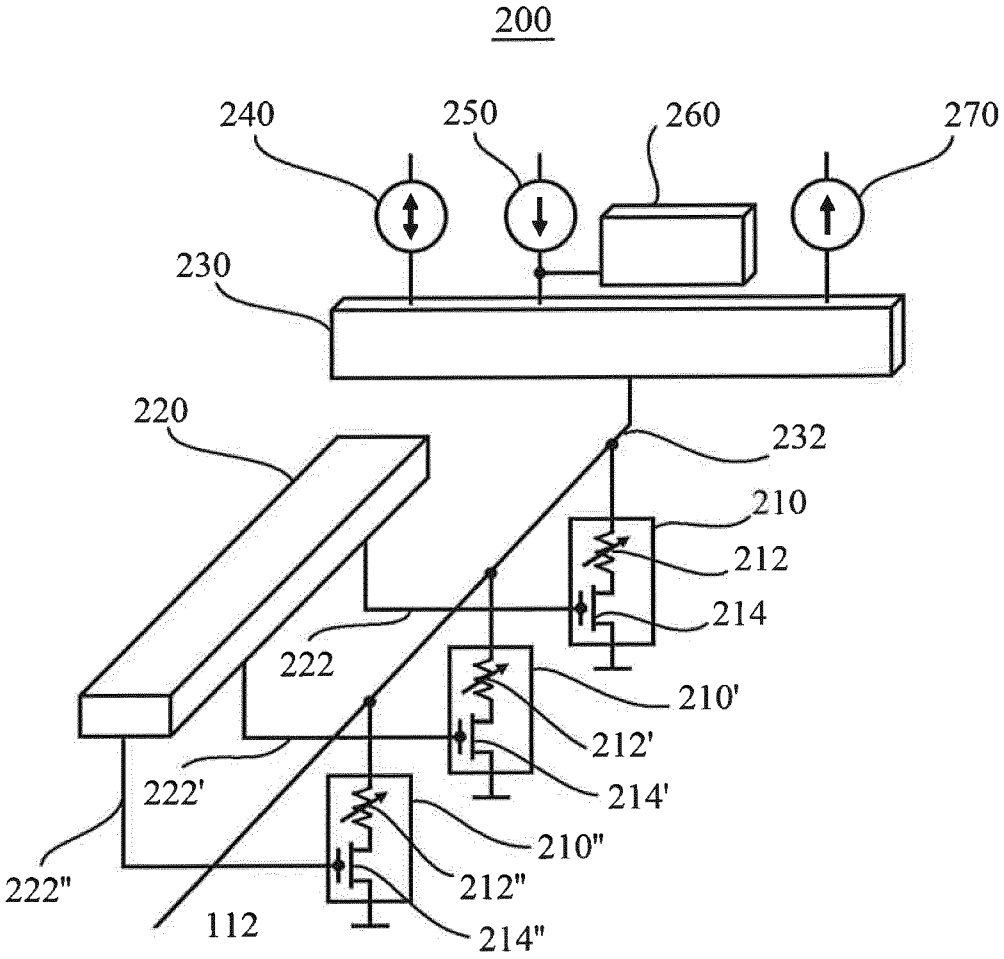

200
240
250
260
270
230
220
232
210
212
214
222
210'
212'
214'
222'
210"
212"
222"
112
214"

Figure 3

$T\_n+1 \leftarrow T\_n \text{ NIMP } S\_n$

	Initial state		Current		Final state	
Case	Source (S_n)	Target (T_n)	Source	Target	Source (S_n+1)	Target (T_n+1)
1	HRS (1)	HRS (1)	I_S1<I_rd0	I_T1>I_wr0	HRS (1)	LRS (0)
2	HRS (1)	LRS (0)	I_S2<I_rd0	——	HRS (1)	LRS (0)
3	LRS (0)	HRS (1)	——	I_T3<I_rd0	LRS (0)	HRS (1)
4	LRS (0)	LRS (0)	——	——	LRS (0)	LRS (0)

Figure 4A

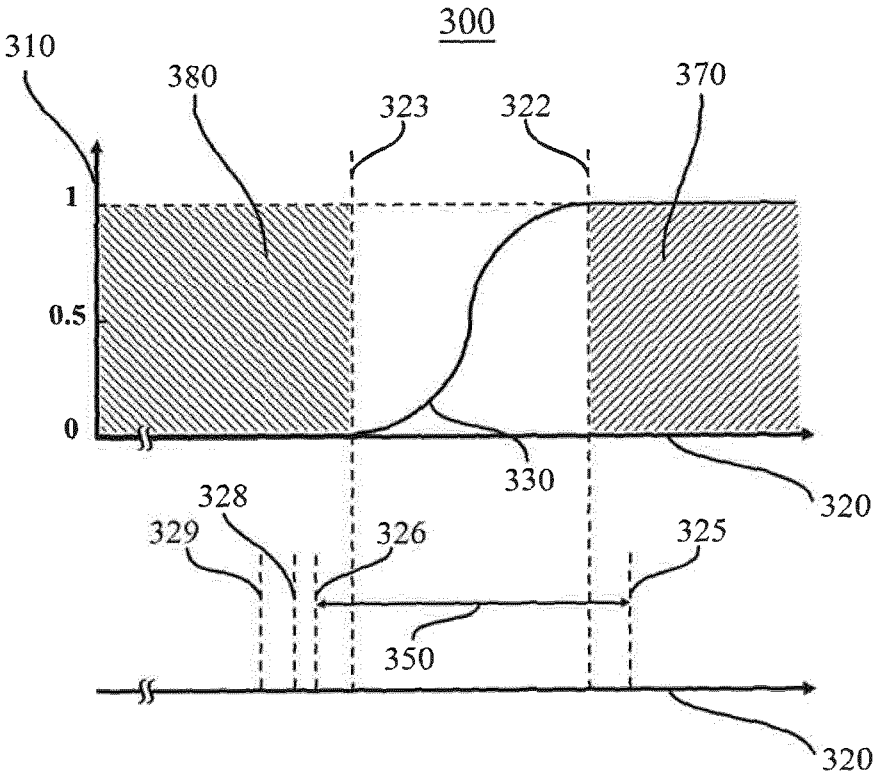


Figure 4B

	Current	Voltage		
Step	Column Line	C	C'	C''
1: TRUE	I_L-to-H	——	——	V_s
2: NIMP	I_imp	V_p-s	——	V_s
3: NIMP	I_imp	——	V_p-s	V_s

Figure 5A

$$C''_{n+3} \leftarrow C_n \text{ NOR } C'_n$$

	Initial state		Step 1	Step 2	Step 3
Case	C_n	C'_n	C''_n+1	C''_n+2	C''_n+3
1	HRS (1)	HRS (1)	HRS (1)	LRS (0)	LRS (0)
2	HRS (1)	LRS (0)	HRS (1)	LRS (0)	LRS (0)
3	LRS (0)	HRS (1)	HRS (1)	HRS (1)	LRS (0)
4	LRS (0)	LRS (0)	HRS (1)	HRS (1)	HRS (1)

Figure 5B

$T\_n+1 \leftarrow S\_n \text{ IMP } T\_n$

	Initial state		Final state	
Case	Source (S_n)	Target (T_n)	Source (S_n+1)	Target (T_n+1)
1	HRS (0)	HRS (0)	HRS (0)	LRS (1)
2	HRS (0)	LRS (1)	HRS (0)	LRS (1)
3	LRS (1)	HRS (0)	LRS (1)	HRS (0)
4	LRS (1)	LRS (1)	LRS (1)	LRS (1)

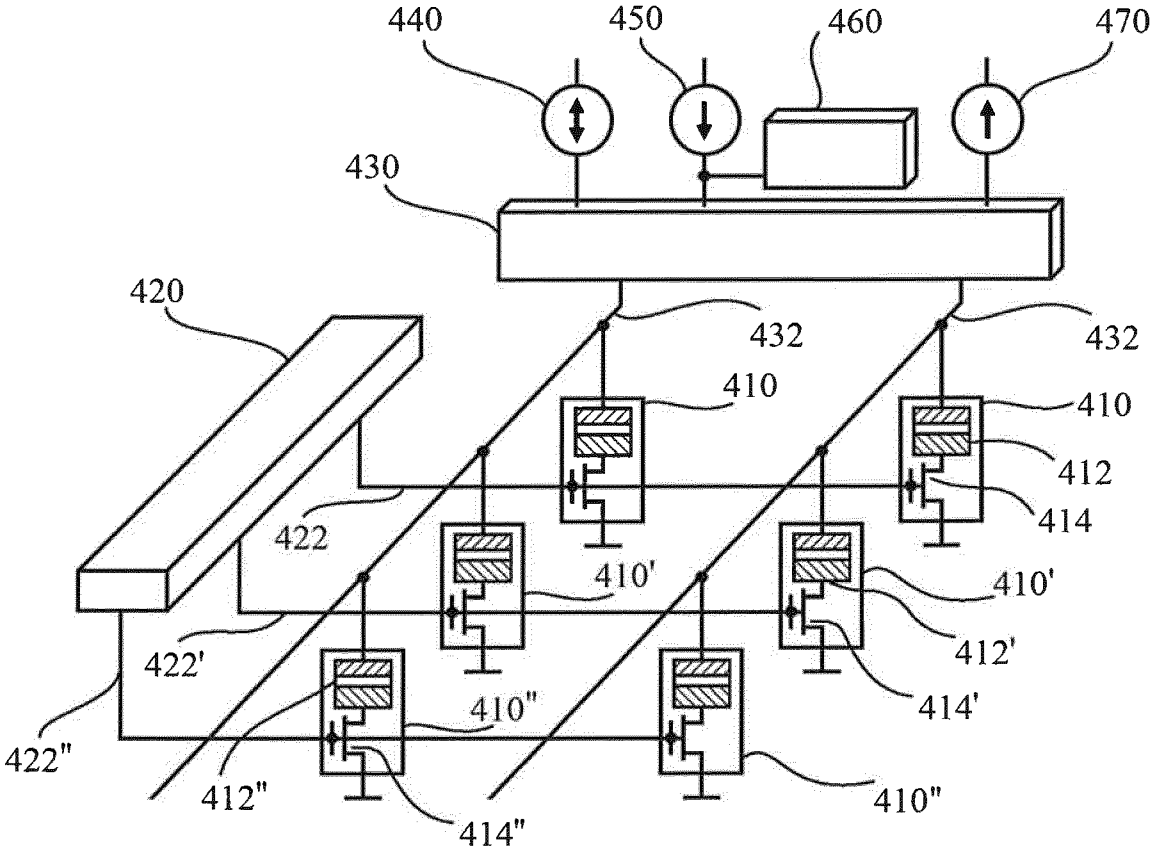
Figure 6A

$C''\_n+3 \leftarrow C\_n \text{ NAND } C'\_n$

	Initial state		Step 1	Step 2	Step 3
Case	C_n	C'_n	C''_n+1	C''_n+2	C''_n+3
1	HRS (0)	HRS (0)	HRS (0)	LRS (1)	LRS (1)
2	HRS (0)	LRS (1)	HRS (0)	LRS (1)	LRS (1)
3	LRS (1)	HRS (0)	HRS (0)	HRS (0)	LRS (1)
4	LRS (1)	LRS (1)	HRS (0)	HRS (0)	HRS (0)

Figure 6B

400


440
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460
470
430
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412
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422
410'
410'
412'
414'
422'
410"
422"
412"
414"
410"

Figure 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2013/073707

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C11/16 G11C13/00 H03K19/177
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	HIWA MAHMOUDI ET AL: "MTJ-based implication logic gates and circuit architecture for large-scale spintronic stateful logic systems", 2012 PROCEEDINGS OF THE EUROPEAN SOLID-STATE DEVICE RESEARCH CONFERENCE (ESSDERC), 1 September 2012 (2012-09-01), pages 254-257, XP055059245, DOI: 10.1109/ESSDERC.2012.6343381 ISBN: 978-1-46-731706-1 pages 256-257; figures 1,6,7	1-15
A	EP 1 557 841 A2 (SONY CORP [JP]) 27 July 2005 (2005-07-27) paragraphs [0021] - [0030], [0115]; figure 6A	1-15

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 January 2014	17/01/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Havard, Corinne

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2013/073707

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	BORGHETTI J ET AL: "'Memristive' switches enable 'stateful' logic operations via material implication", NATURE: INTERNATIONAL WEEKLY JOURNAL OF SCIENCE, NATURE PUBLISHING GROUP, UNITED KINGDOM, vol. 464, no. 7290, 8 April 2010 (2010-04-08), pages 873-876, XP002608177, ISSN: 0028-0836, DOI: 10.1038/NATURE08940 the whole document -----	1-15

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2013/073707

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EP 1557841 A2	27-07-2005	CN 1722302 A	18-01-2006
		EP 1557841 A2	27-07-2005
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		TW I261838 B	11-09-2006
		US 2005174840 A1	11-08-2005