Observation of Normally Distributed Energies for Interface Trap Recovery After Hot-Carrier Degradation

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***Abstract*— We investigate the temperature accelerated recovery from hot-carrier (HC) damage with the help of local polycrystalline heating structures in n-MOSFETs designed for power applications. These devices have a rather thick gate oxide and long channel, which assures that mainly interface traps are created through the HC stress. We further verify with frequency-dependent charge pumping that in our devices border traps are of vanishing importance compared to interface traps. We analyze the time and temperature dependence of the recovery of the interface traps after HC stress using models from the literature. The data are fairly consistent with the assumption of interfacial silicon dangling bonds that become passivated by hydrogen. The forward passivation energy is found to be normally distributed because of the distribution of atomic defect configurations. The distribution parameters are independent of the overall degradation level which shows that the passivation process is limited by the bond association kinetics rather than hydrogen supply. Our results are of importance for HC research as well as for the ongoing discussion regarding the quasi-permanent component of bias temperature instability.**

***Index Terms*— Automotive electronics, bias temperature instability, high-temperature techniques, hot carrier degradation, MOSFETs, oxide and interface defects, power MOSFET, semiconductor device reliability, temperature annealing.**

I. Introduction

HOT-carrier (HC) degradation is a major reliability issue for MOSFETs [1], [2]. Despite the considerable progress in understanding the degradation effect [3], the exact microscopic transitions that take place at the MOSFET interface or in the oxide remain unresolved. Conventionally, the HC-induced degradation buildup is analyzed with respect to stress time and bias to advance the understanding of the HC effect. By contrast, we investigate here the recovery from HC damage [4]–[6], through baking the degraded device with an *in situ* heating structure [7]. We analyze the temperature and time dependence of the recovery after HC stress and compare our results with previously published models. We observe that the recovery closely follows the kinetics of interface trap passivation by hydrogen [8], [9].

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II. Experimental Details

We perform HC degradation experiments on a 100 μm wide and 6 μm-long n-MOSFET with a 30-nm-thick gate oxide to minimize other parasitic degradation effects. In particular, using an n-MOSFET instead of a p-MOSFET eliminates a possible occurrence of negative bias temperature instability (BTI). Even though positive BTI may occur in n-MOSFETs, the few volts applied to the gate during HC stress cause an electric field less than 1 MV/cm, which is a way too small for any significant positive BTI.

The n-MOSFET under test is surrounded by two polycrystalline silicon wires that permit local Joule heating within seconds to temperatures above the highest temperature (200 °C) of the thermo chuck system. The power needed to elevate the device temperature T_{dev} to a certain value is determined in a calibration before stress, by making use of the temperature dependence of the drain current [7]. T_{dev} consequently reflects the temperature of the Si–SiO_2 interface in the recovery bake phases after stress.

To find the worst case biasing conditions for HC stress, we measure the dependence of the substrate current on the gate voltage for large drain biases [1]–[3]. We obtain a maximum substrate current at $V_{\mathrm{D}} = 8$ V and $V_{\mathrm{G}} = 3.8$ V and use this biasing point for the subsequent HC recovery experiments.

To verify that the HC stress creates mainly interface traps, we perform charge pumping (CP) measurements with variable frequency but constant rise/fall times. For such an experiment, the number of charges pumped per cycle $N_{\mathrm{CP}} = I_{\mathrm{CP}}/(qfA)$ is supposed to stay constant for ideal interface traps [10]. There is, however, usually a small increase of N_{CP} with decreasing f because of border traps [11] with emission and capture time constants $\tau \lessapprox 1/(2f)$. As shown in Fig. 1, we observe that the HC stress creates $\approx 10^{10}$ cm^{-2} interface traps but only $\approx 10^{9}$ cm^{-2} border traps. Therefore, we conclude that we indeed analyze to a large extend the recovery characteristics of fast responding traps at the interface.

Fig. 2 shows a constant base level CP measurement of an n-MOSFET before and after HC stress, as well as after

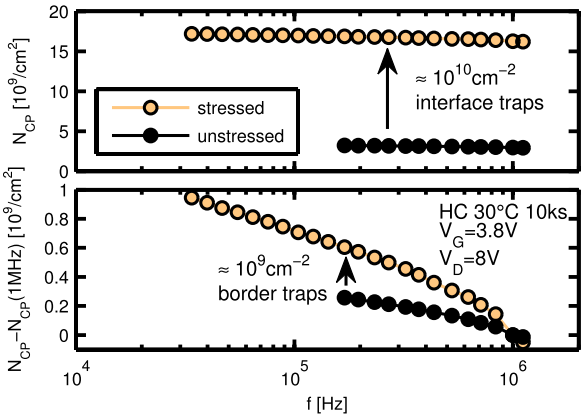

Fig. 1. Frequency-dependent CP measurement before and after HC stress. The HC stress increases the number of interface traps, here defined as traps with emission and capture time constants smaller than $\approx 0.5\ \mu$s (upper plot). In contrast, the number of border traps (here defined as traps with time constants larger than $\approx 0.5\ \mu$s) created during HC stress is roughly one order of magnitude smaller.

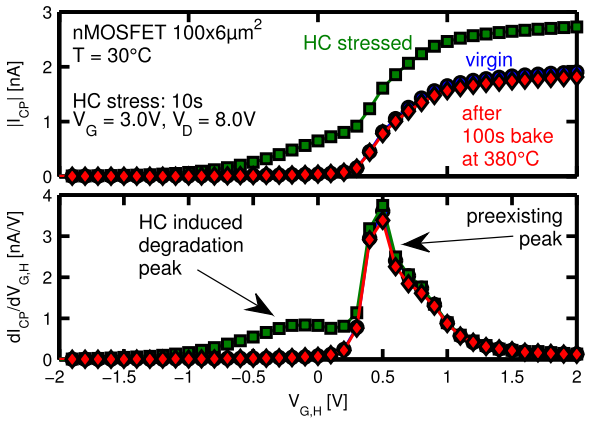

Fig. 2. Upper plot shows constant base level (−5 V) CP characteristics at 625 kHz with rising and falling slopes of 50 ns/V. The HC-induced increase in the CP current can be fully removed with the short bake phase. The derivative of the characteristics (bottom plot) shows that the increase of the I_{CP} is due to a second degradation-induced peak that is due to the strongly localized buildup of charges near the drain junction [10].

a subsequent short high temperature pulse. The HC stress increases the maximum CP current because of newly created interface traps. The derivative of the constant base level CP characteristic with respect to the gate voltage allows to investigate the lateral position of these defects (see [10] for details). The first, pre-existing peak marks the CP threshold voltage where most of the area of the MOSFET becomes inverted [10]. This first peak is unaffected by the HC stress or the bake phase. However, through the HC stress a second peak evolves which hints for strongly localized interface traps near the drain junction, which is characteristic for HC induced damage [2], [3]. Only these previously created traps are annealed through the temperature treatment.

To analyze the dynamics of the temperature accelerated recovery effect, we perform isothermal annealing experiments after HC stress. For this, we analyze the recovery behavior at various temperatures between 150 °C and 275 °C. We interrupt the recovery phases regularly to analyze the remaining level of degradation by measuring the maximum CP current always at 30 °C. The sensitivity of the CP measurement

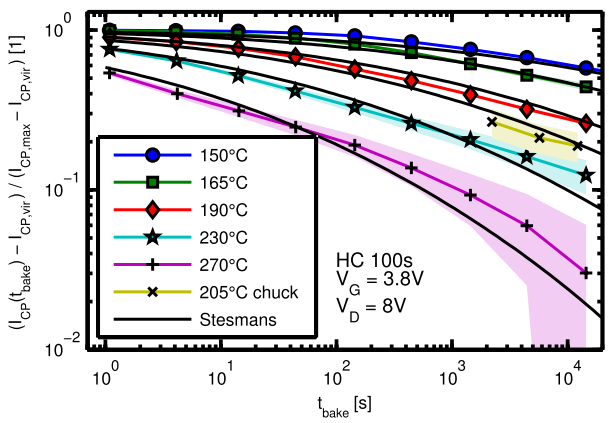

Fig. 3. Baking the device at zero gate and drain bias decreases the number of HC-induced traps visible in the maximum CP current. It is thereby insignificant whether the temperature is provided by the poly-heater (standard case in this letter) or the thermo chuck (trace labeled chuck). The shaded areas correspond to the confidence intervals of the I_{CP} measurement. In addition, the result of a fit to the model by Stesmans (1) [8] is shown.

is about 10^8 cm^{-2} charges pumped per cycle, judged from the amplitude of noise in a time-resolved CP measurement. This high sensitivity is only given on large area devices because of the proportionality of the CP current to the device area. The change of the subthreshold slope of our devices through HC stress is not large enough to be analyzed. This is because this technique is most sensitive to interface traps in the highest doped region of the channel, which is in the middle of the device and therefore not affected by HC degradation. For illustration, Fig. 3 shows the relative decrease of the CP current over time. All experiments are performed on a single device because a final bake step at 380 °C for 100 s restores the virgin interface trap density of 3×10^9 cm^{-2} within a 10% error.

III. Recovery Dynamics Analysis

We compare the decrease of the number of HC-induced traps with different models, as e.g., single energy-valued thermal emission [5] or the reaction–diffusion framework [6]. We observe, however, convincing agreement only with the model of Stesmans for the passivation of P_b centers with molecular hydrogen [8]

$$[P_b]/N_0 = \frac{1}{\sqrt{2\pi}\sigma_{E_f}} \int_{E_f-3\sigma_{E_f}}^{E_f+3\sigma_{E_f}} \exp\left(-\frac{(x-E_f)^2}{2\sigma_{E_f}^2}\right) \times \exp\left(-k_{f,0}[H_2]t_{\text{bake}} \exp\left(-\frac{x}{kT}\right)\right) dx \quad (1)$$

where $[H_2]$ is the volume concentration of molecular hydrogen in amorphous SiO_2 after [12] and $k_{f,0}$ is the forward rate constant. A peculiarity of this model is that the forward passivation energy E_f is normally distributed with variance σ_{E_f}.

The three parameters E_f, σ_{E_f}, and $k_{f,0}$ of (1) and their confidence intervals are obtained by fitting (1) to the data of Fig. 3, where we use the inverse of the error of the CP measurement as weights for the least squares solution. We obtain $E_f = (1.6 \pm 0.1)$ eV, $\sigma_{E_f} \approx (0.20 \pm 0.02)$ eV and $k_{f,0} = 7 \times 10^{-4}(6 \times 10^{-5}/9 \times 10^{-3})$ cm^3/s. These values are

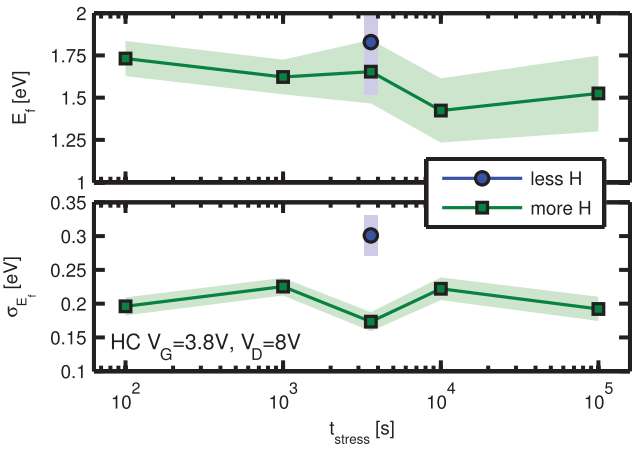

Fig. 4. Dependence of the recovery activation energy and its variance on the stress duration for a device with more/less H at the interface [14], [15]. The shaded areas are 95% confidence intervals for the parameter estimation of the E_f and σ_{E_f} values. For the device with more H, the 100 s stress leads to $\approx 10^9$ cm^{-2} increase of charges pumped/cycle, and the 100 ks stress in contrast leads to a $\approx 2 \times 10^{10}$ cm^{-2} rise. Still, despite this difference in the absolute degradation level, no large change of E_f and σ_{E_f} is observed, also independent of the H passivation degree.

close to the values reported for the passivation of the defects of the P_b center family at the (100) Si–SiO$_2$ interface with hydrogen, P_{b0}: $E_f \approx 1.51$ eV, $\sigma_{E_f} \approx 0.14$ eV and $k_{f,0} \approx 1.43 \times 10^{-6}$cm^3/s and P_{b1}: $E_f \approx 1.57$ eV, $\sigma_{E_f} \approx 0.15$ eV and $k_{f,0} \approx 1.43 \times 10^{-6}$cm^3/s [8]. This is strong evidence that the HC-induced degradation of the device is indeed due to interface traps that later become passivated with hydrogen through temperature treatment. The somewhat larger values can either be because of the influence of the gate bias during annealing at high temperatures, as reported in [9], where a larger energy value was attributed to different charge states of the interface traps leading to different effective activation energies, or because of the strongly localized nature of the HC-induced P_b centers that changes the atomic conditions of the reaction site [13].

In addition, we investigate the dependence of the activation energy and its variance on the stress time, as shown in Fig. 4. We do not observe any significant dependence of the passivation kinetics on the absolute degradation value. This indicates that independent of the number of interface traps and thus the number of previously released hydrogen in the vicinity of the interface trap, the passivation is always limited by the reaction of bond association [16], rather than by the availability of hydrogen.

Furthermore, we observe that the same experiment reveals similar estimations for E_f and σ_{E_f} on a device where a larger amount of titanium impedes the diffusion of hydrogen from the upper metal stack toward the Si–SiO$_2$ interface [14], [15] (see Fig. 4, device with less H). This device has a smaller amount of passivated P_b centers at the interface in the beginning and experiences therefore a smaller increase in the number of charges pumped/cycle (N_{CP} : 33×10^9 cm^{-2} $\longrightarrow$ 35×10^9 cm^{-2}) compared with the device with a well-passivated interface (N_{CP} : 3×10^9 cm^{-2} $\longrightarrow$ 12×10^9 cm^{-2}) for the same stress conditions.

IV. Conclusion

We investigated the temperature activation of interface trap recovery created through HC stress using local heating structures. We found that full recovery from HC-induced damage through temperature treatment was possible, which suggested a possibility to extend the reliability limit of HC susceptible devices. We observed that the recovery was consistent with a first-order thermally activated process, with normally distributed barriers. The parameters of this distribution were fairly consistent with the passivation of interfacial Si dangling bonds with hydrogen. Furthermore, the parameters of the distribution did not seem to depend on the absolute degradation level which was strong indication for a reaction-limited process. Our results provided valuable information on the passivation kinetics of interface traps in MOSFET devices that were also important for the understanding of other reliability issues such as the BTI.

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