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Impact of hot carrier degradation and positive bias temperature stress on lateral 4H-SiC nMOSFETs

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Abstract. We study the impact of positive bias temperature stress (PBTS) and hot carrier stress (HCS) on lateral 4H-SiC nMOSFETs. These degradation mechanisms are prominent in silicon (Si) based devices where both create oxide (OT) as well as interface traps (IT) [1, 2]. For SiC MOSFETs only limited information regarding these mechanisms is available [3–5]. We transfer the charge pumping (CP) technique, known from Si MOSFETs, reliably to SiC MOSFETs to learn about the nature of the stress induced defects.

Details of the experiment:

The measurements were performed on dedicated lateral nMOSFET test structures on 4H-SiC with an 80nm thick NO-annealed deposited oxide with 100μm channel width and 2μm length. We analyze interface traps with CP [6] because this technique allows to resolve very low trap densities compared to capacitance or conductance methods (in Si down to $\approx 10^9\text{cm}^{-2}\text{eV}^{-1}$). We do not observe a geometric component which recently questioned the applicability of CP for SiC MOSFETs [7]. Further, CP can be applied to SiC MOSFETs directly, alleviating the problem of having to draw conclusions from capacitance-voltage measurements obtained on large area MOS capacitors.

CP is performed by repeatedly switching ($f = 100$kHz) the gate voltage between full inversion ($V_\text{G} = 25$V) and full accumulation ($V_\text{G} = -25$V). The rising and falling slopes are $13.33\text{V}/\mu\text{s}$. The resulting CP current (I_CP) between the source/drain and the bulk is proportional to the mean density of interface traps (D_IT) in an energy range (2.9 ± 0.1)eV symmetrically around mid-gap (at room temperature). This energy range is calculated [6] by

$$\Delta E_\text{CP} = 2k_\text{B}T \ln\left(\frac{\Delta V_\text{G}}{v_\text{th}\sigma n_\text{i}(V_\text{TH} - V_\text{FB})\sqrt{t_\text{r}t_\text{f}}}\right), \tag{1}$$

where $k_\text{B}T$ is the Boltzmann constant times the temperature and $\Delta V_G/(V_\text{TH} - V_\text{FB}) = 50\text{V}/6.5\text{V}$ is the ratio between the pulse amplitude and the difference between the threshold and the flat-band voltage. The remaining parameters depend on the type of semiconductor and are not unambiguously determined for 4H-SiC. However, we defined a range of possible values and calculated the propagating maximum error for the CP energy range and the D_IT. The used values are $v_\text{th} = (0.75 \ldots 2) \times 10^7\text{cm/s}$ for the thermal drift velocity [8], $\sigma = \sqrt{\sigma_n\sigma_p} = (10^{-18} \ldots 10^{-16})\text{cm}^2$ for the geometric mean of the electron and hole capture cross-section of the interface traps, respectively [9] and $n_\text{i} = (0.5 \ldots 1) \times 10^{-8}\text{cm}^{-3}$ for the intrinsic carrier density [10].

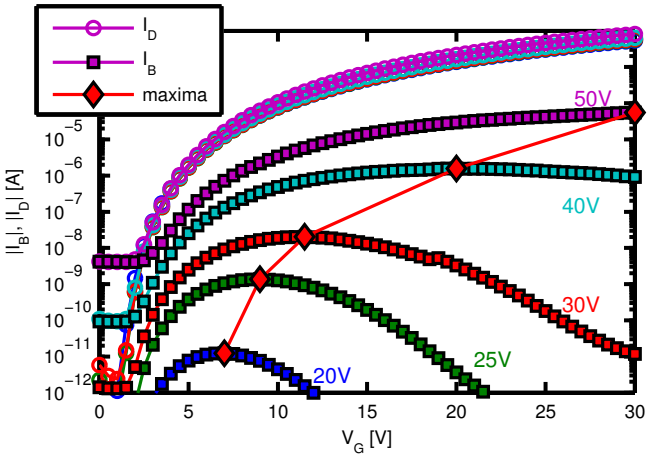

Fig. 1: Bulk I_B and drain I_D current as a function of gate voltage V_G for several high drain voltages V_D. The substrate current peak increases and shifts towards larger V_G values with increasing V_D. We observed a destructive breakdown for $V_D = 60$V.

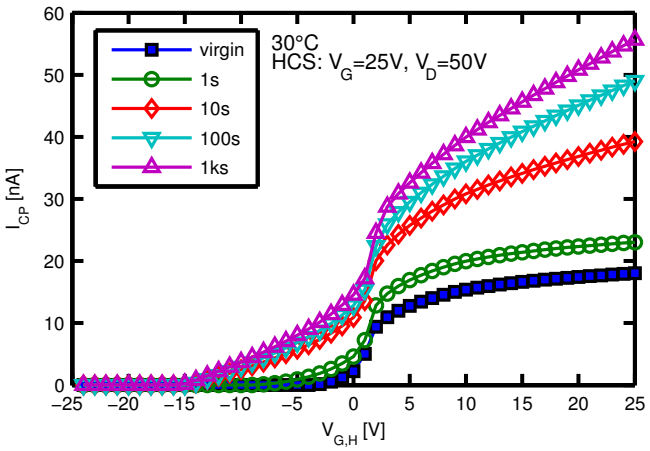

Fig. 2: Constant base level CP measurement before and after HCS. A large increase in the number of interface traps is observed.

Hot carrier degradation:

To test whether hot carriers can be created in the channel of the device under test, we measure the bulk current as a function of the V_G for high drain bias, as depicted in Fig. 1. We indeed observe a bulk current because the electrons accelerated from the source gain sufficient kinetic energy such that they cause impact ionization at the interface region near the drain junction [2]. This impact ionization creates electron-hole pairs which are separated by the space charge region of the reverse biased drain-bulk pn-junction and may cause interface degradation. The mechanism is most efficient (peak in I_B) for large drain bias and $V_G \approx 1/\alpha \times V_D$ with $\alpha = 2$–3, as expected for long channel devices of Si technology [2]. As depicted in Fig. 2, the CP current increases considerably due to HCS. In terms of D_{IT}: from $(1.9 \pm 0.1) \times 10^{11}\text{cm}^{-2}\text{eV}^{-1}$ to $(6.0 \pm 0.4) \times 10^{11}\text{cm}^{-2}\text{eV}^{-1}$ after 1ks stress. These newly created IT decrease the drain current of the device as visible in the transfer characteristic, see Fig. 3. The induced threshold voltage shift depends strongly on the readout bias.

Positive bias temperature stress:

To study the impact of BTS on 4H-SiC nMOSFETs, we subjected a device to $V_G = 50$V (≈ 6MV/cm), $V_D = 0$V at 200°C chuck temperature to accelerate the degradation. The transfer characteristic of the device is shifted parallel along the voltage axis towards larger V_G values as depicted in Fig. 4. This indicates the creation of $1.9 \times 10^{11}\text{cm}^{-2}$ OT after 1ks stress when assuming the charges at the SiC-SiO_2 interface. The readout bias independence indicates that the defects created through PBTS are located within the SiO_2 and cannot exchange charge with the carriers in the channel during the transfer characteristic measurement. I.e. charge exchange with these defects occurs only on larger timescales.

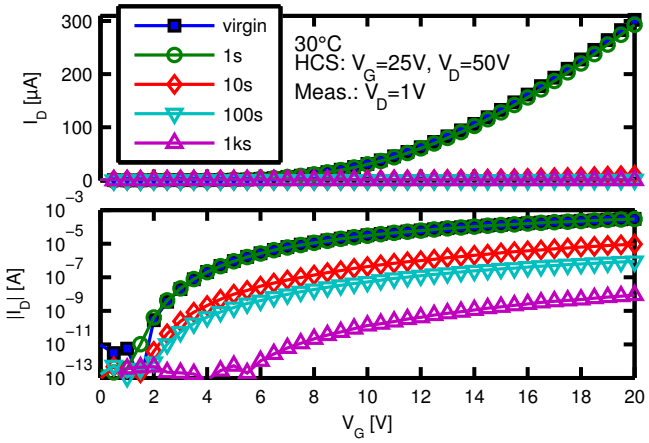

Fig. 3: Transfer characteristics after HCS in linear and logarithmic scale. The stress decreases the drain current of the device largely.

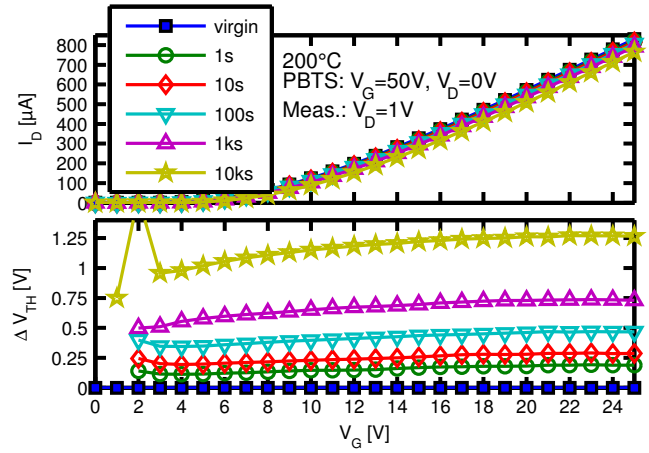

Fig. 4: Change of the transfer characteristic (upper plot) with increasing PBTS time. The V_{TH} shift occurs parallel along the voltage axis, as also visible when plotting the horizontal difference between the characteristics (lower plot).

In accordance, the CP current stays almost constant with increasing stress time [5] if compared to HCS (c.f. Fig. 5).

Discussion:

In the degradation after HCS and PBTS we distinguish between OT and IT by analyzing the transfer characteristics and the CP current of dedicated test structures. We find that only the high energetic carriers during HCS can cause interface degradation measurable with CP. PBTS causes the creation of gate bias independent negative oxide charges consistent with results for negative BTS [5]. We explain our results by assuming that IT at the SiC-SiO_2 interface are passivated by nitrogen atoms [11] which are strongly bonded to the interfacial Si or C atoms [12] and are therefore only dissociated by the high

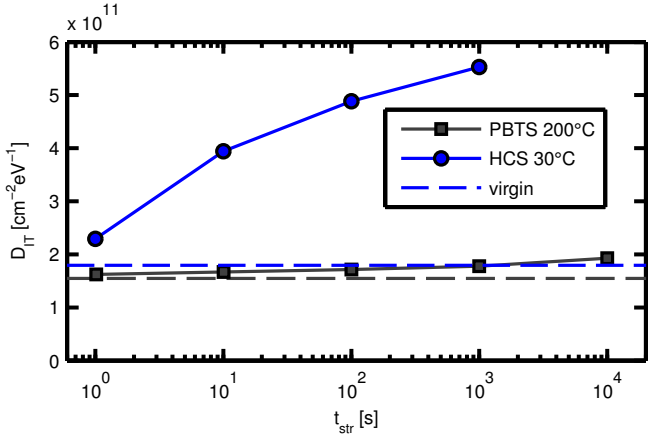

Fig. 5: Change of the density of interface traps measured with CP over stress time for HCS and PBTS. The smaller CP energy range at 200°C for PBTS compared to 30°C [6] for HCS was considered by calculating the energy range with (1). The remaining difference in the virgin I_{CP} is due to device-to-device variations.

energetic carriers existent during HCS. In contrast, PBTS causes a degradation because of field and temperature dependent bond dissociation [1, 13] of precursor defects within the SiO_2 layer.

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