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Application of the complete tableau approach in JANAP

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So-called *third generation* techniques offer possibilities to improve the efficiency of circuit simulation programs form the purely algorithmic point of view e.g. better decomposition techniques. Another important point is the availability of an efficient and flexible method to describe semiconductor devices and macro models. We like to present a better initial formulation of network equations in order to fully utilize modern numerical methods and to allow a simple realization of nonstandard network elements e.g. switches. We combine all branch voltages, branch currents, branch charges, branch fluxes and artificial branch values to a *complete tableau.* With this formulation the charge conservation problem is solved. Based on our new formulation approach a program to simulate electrical networks called JANAP has been implemented.

1. INTRODUCTION

Since the early 1970's circuit simulation has evolved to a significant design aid for integrated circuit engineering. The present situation, however, reveals the need of more efficient and economic simulation tools in terms of computer resources and person power.

So-called *third generation* techniques offer possibilities to improve the efficiency of circuit simulation programs from the purely algorithmic point of view e.g. better decomposition techniques. Another important point is the availability of efficient and flexible methods to describe semiconductor devices and macro models. We present a better initial formulation of network equations in order to fully utilize modern numerical methods and to allow a simple realization of nonstandard network elements e.g. switches. The *modified nodal* formulation is perhaps the best established approach for network equations[47,48,38,12,37,7,58,41]. The node voltages and some artificial variables are treated as unknowns. As an alternative fairly generally accepted formulation the *sparse tableau approach* has to be cited[35,12]. This formulation technique combines node voltages, branch voltages and currents and possibly artificial variables into one tableau matrix with fixed sparsity and block structures. We combine all branch voltages, branch currents, branch charges, branch fluxes and artificial branch values to a *complete tableau* leading also to a fixed sparsity pattern and block structure. Node voltages of interest are treated by introducing a zero conductivity branch.

Based on our new formulation approach, a program to simulate electrical networks called JANAP has been implemented. JANAP stands for *Just Another Network Analysis Program.* The network equations are reduced by symbolic solution of all simple equations in the setup phase. We shall demonstrate that the final set of relevant network equations, owing to the complete tableau approach, is usually smaller than the set of nodal equations. The final, partly nonlinear equations are solved with a modified, adaptively damped Newton scheme. Transient analysis is accomplished by fully implicit backward difference formulae with automatic time step and order control. Latency is automatically accounted for with zero order integration and bypassing of Jacobian evaluations. The

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Jacobian is decomposed from block lower triangular form. The decomposition is automatically bypassed for latent blocks.

2. PHILOSOPHY BEHIND JANAP

Most of the existing circuit simulation programs impose a lot of restrictions on the description of the parameters of the intrinsic ideal circuit elements. Typical restrictions are:

- resistance or conductance has to be larger than zero
- magnetic coupling has to be in the range between zero and one
- capacitance and inductance has to be larger than zero
- The network has to consist of only one component, i.e., there should be one common ground node. If one wants to implement a switch as basic circuit element one cannot grant this condition for all cases.
- Most of the parameters can only be constants.
- No inductor-only loops or capacitor-only nodes.

This restrictions make it very hard or impossible to describe the real behavior of semiconductors or larger building blocks (gate, operational amplifier) using the built-in ideal circuit elements. In Fig. 1 a simplified model of a field effect transistor is shown. Most of the existing circuit simulation programs cannot simulate this circuit because node A is a capacitor only node. One can argument that this circuit cannot be realized in real world because there is always some conductivity somewhere. This is true indeed, however a circuit simulation program on the other side has to simulate the given circuit of *ideal* elements in a consistent manner. This circuit is a model of a *real* circuit, which has a defined accuracy and models only a defined subset of the *real* behavior of the circuit.

Simulations such as shown in Fig. 1 occur for switched capacitor networks as well. The problem is well known as the *charge conservation problem*[59,55,26].

The main goals of our new circuit simulation program JANAP and the complete tableau approach are:

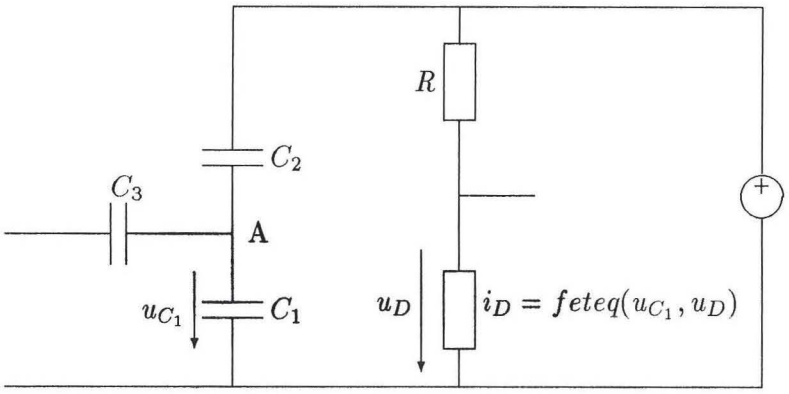

Fig. 1. Simplified FET-model

- to not impose restrictions on the description of circuit elements.
- to solve the given circuit of *ideal* elements in a consistent way, even if the circuit is not realistic.
- to allow switches and boolean controlled elements[3] as basic circuit elements.
- provide a flexible modeling technique to model the behavior of semiconductor devices and circuit building blocks (e.g. gate, operational amplifier) using the built-in ideal circuit elements.
- to allow the modeling of real elements with different accuracy (timing model, logic model, complete model).
- userfriendly interface.
- to use state-of-the-art numerical methods.

3. THEORETICAL FOUNDATION OF THE COMPLETE TABLEAU APPROACH

3.1 *Terminology*

A circuit simulation program uses *ideal* oneport (two terminal) elements or twoport elements (e.g. magnetic coupling, controlled sources) to describe the circuit to simulate. If one or more parameters of a oneport are controlled by a branch-value of one or more other branches, we have a multiport element.

An element is called *ideal* because of the following simplifications:

Size: The element and the complete circuit is infinitesimal small, i.e. the size of the element has no relevance. There is no timedelay in the element and the whole circuit.

Orientation: Location, orientation and motion of the element has no impact on the electrical behaviour of the element.

Force: No external forces such as gravitation influence the behavior of the element.

Field: The absolute values of the electrical and magnetic potential are of no relevance. Only the corresponding relative values are of importance for the simulation.

The state of an ideal oneport can be described by the parameter *time* and the electrical values *voltage*, *current*, *stored charge* and *stored flux*, i.e. the vector (t, i, v, q, ϕ). The behavior of the oneport can be specified implicit with the equation $F(t, i, v, q, \phi) = 0$. Depending on the nature of function F a oneport can be classified with some of the following attributes[9]:

Linearity: A oneport is said to be *linear* if function F is a set of linear functions of any variable at any time t[9].

Algebraic: A oneport is said to be *algebraic* if its set of equations F can be expressed symbolically by algebraic relationships. By an *algebraic relationship*, we mean any equation or system of equations involving *strictly algebraic* operations (no differentiation, integration, time delay, etc.) whose solution gives, at any time t, a subset of points in the $v-i$, $\phi-i$, $q-v$, and $q-\phi$ plane, respectively[9].

Dynamic: A oneport is said to be *dynamic*, if the element is not *algebraic*.

Timevariant: A oneport is said to be *time-invariant* if its constitutive function F does not depend explicitly on time[9].

Resistive: A purely resistive element does not store any charge or flux in its electromagnetic fields.

Capacitive: A oneport is capacitive if the stored charge of the element can be nonzero.

Inductive: A oneport is inductive if the stored flux of the element can be nonzero.

Memristiv: A oneport is memristive if there is a functional dependency of stored charge form stored flux or vice versa[11,8].

For linear oneports F can be written as a matrix equation:

$$A \cdot (1, i, v, q, \phi)^T = 0 \tag{1}$$

A, i, v, q and ϕ are constant or depend on time. The 1 in equation (1) represents the inhomogeneity introduced with energy sources. If equation (1) has no solution, the element can not exist. Conditions for the existence of a oneport can be found in Refs 10 and 13. The coefficients a_{xy} of equation system (1) with their practical meaning are compiled in Table 1. In Table 2 the constitutive relations of the well known ideal oneports are summarized.

It is possible to model the behavior of real oneports with two or more ideal oneports. If the topology of the model and the used ideal oneports satisfy some constraints, the model can be combined into one 'real' oneport which can be described with a single function F. The constitutive relations for the most important real oneports are summarized in Table 3.

Table 1. Coefficients of the constitutive relations of a oneport

Index of coefficient	coefficient	Unit	Meaning
i	I	[A]	Current source
i, v	G	[S]	Conductor
i, q	$\frac{d}{dt}$	[1/s]	represents electrical displacement
i, ϕ	ϕ	[1/H]	reciprocal inductivity
v	V	[V]	Voltage source
v, i	R	[Ω]	Resistor
v, q	S	[1/F]	Elastanz
v, ϕ	$\frac{d}{dt}$	[1/s]	represents induction voltage
q	Q	[C]	Charge source (electrostatic field source)
q, i	$\int dt$	[s]	represents generation of charge
q, v	C	[F]	Capacitor
q, ϕ	M_G	[S]	Memductance
ϕ	Φ	[Wb]	Flux source (magnetic field source)
ϕ, i	L	[H]	Inductor
ϕ, v	$\int dt$	[s]	represents generation of stored flux
ϕ, q	M_R	[Ω]	Memristor [11, 8]

Table 2. Constitutive relations for ideal twoports

Twoport	i	v	q	ϕ	r	s
ideal voltage source		V	0	0		
ideal current source	I		0	0		
resistor		$R \cdot i$	0	0		
conductor	$G \cdot v$		0	0		
inductivity		$\frac{d\phi}{dt}$	0	$L \cdot i$		0
capacitance	$\frac{dq}{dt}$		$C \cdot v$	0	0	
open switch		0	0	0		
closed switch	0		0	0		
norator			0	0		
memristor	0	0		$M_R \cdot q$		
memductance	0	0	$M_G \cdot \phi$			
nullator	0	0	0	0		

3.2 Electrical networks

To simulate the behavior of an electrical network an equation system has to be solved which consists of the constitutive relations of the network elements (oneports) and equations to describe to interconnection of the network elements.

The fundamental equations to describe the topology of an electrical network are the well known Kirchhoff's Laws. The Kirchhoff's Current Law $\sum_j i_j = 0$ describes the relations between the currents of the elements connected to one node or the elements of a cutset. i_j is the current of oneport j connected to the given node.

Table 3. Constitutive relations for real twoports

Twoport	i	v	q	ϕ
real voltage source	$V + i \cdot R$		0	
real current source	$I + v \cdot G$		0	
real coil	$\frac{dq}{dt}$	$Ri + \frac{d\phi}{dt}$	$C(Ri + v)$	$L(GRi - Gv - \frac{dq}{dt})$
real capacitor	$\frac{1}{1+GR}(v + \frac{dq}{dt}) - G\frac{d\phi}{dt}$		$C(Ri + v - \frac{d\phi}{dt})$	Li

The Kirchhoff's Voltage Law $\sum_j v_j = 0$ describes the relation of the voltage differences at the oneports contained within a loop of the network. v_j is the voltage difference between the nodes of oneport j, which is part of the loop.

Both laws can be written as matrix equations (2) and (3) respectively.

$$\mathbf{A} \cdot i = 0 \tag{2}$$

$$\mathbf{B} \cdot v = 0 \tag{3}$$

A is the incidence matrix and **B** the loop matrix of the network. i and v are the vectors of the currents and voltages of the oneports of the network. These two equation systems are usually enough for a description of the network. A complete description of the topology of networks with capacitor-only cutsets and inductor-only loops with the above equations to compute the DC operating point is not possible. Such networks may occur using specific models for field effect transistor as shown in Fig. 1. Another indeed relevant problem is the well known charge conservation problem[59,55,26] which is of particular importance for the simulation of switched capacitor filters, dynamic RAMs and any circuit which contains switches. The dual problem exists for flux and inductors. To solve this problems we have to find additional rules which describe the missing topological relations between the network elements.

First let us consider the problem of networks with capacitor-only cutsets.

We start with Maxwell's equations for the stationary electromagnetic field for the capacitor-only cutset.

$$\text{div } \mathscr{D} = \rho_{WA} \tag{4}$$

Next we apply the integral-theorem of Gauss

$$\int_V \text{div } \mathscr{D}\, dV = \oint_A \mathscr{D}\, dA = \int_V \rho_{WA}\, dV \tag{5}$$

On the surface of the volume defined by the capacitor-only cutset there are the plates of n capacitors, each with an area of A_j. The charge q_j on each of the plates is defined by equation (6)

$$q_j = \int_{Aj} \mathscr{D}\, dA \tag{6}$$

We can now combine equations (5) and (6) and obtain equation (7).

$$\sum_j q_j = \int_V \rho_{WA}\, dV \tag{7}$$

The initial charge of the volume of the capacitor-only cutset is defined to be zero. Charges can only be transferred through conductive paths into or out of the volume. Since no such paths cross the surface of the volume, no charge can enter into it or leak out from it. Therefore the charge within the volume will remain constant. Therefore $\int_V \rho_{WA}\, dV$ is 0 and equation (7) becomes (8)

$$\sum_j q_j = 0 \tag{8}$$

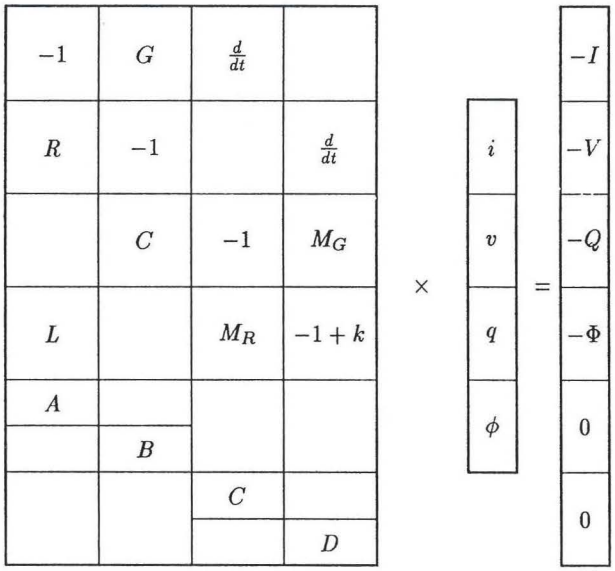

Fig. 2. Complete tableau matrix

Equation (8) is additional rule required to simulate capacitor-only cutsets. After adding this rule to the well known Kirchhoff rules we can compute the behavior for electrical networks with capacitor-only cutsets. Rule (8) looks like the traditional Kirchhoff current law. In contrast to the KCL this charge law holds for capacitor-only cutsets only. Therefore a new topology matrix is required to describe the capacitor-only cutsets.

Similar to the above charge law, an additional topology law (9) for the stored flux in inductor-only loops can be derived.

$$\sum_j \phi_j = 0 \tag{9}$$

This law is equivalent to Kirchhoff's voltage law but it holds for each inductor-only loop. Again we need a new topology matrix to describe all inductor-only loops.

If we have matrix C which describes the capacitor-only cutsets and matrix D to describe the inductor-only loops equations (8) and (9) can be written in matrix form:

$$\mathbf{C} \cdot q = 0 \tag{10}$$

$$\mathbf{D} \cdot \phi = 0 \tag{11}$$

The constitutive equations, the Kirchhoff laws and rules (10) and (11) can be combined into a *complete tableau* as shown in Fig. 2 for typical networks containing resistors, conductors, capacitors, inductors, current and voltage sources, memristors, magnetic coupling (indicated by matrix k) and controlled sources. The unknown vector consists of all currents and voltages as well as stored charges for capacitors and stored flux for inductors.

3.3 Generalized complete tableau approach

With the *complete tableau approach* described in the previous section it is now possible to simulate electrical networks without enforcing restrictions on the topology of the network. There may be only restrictions on the value of the circuit elements in the network to get a consistent solution (e.g. it is not possible to have a circuit with a voltage source and a zero value resistor in parallel). When implementing the *complete tableau approach* within a network simulation program, there arise some difficulties:

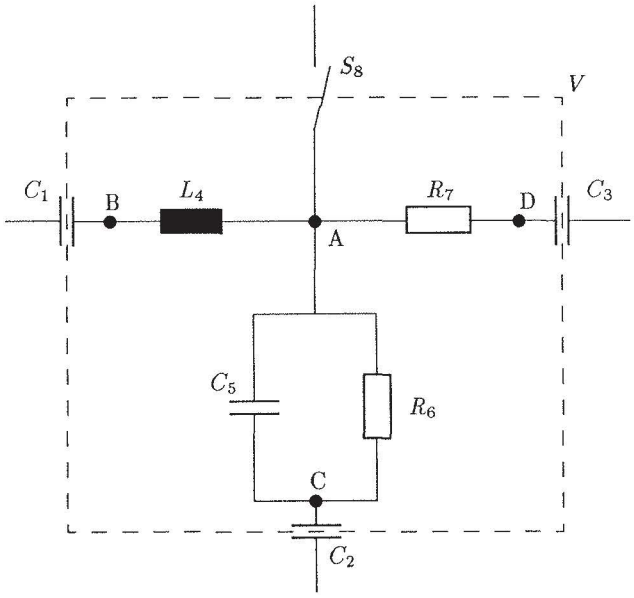

Fig. 3. Capacitive star

- We have to compute two new topology matrices which require a detailed analysis of the characteristic of each element. The program must decide if we have a capacitor. If this capacitor has a conductor in parallel we must check if the value of the conductor may become 0. If this situation may occur the topology of the network changes and we need a different matrix for the charge law.
- For a circuit simulation program with an ideal switch as one of its built-in basic elements, it is very hard to compute the topology matrices. Because the state of one or more switches can charge at each timestep, the topology matrices for the charge and flux laws must be recomputed at each timestep. Therefore, the sparsity pattern and the size of the Jacobian matrix can change each timestep.

To overcome the above difficulties we want to simplify the charge and flux laws to get a better formulation from an algorithmic point of view. First we will define some values for each oneport:

1. For each oneport which has no constitutive relation using the element charge (i.e. all elements except capacitor, memristor and memductance) we define the stored charge of the element to be zero ($q_j = 0$).
2. We introduce a new value called *artificial charge* r_j for each oneport.
3. For capacitors r_j is defined to be zero.
4. For all other oneports the value is not fixed, i.e. it is floating. The value is zero if there is no energy at all in the network (initial condition).

As a next step we modify the charge law to convert the equation in the format with the above stated requirements. This modification can be illustrated with Fig. 3.
We have a charge law for volume V which uses the charges stored in the plates of the three capacitors on the surface of volume V:

$$q_1 + q_2 + q_3 = 0 \tag{12}$$

Because of the above definitions ($r_i = 0$ for capacitors) we can modify equation (12)

$$(q_1 + r_1) + (q_2 + r_2) + (q_3 + r_3) = 0 \tag{13}$$

The open switch S_8 is equivalent to a conductivity of zero and therefore q_8 is defined to be zero. r_8 is defined to be floating starting with a zero value in the energy-less state. With inclusion of switch

S_8 equation (13) becomes (14):

$$(q_1 + r_1) + (q_2 + r_2) + (q_3 + r_3) + (q_8 + r_8) = 0 \tag{14}$$

Equation (14) can be rewritten in the form

$$\sum_{j=1}^{n} (q_j + r_j) = 0 \tag{15}$$

Equation (15) holds for each capacitor-only cutset, i.e. a cutset which consists of capacitors and open switches (or conductors with zero conductivity) only due to the charge law (8) and our above definitions. Now we want to proof that equation (15) holds for each node of our network using the network in Fig. 3. We will verify that the equation holds for node A too. For node B, C and D rule (15) results in the following additional equations:

$$(q_1 + r_1) = (q_4 + r_4) \tag{16}$$

$$(q_2 + r_2) = (q_5 + r_5) + (q_6 + r_6) \tag{17}$$

$$(q_3 + r_3) = (q_7 + r_7) \tag{18}$$

We insert these three equations into equation (14) and will get equation (19).

$$(q_4 + r_4) + (q_5 + r_5) + (q_6 + r_6) + (q_7 + r_7) + (q_8 + r_8) = 0 \tag{19}$$

Equation (19) is exactly rule (15) for node A. Therefore we have proved that equation (15) holds for every node in an electrical network. This rule is a *modified charge law* which can be written in matrix-form using the incidence matrix for the whole network:

$$A \cdot (q + r) = 0 \tag{20}$$

For the above equations we assumed that switch S_8 is open. Our volume V had no conductive path to the outside world and to possible energy sources. Now we should consider the case when switch S_8 is closed or was closed previously. Equation (12) for volume V must be rewritten as (21) with q_{tot} indicating the total charge brought into volume V.

$$q_1 + q_2 + q_3 = q_{tot} \tag{21}$$

Comparing equation (21) with (14) we get the relation

$$q_8 + r_8 = -q_{tot} \tag{22}$$

Because $q_8 = 0$ holds per definition we can simplify (22):

$$r_8 = -q_{tot} \tag{23}$$

Due to equation (23) r_8 can be interpreted as the total charge brought into volume V. To generalize we can state:

> The sum of the virtual charges of all elements located at the surface of a volume represent the total charge brought into or extracted from that volume.

Similar to the *modified charge law* we define:

1. For each oneport which has no constitutive relation using the elements flux (i.e. all elements except inductor, memristor and memductance) we define the stored flux of the element to be zero ($\phi_j = 0$).
2. We introduce a new value called *artificial flux* s_j for each oneport.
3. For inductors s_j is defined to be zero.
4. For all other oneports the value is not fixed, i.e. it is floating. The value is zero if there is no energy at all in the network (initial condition).

Now we can derive the following *modified flux law* which holds for each loop in the network:

$$\sum_{j=1}^{n} (\phi_j + s_j) = 0 \tag{24}$$

Again, we can write equation (24) in matrix form for the whole network:

$$B \cdot (\phi + s) = 0 \tag{25}$$

It is a simple task to prove that in addition to Tellegens theorem[49] for voltages and currents

$$v^T \cdot i = 0 \tag{26}$$

three new Tellegen laws hold for electrical networks.

$$v^T \cdot (q + r) = 0 \tag{27}$$

$$(\phi + s)^T \cdot i = 0$$

$$(\phi + s)^T \cdot (q + r) = 0 \tag{28}$$

After modifying the charge and flux laws we can now describe a network consisting of

b	oneports
n	nodes
k	connected subnetworks
b_i	current controlling elements
b_v	voltage controlling elements
b_q	charge controlling elements
b_ϕ	flux controlling elements
b_r	capacitors
b_s	inductors

with the following set of equations:

$b_i + b_v + b_q + b_\phi$	constitutive relations of the elements
$b_r + b_s$	additional relations for the artificial values
$n - k$	Kirchhoffs current laws
$b - n + k$	Kirchhoffs voltage laws
$n - k$	modified charge laws
$b - n + k$	modified flux laws

Note that a capacitor has three constitutive relations, one current controlling, one charge controlling and an equation for the virtual charge.

There are $6b$ unknowns in the equation system consisting of at least $3b$ equations.

The linearized equation system including magnetic coupling is shown in Fig. 4. See Appendix A for a complete example.

4. IMPLEMENTATION OF JANAP

The *Complete Tableau Approach* has been implemented in a new circuit simulation program called JANAP[17]. In the following sections some topics which are important for an efficient implementation of the CTA-method will be discussed.

4.1 Overview

The network simulation program JANAP (*Just Another Network Analysis Program*) for electrical networks follows the following general design aspects:

- Values of basic elements can be specified using arbitrary algebraic expressions. Within the expression built-in, user defined or external functions can be used. The expression can use electrical values from other branches. i.e., arbitrary controlled elements can be defined.
- An ideal switch is implemented as one of the basic elements.
- A universal element is provided as one of the basic elements.
- The input language allows the description of the electrical network in a free format language.
- There exist 38 built-in functions, including MAX, IFEQ, IFGT (choose one of two expressions depending on the value of a third expression), SQRT, EXP, LN, SIN, ASIN, SINH, ASINH, PULSE, EDGE and DT ($\frac{d}{dt}$).
- The generalized complete tableau approach is used to solve the charge conservation problem.

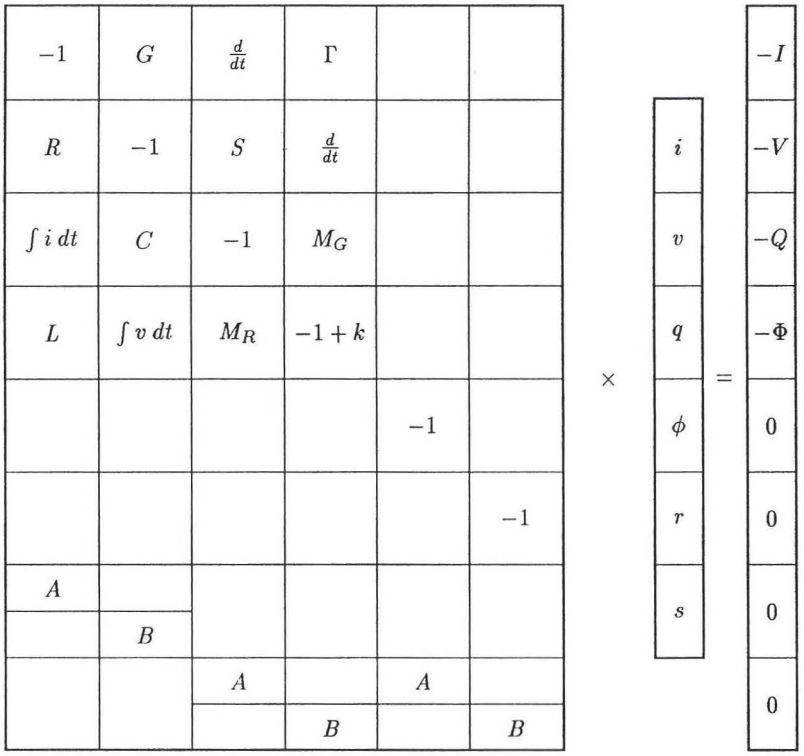

Fig. 4. Expanded CTA matrix

- To enhance the portability JANAP has been implemented using the programming language FORTRAN 77 (Refs 2 and 40).
- Before generating the equation system to describe the network, simple equations are solved symbolically.
- JANAP does not implement built-in models for semiconductor devices. JANAP provides a comfortable facility called JANLIB[54] to define and administer subcircuits within subcircuit libraries. Users can access standard models for semiconductor devices from standard subcircuit libraries.

JANAP implements the following basic elements:

- resistor, conductor
- capacitor, inductor
- current source
- voltage source
- switch
- universal element
- magnetic coupling

Each of the above elements can be nonlinear and can be controlled by an arbitrary number of values of other elements. The magnetic coupling can be asymmetric too.

JANAP implements a so called *universal element*. With this element users can explicitly define a oneport by specifying their constitutive relations. For a universal element up to relations for the electrical values i,v,q,ϕ and the artificial values r and s can be given. The expressions for the artificial values must be of the form $x = 0$ if present. Therefore, it is possible to define real oneports, such as the oneports in Table 3, as one single basic element. This allows to write compact device and macro

models and will reduce the total size of the equation system.

JANAP does not require that the network to simulate consists of only one connected network. A common ground node is not required.

JANAP implements the following simulations:

- DC operating point, DC transfer function
- transient simulation
- parameter variation including temperature

JANAP does not implement the linear small signal AC simulation, because this seems to be useless in a simulation program with extensive use of nonlinear elements and switches. In a future version JANAP will provide the nonlinear steady-state simulation.

4.2 Generation and solution of the equation system

As mentioned above JANAP uses the generalized complete tableau approach for the formulation of the equation system to describe the network. This formulation technique results in a relatively large equation system. As can be seen from Table 2 most of the constitutive relations of the built-in elements are of the form $x = 0$. All this equations can be solved *a priori* by inspection of the equations during the setup phase. This reduces the size of the equation system dramatically. Most of the relations which have been added to the equation system to solve the charge conversation problem and to have a clean network formulation are eliminated during this reduction process. Only the relations which are really needed to solve the charge conservation problem remain in the equation system.

Due to the formulation of the network equations the rank of the equation system is not equal to the number of unknowns in the equation system. This situation has the following reasons:

- Due to the implementation of an ideal switch it is possible that the topology of the network (the number fo subnetworks) changes during the simulation. When the number of connected subnetwork increases the equation system will contain redundant equations.
- The modified complete tableau approach adds the artificial variables r and s to the network equations. The value of the artificial variables cannot be uniquely computed in all cases without an initial value assumption. If we look at a simple circuit consisting of a voltage source and a resistor in parallel, there is no constitutive relation for r. r appears only in the topology equations. Therefore, it is not possible to specify a concrete value of r. This situation does not effect the solvability of the network equations in general because nobody wants to know the values of r in this case. It is important that the vector r and s is present to *transport* the information about the changes of stored charge or flux from one part of the network to all other parts. The concrete value has no relevance. Due to the initial conditions, which are zero for r and s, there will be a concrete value for r and s in practice.

The solver for the equation system must be able to handle these special conditions. JANAP uses a code based on the sparse matrix solver MA28 (Ref. 19) MA28 makes the matrix square by bordering it with a zero matrix. Then it transforms the matrix to a block triangular form[18,22,23]. The Jacobian matrix of the equation system usually has zeros in the main diagonal. Therefore the matrix has to be permuted[20] applying stability criterions[24, 43]. The reordering and block triangularization must only be performed when the sparsity pattern changes due to a topology change of the network, or when major changes in the values of the Jacobian matrix occur due to the nonlinearities in the network.

After reducing the network equation system by symbolic methods, the Jacobian matrix is computed symbolically as far as possible. The entries of the Jacobian can be classified by one of the following attributes:

constant 0: Most of the entries in the Jacobian are constant zero. Typically only three entries within one row of the Jacobian are nonzero.

constant: Most of the remaining entries in the Jacobian have a constant value. All entries resulting from the topology equations generate either + 1 or − 1. For all elements, which do not depend on another branch or depend on time, we will get a constant entry for the Jacobian too.

Fig. 5. Diode model in JANAP

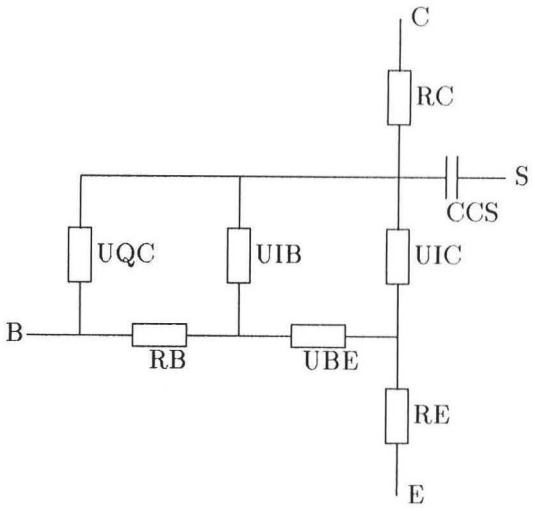

Fig. 6. Bipolar Transistor Model in JANAP

equation: Almost all the remaining entries in the Jacobian can be computed symbolically. $\partial f_i(x)/dx_j$ will be computed by symbolic methods during the setup phase.

numeric: For some networks there will remain few entries of the Jacobian, which can only be computed using numeric differentiation. Typical examples include networks which require external functions to describe some of the elements. For circuits containing the basic elements, including switches, and BJT or FET devices modeled according to the well known device models, no entry of the Jacobian has to be computed by numeric differentiation.

Numerical differentiation is usually not required. Therefore, the Jacobian matrix can be computed with high accuracy. During latent time periods of the network the evaluation of the Jacobian will by bypassed to reduce computation time. The equation system for a specific time step or for the DC operating point is solved using an adaptively damped Newton schema[4]. The Jacobian matrix is a very sparse matrix with typically three entries for each row. For processing of the Jacobian, sparse matrix methods are heavily used[21].

The transient simulation is accomplished by fully implicit backward difference formulae with automatic time step and order control[6,44,27,28,29,31,34]. Due to the availability of ideal switches and built-in functions with discontinuities, the algorithms for the computation of the transient solution of a network must handle discontinuities properly[30].

In contrast to most of the available circuit simulation programs JANAP has no built-in models for semiconductor devices. Therefore, it is not possible to handle overshooting and similar effects which occur during the solution of highly nonlinear systems of equations in a customized fashion. Overshooting has to be processed by a general damping method and range checks throughout the whole solution phase.

4.3 Modeling in JANAP

In contrast to most of the existing circuit simulation programs[47,14,25,56,57], JANAP has no built-in models for semiconductor devices. The models have to be provided as subcircuits which may be

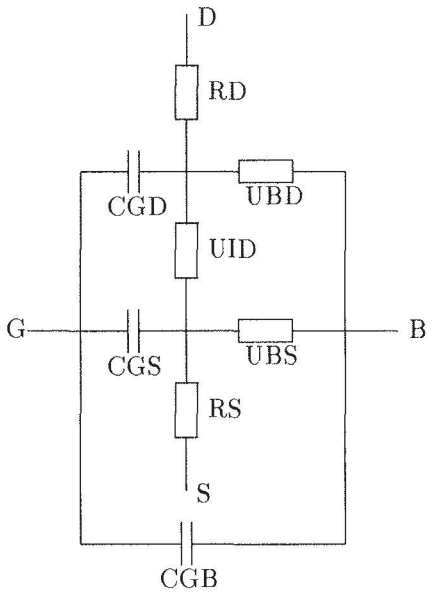

Fig. 7. Example of a MOS Transistor Model in JANAP

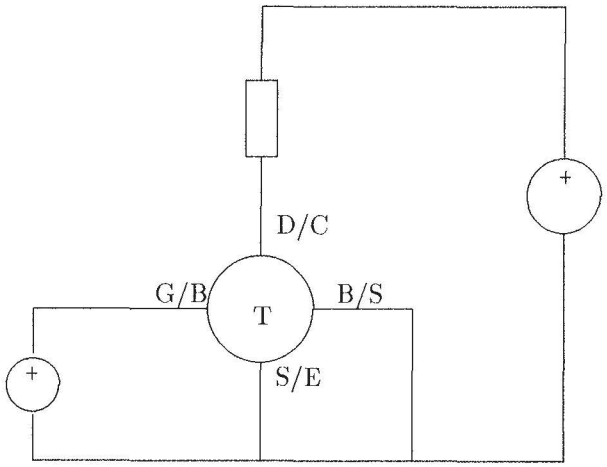

Fig. 8. Test circuit for transistor models

Table 4. Comparison of transistor models

Model	Figure	Elements		Number of Equations	Jacobian Nonzeroes		Number of Unknowns
		SPICE2	JANAP		const.	symb.	
BJT	6	13	8	34	81	10	42
MOS	7	10	8	36	81	22	42

available in standard subcircuit libraries. The pros and cons of this method are:

```
subckt  D  PLUS-MINUS = IS,RS,N,TT,CJO,VJ,M,FC,BV,IBV,EG,XTI,A
*       default values of parameters
param M=.5, VJ=1, N=1, IS=1E-14, FC=.5, IBV=1E-3, BV=0, RS=0, TT=0, CJO=0
param EG=1.11, XTI=3, KB=1.3806226E-23, ECH=1.6021918E-19

function VT(0) = KB/ECH*temp

RS  PLUS-1    =  RS/A
UD  1-MINUS   =  I= IS*A*(exp(V(UD)/N/VT(0))-1)
                   - ifgt(BV,0,ifgt(BV-V(UD),0,IBV*exp((V(UD)-BV)/VT(0)) ))
                   + dt(Q(UD))  ,
                 Q=V(UD)*( TT/VT(0)*( IS/N*exp(V(UD)/N/VT(0))
                           -ifeq(BV,0,ifgt(BV-V(UD),0,
                                IBV*exp((V(UD)-BV)/VT(0)) )) )
                         + CJO*A*ifgt(V(UD)-FC*VJ,
                                1-M/VJ*(V(UD)-FC*VJ)/(1-FC)))/(1-FC)**M,
                                1/max(1-FC,1-V(UD)/VJ)**M )) ,
                 P=0
ends
```

Fig. 9. JANAP input for diode model

- Built-in models can be realized in a more efficient way.
- For built-in models the nonlinear behavior of the device is well known. This information can be used during the solution process for the damping method.
- If someone wants to change the built-in model because additional affects should be included in a model, this must be done by changing the simulation program itself. This may be a very complicated task and requires knowledge about the internal structure of the simulation program.
- If someone wants to implement the model of a new device this may require changing the simulation program too, because most of the simulation programs do not provide the required functions to describe the model.

JANAP provides the following features to allow an easy implementation of device models:

- nonlinear functions required to describe a model (e.g. e^x, $\sqrt{x}$)

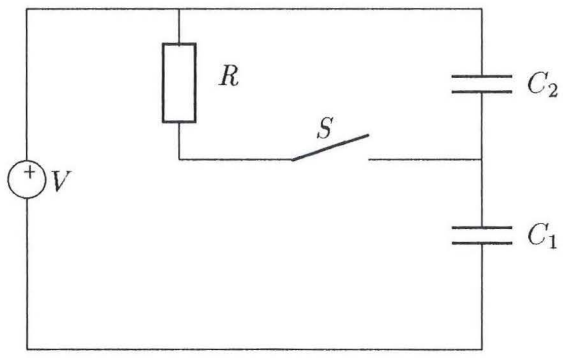

Fig. 10. Simple Demonstration circuit

```
TITLE 'VSRCC - RCC with periodic switch.'
V  3-GND =  1
R  3-2   =  1Ohm
S  2-1   =  PTIME(0,1)-.5
C2 3-1   =  1Farad
C1 1-GND =  1Farad
DC
TRAN 0,5,1E-3,0.2, pstep=points 300
PRINT table 'Time' time, 'V(C1)' v(c1), 'V(C2)' v(c2), 'Switch' v(s)
PLOT  'Time' time
      scale common 'V(C1)' v(c1), 'V(C2)' v(c2)
END
```

Fig. 11. JANAP input of demonstration circuit

- possibility to specify different formulas for different operating regions of the device (functions IFEQ, IFGT, MIN, MAX, ABS)
- compact description using the universal element
- The behavior of a device can be described using one or two-dimensional tables.

$$
\begin{aligned}
-i_{C1} + \frac{dq_{C1}}{dt} &= 0 \\
-i_{C2} + \frac{dq_{C2}}{dt} &= 0 \\
-i_S + switcho(i_S, p) &= 0 \\
Ri_R - v_R &= 0 \\
-v_S + switchc(v_S, p) &= 0 \\
C_1 v_{C1} - q_{C1} &= 0 \\
C_2 v_{C2} - q_{C2} &= 0 \\
-i_V - i_R - i_{C2} &= 0 \\
i_R - i_S &= 0 \\
-i_{C1} + i_{C2} + i_S &= 0 \\
v_{C1} + v_{C2} &= V \\
-v_R + v_{C2} - v_S &= 0 \\
-q_{C2} - r_V - r_R &= 0 \\
r_R - r_S &= 0 \\
-q_{C1} + q_{C2} + r_S &= 0 \\
-s_V + s_{C1} + s_{C2} &= 0 \\
-s_R + s_{C2} - s_S &= 0
\end{aligned}
$$

Fig. 12. The reduced equation system

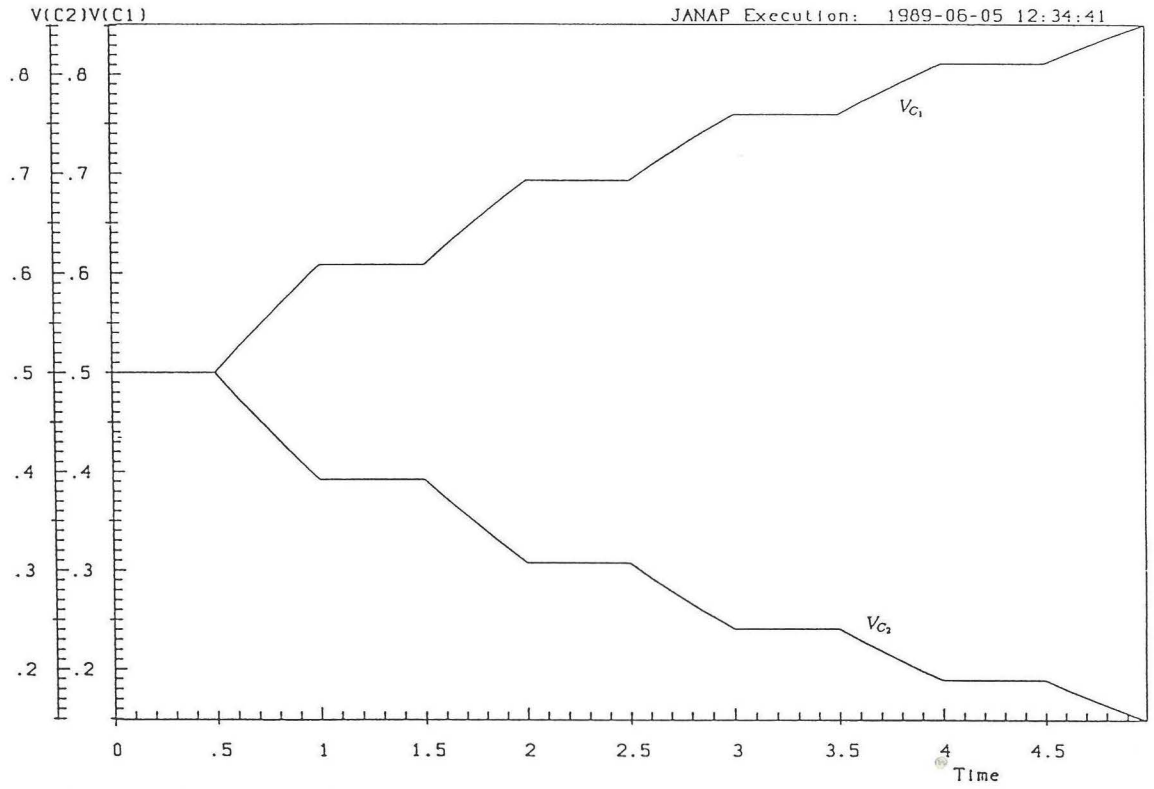

Fig. 13. Simulation result for the demonstration circuit

- For each subcircuit formal parameters can be specified, which may be used to specify the model parameters.
- Subcircuits can be grouped in subcircuit libraries, which can be made available to the user of the simulation program.
- Using the ideal switch it is possible to define models of different accuracy for digital circuits. It is possible to implement logic, timing and full models of a semiconductor device. Therefore, it is possible to apply the ideas of the *hybrid* simulation[15,16] and macro modeling[33,5,3,39] in JANAP.
- JANAP allows the usage of external (FORTRAN) functions. This allows to define the complex behavior of devices which cannot be described in the JANAP input language. As an extreme example, it is possible to call a device simulator such as MINIMOS[52,36,53] via an external function call.

The standard models for semiconductor devices[32,50,57,44,46,51,45] have been implemented in JANAP input language[42,54]. All the models of SPICE2[57] are realized in JANAP input language[42]. The models for a diode, a bipolar transistor and for MOS transistors are shown in Figs 5, 6 and 7. As you can see, the number of elements to characterize a device is less than the number in models of conventional circuit simulation programs due to the heavy usage of the universal element.

To compare the models for BJT and MOS transistors in JANAP with the built-in models of SPICE2, the test circuit 8 will be used. The result is summarized in Table 4.

The description of the temperature independent model for a diode realized in JANAP input language which is compatible with the corresponding SPICE2 built-in model is shown in Fig. 9[42].

5. CONCLUSION

The *complete tableau approach* to formulate the network equations for nonlinear circuits using semiconductor devices and switches has been presented. It has been shown how the complete tableau

approach solves the charge conservation problem for capacitor-only cutsets and inductor-only loops in an efficient and computational oriented way. A circuit simulation program which implements the complete tableau approach has been described. The new possibilities which are offered with the ideal switch and the universal element in JANAP applied to device modeling are described. To exploit all the possibilities offered by the universal element additional studies can be imagined.

APPENDIX A

Figure 10 shows a very simple circuit with 5 oneports which requires the solution of the charge conservation problem. The actual input for JANAP is shown in Fig. 11. The full equation system consists of 29 equations. Of the 30 unknowns of the network 12 unknowns can be computed *a priori* due to the trivial defining equations $x = constant$. The reduced equation system (Fig. 12) consists of 17 equations.The values of 4 unknowns (the virtual fluxes of the passive elements) cannot be computed without an assumption for the initial value due to the rank-defect of the equation system. In the equation system the *switch*-functions are defined as follows:

$$switcho(i, p) = \begin{cases} i & \text{switch closed} \\ 0 & \text{switch open} \end{cases}$$

$$switchc(v, p) = \begin{cases} 0 & \text{switch closed} \\ v & \text{switch open} \end{cases}$$

The results provided by JANAP are shown in Fig. 13.

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