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The Application of Charge-Pumping Technique to Characterize the Si/SiO_2 Interface in Power VDMOSFETs

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The possibility to perform charge-pumping measurements on power VDMOS transistors is investigated. By analyzing the spatial distributions of the charge-pumping threshold and flat-band voltages it is concluded that the charge-pumping measurements can be carried out in the subthreshold region of the device. This conclusion is confirmed by two-dimensional transient numerical modeling of the charge-pumping effect and supported by experiments. The method for a separate extraction of interface state and fixed charge densities generated by irradiation in the oxide of VDMOSFETs is proposed.

1. INTRODUCTION

Power Vertical Double-diffused (VD)MOSFETs have found an important application in very high-frequency switching power supplies due to their fast switching capabilities. Thanks to a high power/volume ratio, these power supplies are suited for the aerospace satellites. In these applications power VDMOSFETs are exposed to a high space radiation, which strongly reduces their lifetime due to the generation of fixed oxide charge ΔN_{ox} and interface states ΔN_{it} [1]. In order to extract separately ΔN_{ox} and ΔN_{it} induced by irradiation in MOSFETs (both assumed as spatially uniform), methods based on the threshold voltage shift and either the subthreshold-slope change [2], the mobility degradation (the MOSFET gain factor [3,4] or the transconductance [5] change) or the mid-gap voltage shift [6] have been proposed. These routinely used techniques are indirect and involve some restrictive assumptions. The charge pumping has been proven, however, to be an accurate and very sensitive technique to characterize N_{it} in various devices in *a direct manner* [7,8].

The purpose of this work is to investigate the possibility to apply charge-pumping measurements on power VDMOS transistors – directly on the standard structures. It is demonstrated by numerical modeling and confirmed by experiments that the charge-pumping measurements can be performed on power VDMOSFETs. Moreover, they enable a direct and separate extraction of densities of interface traps and fixed charges induced by irradiation in these transistors.

2. CHARGE PUMPING IN VDMOSFETS

As opposed to conventional silicon bulk MOSFETs, there is no a separate bulk contact which can supply majority carriers in VDMOS structure (Fig.1). The same problem occurs when applying charge-pumping (CP) measurements on SOI devices. In (n-channel) VDMOSFETs, however, the p^--region which represents the bulk is shortly connected over the p^+-region with the source contact. The source contact can, therefore, play a role of the bulk contact unless the n^+-source region is inactive. These conditions are fulfilled in CP measurements if the channel region is always biased under the threshold voltage U_{th} during the excursion of the gate bias. A crucial fact is that the electron charge-pumping threshold voltage of the epitaxial (epi) region U_{th}^{cp}-epi, which is deter-

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mined by the n^- surface concentration, is lower than the channel threshold voltage U_{th} which depends on the p^--concentration at the source channel-end. Moreover, the hole charge-pumping flat-band potential of the epi-region V_{fb}^{cp}-epi lies under the flat-band potential of the p^- area. Thereby, interface states along the complete SiO_2/epi interface and in part in the channel region (SiO_2/p^-) as well, can be filled by electrons supplied by the n^+ drain over the n^--epi layer at the gate-pulse top level U_{GH}, even the device is biased in the subthreshold region ($U_{GH} < U_{th}$). Interface states are filled by holes provided by the source contact over the p^+ and p^- areas at the gate-pulse bottom level U_{GL}. In these conditions, n-channel VDMOSFETs behave as conventional p-channel MOSFETs and various CP measurements can be carried out on these structures.

3. NUMERICAL MODELING

The present concept is confirmed by modeling and experiments on low-voltage ($100V$) and high-voltage ($500V$) power VDMOSFETs fabricated by standard Si (polysilicon gate) processes. The low-voltage devices consist of about 860 hexagonal cells of $33\mu m$ size arranged in a hexagonal mesh. The cross section of two half-cells considered in modeling is shown in Fig.1, with all geometry-data specifications assumed according to the process description [9]. The applied doping profile is simulated by employing MUSIC 2 [10], an adaptive multigrid 2D process simulator, using the detailed process flow description as input [9]. Steady-state and transient (charge-pumping) device characteristics are numerically calculated by employing MINIMOS 6 which has been extended to account for VDMOS structure [9]. The model of the charge-pumping effect is the rigorous numerical approach described in [8,11].

Fig.2 shows the edges of the interface area for the total electron and hole capture, which are calculated by steady-state MINIMOS 6 simulation. These edges represent the local CP threshold voltage U_{th}^{cp} and CP flat-band potential V_{fb}^{cp}, which are defined by the critical concentrations $n_s^{crit.} = 1/(v_{thn}\sigma_n t_H/3)$ and $p_s^{crit.} = 1/(v_{thp}\sigma_p t_L/3)$ dependent on the top and bottom level durations t_H and t_L, respectively. Different characteristic positions of the gate pulses with respect to U_{th}^{cp} and V_{fb}^{cp} are denoted on Fig2:

A) $U_{GH} < U_{th}^{cp}$-epi. Very small region close to the n^+/p junction is active in charge pumping. The terminal d.c. current vanishes because both the recombined electrons and holes are supplied by the source contact.

B) $U_{GH} \geq U_{th}^{cp}$-epi, $U_{GL} \leq V_{fb}^{cp}$-epi; these conditions represent the charge-pumping active region. The d.c. drain electron current I_{De} is equal to the net electron and hole recombination rate $G_{\mathrm{eff}n,p}$ at the complete SiO_2/epi interface and in a part of the channel-interface. The I_{De} also equals to the d.c. source hole current $-I_{Sh}$. The d.c. source electron current I_{Se} is small, but it rapidly increases when U_{GH} approaches U_{th}, while the d.c. drain hole current I_{Dh} is negligible. The measured d.c. drain current $I_{cp} = I_D \approx I_{De}$ is negative in n-channel VDMOSFETs.

C) $U_{GH} \geq U_{th}^{cp}$-epi; $U_{GL} > V_{fb}^{cp}$-epi. A part of the channel-interface is active in charge pumping; the SiO_2/epi interface is inactive because of an insufficient hole capture.

D) $U_{GH} \geq U_{th}$. Independent of the pulse amplitude ΔU_G, when the top level exceeds the channel threshold voltage the n^+-source region becomes active. In this, for the CP measurements unattractive region, we observed a d.c. transfer of electrons from the source towards the drain in numerical simulations. The component I_{Se} increases and the drain current becomes $I_D = -(I_{Sh} + I_{Se})$. The I_{Sh} is solely due to the interface recombination. The current I_D changes the sign because the negative I_{Se} dominates over the positive I_{Sh} (n-channel devices).

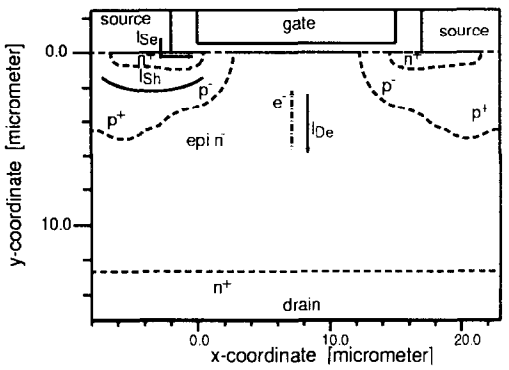

Fig.1 Analyzed low-voltage power VDMOSFET with parameters: $t_{ox} = 100nm$, $L_G = 15\mu m$. The doping profile resulting from 2D multigrid process simulation is used. The arrows show the d.c. components of the source electron I_{Se}, the source hole I_{Sh} and the drain electron I_{De} currents.

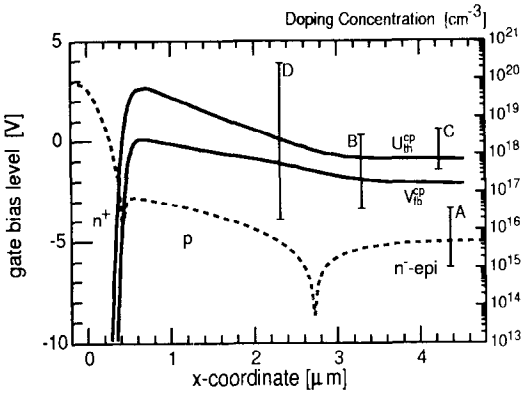

Fig.2 The position of the electron (U_{th}^{cp}) and hole (V_{fb}^{cp}) total-capture edges in a half of the VDMOSFET cell. Some characteristic positions of the gate-pulse top and bottom levels are denoted. The impurity profile along the interface is shown.

In the CP active region, the $|I_{cp}|$ increases with increasing U_{GH} and becomes maximal at $U_{GL} = V_{fb}^{cp}$-epi. After that point it decreases due to effect C). However, the decrease of $|I_{cp}|$ can only be observed if the conditions D) do not take place, *i.e.* if $U_{GH} = \Delta U_G + V_{fb}^{cp}$-epi $< U_{th}$, which is fulfilled for small amplitudes ΔU_G.

4. MEASUREMENTS AND APPLICATION

All discussed effects are fully confirmed by numerical results (Fig.3) and completely supported by experimental data for low-voltage (Fig.4) and high-voltage devices. The agreement between experimental and simulated results is very good in the CP active region. However, a significant disagreement is found in the parasitic $U_{GH} > U_{th}$ region, which origin is not clear.
In Fig.5 we focus on the CP active region $U_{GH} < U_{th}$ of a low-voltage device. The expected dependence of I_{cp} on the rise and fall times (t_r, t_f) and ΔU_G due to the variation in the electron and hole emission times is clearly found in experiments. Note that the numerically calculated I_{cp} cannot be directly compared against the measured I_{cp} because the considered hexagonal VDMOS structures are typical 3D-devices in which the effective device width varies along the x-coordinate (Fig.1).

The modeling results in Fig.6 demonstrate the potentials of the CP measurements to extract the amount of the charge trapped in the oxide and of the interface states generated by irradiation along the active part of the interface in power VDMOSFETs. The ΔN_{it} and ΔN_{ox} assumed in this calculation are the values measured on the considered power devices after $50krad$ radiation dose with zero gate bias [4] ([2]).

REFERENCES

1. T.P.Ma and P.V.Dressendorfer, Ionizing radiation effects in MOS devices and circuits, Wiley & Sons (1989).
2. T.Sakai and T.Yachi, IEEE Trans.Electr.Dev. 38, 1510 (1991).
3. S.Dimitrijev and N.Stojadinović, Solid-State Electr. 30, 991 (1987).
4. N.Stojadinović, S.Golubović, S.Djorić and S.Dimitrijev, Microel.Rel. 35, 587 (1995).
5. K.F.Galloway, M.Gaitan and T.J.Russel, IEEE Trans.Nucl.Scien. NS-31, 1497 (1984).
6. P.J.McWhorter and P.S.Winokur, Appl.Phys.Lett. 48(2), 133 (1986).
7. G.Groeseneken *et al.*, IEEE Trans.Electr.Dev. 31, 42 (1984).
8. P.Habaš, Analysis of physical effects in small silicon MOS devices, TU Vienna (1993).
9. P.Habaš, D.Pantić, Z.Prijić and N.Stojadinović, Proc.CAS, 501, Sinaia (1994).
10. S.Mijalković, D.Pantić, Z.Prijić and N.Stojadinović, Proc.SISDEP, 505, Zürich (1991).
11. P.Habaš,O.Heinreichsberger and S.Selberherr, Proc.ESSDERC, 687, Leuven (1992).

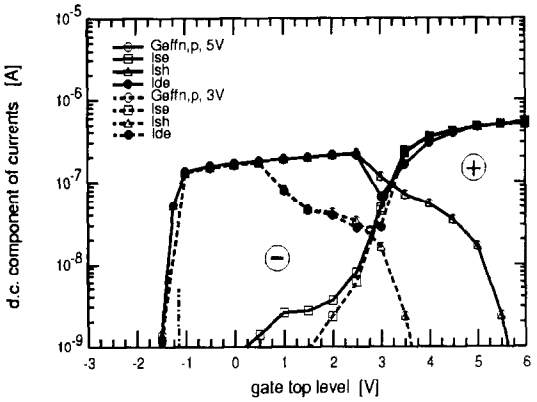

Fig.3 Charge-pumping characteristics of VDMOSFET calculated by 2D transient numerical model for pulse amplitudes ΔU_G $3V$ and $5V$ ($t_f = t_r = 1\mu s$, $f = 100kHz$, 50% duty cycle). Uniform interface traps assumed: $D_{it} = 6 \times 10^9 cm^{-2} eV^{-1}$, $\sigma_n = 10\sigma_p = 3 \times 10^{-15} cm^2$. The positive and negative regions of I_{De} are denoted. The dotted-dashed line depicts the calculated U_{th}^{cp} in the epi-region (Fig.2) – the rising edge of the $I_{cp}(U_{GH})$. The I_{cp} starts to decrease at $V_{fb}^{cp} + \Delta U_G$ in the epi-region.

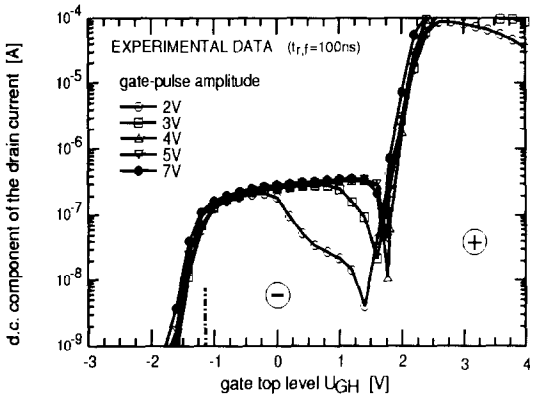

Fig.4 Experimental characteristics of a VDMOSFET at different amplitudes ($f = 100$ kHz, 50% duty cycle). The calculated U_{th}^{cp} in the epi-layer is denoted. The plateau of the CP active region ranges from U_{th}^{cp}-epi to V_{fb}^{cp}-epi$+\Delta U_G$. When plotting the curves with respect to the U_{GH}, the characteristics match each other at the rising edge of the CP active region and in the region where the measured d.c. drain current changes in sign (when approaching the device threshold voltage).

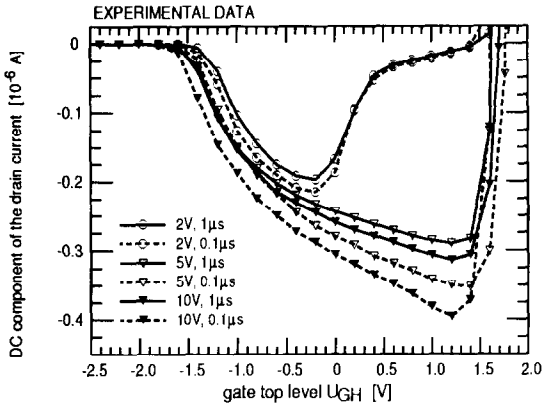

Fig.5 Experimental curves in the CP active region for different pulse amplitudes and rise/fall times. The characteristics nicely reflect the dependence of I_{cp} on the ratio $t_{r,f}/\Delta U_G$ due to emission time variations. The shape of the curves is modulated by the characteristics shown in Fig.2 and by the change in the effective device width due to the 3D-geometry of the analyzed hexagonal VDMOSFETs.

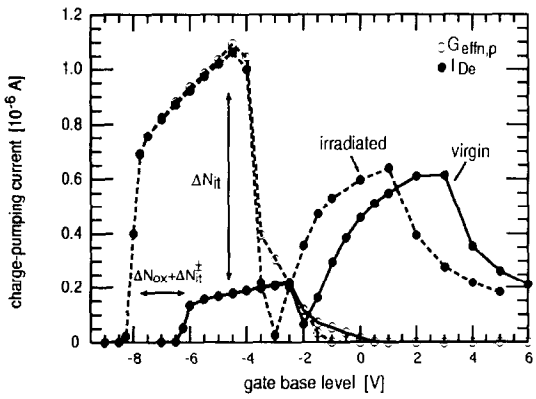

Fig.6 Simulated impact of an uniform increase in interface state density and fixed oxide charge. Gate pulses: $\Delta U_G = 5V$, $t_r = t_f = 1\mu s$. Before stress: $D_{it} = 6 \times 10^9 cm^{-2} eV^{-1}$. After stress: $D_{it} = 3 \times 10^{10} cm^{-2} eV^{-1}$ (acceptor like), $\Delta N_{ox} = 4 \times 10^{11} cm^{-2}$. The increase of I_{cp} is exclusively due to ΔN_{it}, while the voltage-axis shift is mostly due to ΔN_{ox}.