Compact Modeling of Memristive IMP Gates for Reliable Stateful Logic Design

Hiwa Mahmoudi, Thomas Windbacher, Viktor Sverdlov, and Siegfried Selberherr
Institute for Microelectronics, TU Wien, Gußhausstraße 27–29/E360, A–1040 Wien, Austria
E-mail: {mahmoudi|windbacher|sverdlov|selberherr}@iue.tuwien.ac.at

***Abstract*—Introducing non-volatility into CMOS circuits is a promising solution to overcome the standby power dissipation due to leakage, which has become a major challenge of today's VLSI. Stateful logic inherently realizes non-volatile logic-in-memory circuits with zero-standby power and opens the door for a shift away from the Von Neumann architecture. To ensure a correct logic behavior in all input patterns, the reliability of the conditional switching in the stateful logic gates is the most important design objective. In this work the goal is to efficiently calculate the reliabilities in TiO_2-based and spintronic stateful implication (IMP) logic gates with the aid of compact but sufficiently accurate device models. It is demonstrated that in order to avoid a state computation error in the TiO_2-based IMP gate, refreshing is required after a limited number of logic steps as the state drift errors accumulate. Due to the magnetic bistability of the magnetic tunnel junctions (MTJ), spin-transfer torque (STT)-MTJ-based IMP logic gates eliminate error accumulation and thus are inherently suited for digital computing. A modified SPICE model is presented to optimize the circuit parameters of the STT-MTJ-based gates for providing a reliable conditional switching behavior.**

***Index Terms*—magnetic tunnel junction (MTJ), material implication (IMP), memristor, spin-transfer torque (STT), stateful logic, state drift error**

I. Introduction

Recently, it has been shown that a fundamental Boolean logic operation called material implication (Fig. 1a) is naturally realized using titanium dioxide (TiO_2) memristive switches and enables stateful logic by using the memristive devices simultaneously as latches and logic gates [1]. Stateful logic inherently provides a non-volatile logic-in-memory architecture with zero-standby power and is free from the leakage power issue. It also allows to shorten the interconnection delay by eliminating the need for intermediate sense amplifiers as well as the data transfer between separate memory and logic units and, by that, to lift a prerequisite of the Von Neumann computing architecture. Because of unlimited endurance and CMOS compatibility, the spin-transfer torque magnetic tunnel junction (STT-MTJ) has been proposed as a very favorable device for stateful IMP logic [2]. It has been shown that the easy integration of MTJs on top of a CMOS circuit allows for generalization of the MTJ logic gates to large-scale non-volatile circuits [3]. In addition, unlike the TiO_2-based gate (Fig. 1b), due to the magnetic bistability the STT-MTJ-based stateful logic gates (Fig. 1c and Fig. 1d) do not show any state drift error accumulation. As a result, the need for refreshing circuits in stateful logic circuits is eliminated.

In the voltage-controlled IMP logic gates (Fig. 1b and Fig. 1c), the IMP logic operation is performed by simultaneous application of two negative voltage pulses, V_{SET} and V_{COND}, to the non-common terminals of the memory elements S and T. In the current-controlled topology (Fig. 1d), it is performed by applying the current pulse I_{IMP}. In both topologies proper voltage or current signals provide a conditional switching which depends on the initial resistance states of the source (S) and target (T) memory elements. In fact, only when both S and T are initially in the high-resistance state (State 1 shown in Fig. 1a), T is switched to the low-resistance state. In the other cases, S and T are left unchanged. According to the IMP truth table (Fig. 1a), this conditional switching behavior is equivalent to the IMP operation for which the initial resistance (logic) states of S and T act as the logic inputs and the final resistance state of T is the logic output.

It is obvious that a reliable logic behavior of a stateful operation is ensured only, when the logic gate exhibits correct functionality for all input patterns. Therefore, the reliability of the conditional switching behavior in all input patterns is the most important stateful logic design objective. In the following it is explained, how the existing device models are modified and exploited to optimize the stateful logic gates.

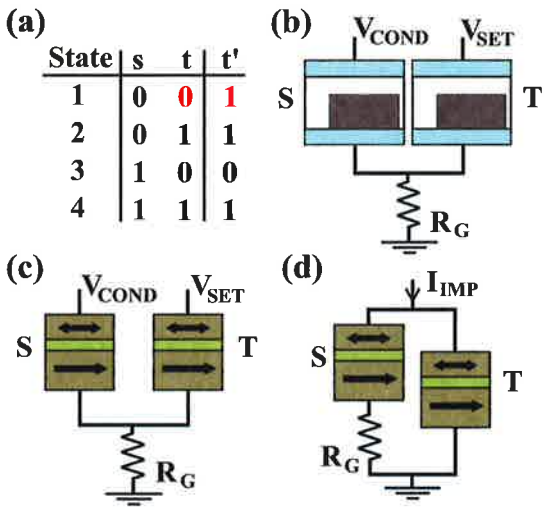

Fig. 1. (a) Material implication (IMP) truth table. (b) TiO_2-based and (c) STT-MTJ-based voltage-control stateful IMP gates. (d) STT-MTJ-based current-control stateful IMP gate.

II. TiO_2-Based Memristive Stateful Logic Gate

In the high voltage regimes required for high-speed computing, an electron tunneling significantly affects the electrical and switching behavior of the of TiO_2 memristive devices [4]. Therefore, most of the available memristor models including the compact models presented in [5], [6] as well as the SPICE models [7], [8], which rely on a linear ionic drift model [9] for TiO_2 memristive devices, are not adequately accurate for reliable stateful logic design. To the authors' best knowledge, the nonlinear ionic drift model described in [4] with its SPICE implementation presented in [10] (Fig. 3b) is up to now the most accurate model for the TiO_2 memristive devices. The voltage across the current source i is determined based on the Simmons tunnel barrier model [11] to take the electron tunneling effect through the undoped TiO_2 region with the width of w shown in Fig. 3a into account. The modulation of w is given by the modulation of the voltage across the capacitor (V_C) shown in Fig. 3b.

In order to simulate the conditional switching behavior of the TiO_2-based IMP gate shown in Fig. 1b, the model described in Fig. 3b is employed. Fig. 2 shows the modulation of the tunnel barrier widths w_S and w_T corresponding to the capacitor voltage V_C for S and T, respectively, during the implication operation for all four possible input patterns (State 1–State 4). It illustrates that for pulse durations between 1–10ms, only in State 1, the target memristor (T) is switched and in all other cases both S and T are left unchanged. Accordingly, correct logic behavior is achieved for all input

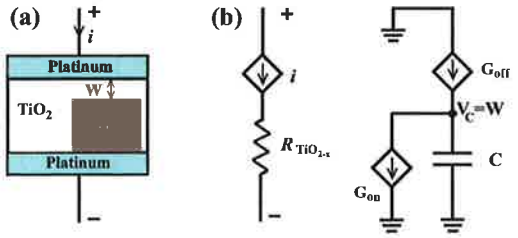

Fig. 3. (a) Schematic of the TiO_2 memristive device cross section [4]. (b) SPICE model of the TiO_2 memristive device [10].

states and the logic result is stored as the final resistance state of T. Here, the initial tunnel barriers are $w_{off} = 1.86$nm and $w_{on} = 1.43$nm which correspond to the high- and low-resistance states of the memristive devices.

Although the digital data is stored in the high- and low-resistance state of the TiO_2 memristive device, the internal state variable w shows analog behavior (Fig. 2). Therefore, during the logic operations the voltage drops on S and T tend to push w toward w_{on}, also when their switching is undesired. By using the method presented in [12], the circuit parameters are optimized to minimize the state drift errors (SDEs) and are obtained as $R_G = 4.41$kΩ, $V_{SET} = -2.28$V, and $V_{COND} = -2.14$V. According to Fig. 2, the dominant SDs occur in State 1 (Fig. 2a) in T (SD_{T1}) and in State 3 (Fig. 2c) in T (SD_{T3}). It is important to note that in the SPICE model shown in Fig. 3b, the SDEs are obtained by using V_C of S and T given by $SD = V_C - V_{C_{on}}$ for a desired switching

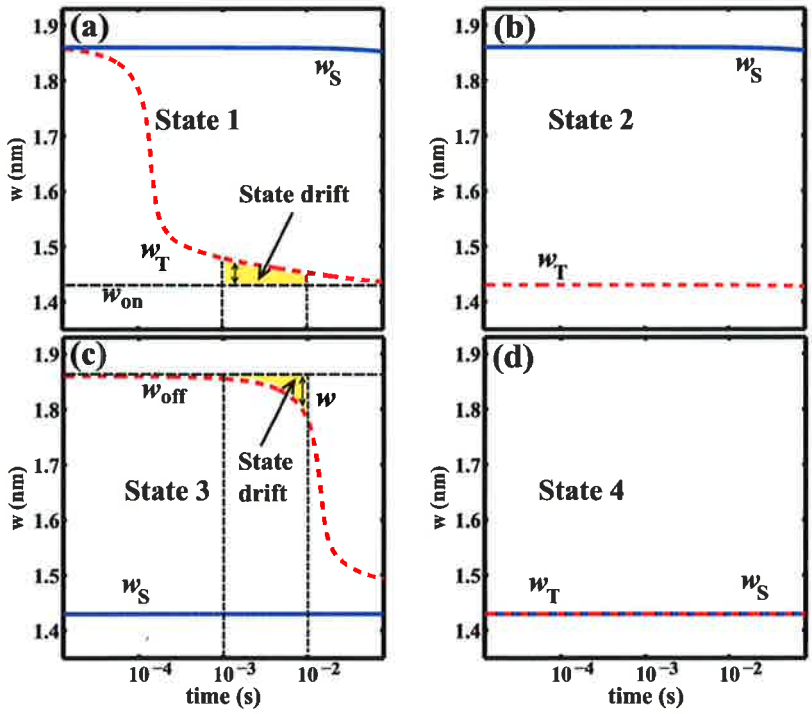

Fig. 2. Modulation of w_S and w_T during the logic operation for different input patterns.

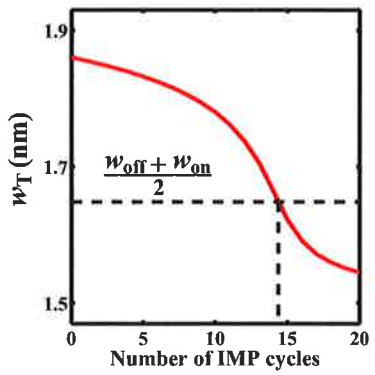

Fig. 4. Cumulative state drift effect in T for State 3.

event or $SD_{T3} = V_{C_{off}} - V_C$ for an undesired switching event. $V_{C_{on}}$ and $V_{C_{off}}$ are equivalent to w_{on} and w_{off} for the low-resistance (Logic 1) and the high-resistance (Logic 0) states.

As the SDE accumulation in sequential logic steps can result in a one-bit error after a certain number of implication operations, a refreshing circuitry is required to avoid this error [13]. Fig. 4 shows the cumulative SD in T during 20 implication operations with 1ms pulse duration when T and S are in high- and low-resistance states, respectively (State 3). It illustrates that after 14 steps the state variable w is equal to the average value of $(w_{off} + w_{on})/2 \simeq 1.65$ nm which can be readout either as high- or low-resistance state. Whereas any resistance switching in State 3 is considered as an undesired switching, the initial logic state of T has to be rewritten before w reaches 1.65 nm. It is worth mentioning that the linear model predicts a state drift of 48.9% [13] which means that refreshing is required after each implication operation. Compared to the nonlinear ionic drift model, the linear drift model exhibits higher state drift values, because it assumes that the state drift is directly proportional to the current or voltage of the memristive devices. However, according to experimental data, the ionic drift velocity shows an exponential dependence on the applied current or voltage [14], which is taken into account in the nonlinear model. One has to emphasize that, as high switching voltages are used for (high-speed) computing, the nonlinear model has to be used to take the tunneling effect and dynamical memristor behavior into account.

III. Spintronic Stateful Logic Gates

The spin-transfer torque (STT)-operated MTJ combines the advantages of scalability, CMOS compatibility, non-volatility, high switching speed, high integration density, and unlimited endurance. Furthermore, due to the magnetic bistability of the MTJ caused by an intrinsic damping in its magnetic free layer, the magnetization of the free layer can relax to its initial state, when there is enough time (in the range of sub-nanosecond) between sequential logic operations. Therefore, unlike the TiO_2-based gates, where the state drift errors are accumulated, there is no need for a refreshing circuitry in the STT-MTJ-based stateful logic systems. This makes STT-MTJs very favorable devices for stateful implication logic [2].

A. Reliability Analysis

The reliability modeling and analysis of the STT-MTJ-based stateful logic gates is an essential prerequisite for designing, optimizing, and comparing different MTJ logic circuits. The reliability of the conditional switching behavior in the STT-MTJ-based logic gates is defined as a function of the switching probabilities (P_{sw}) of desired switching events as well as $1 - P_{sw}$ for undesired switching events [15] and has to be calculated for comparing stateful logic designs.

The STT-MTJ SPICE model presented in [16] includes a (deterministic) decision circuit to control a bistable circuit which shows an immediate switching between parallel (P) and antiparallel (AP) states (Fig. 5). The decision circuit comprises two capacitors (C_1 and C_2), which are excited by two current sources (I_1 and I_2) and connected in parallel to realize the relationship between the critical switching time and the critical switching current. In fact, the rate of the charge/discharge of the capacitors is a function of the current i flowing through the MTJ and is determined by [16]

$$I_1 = \exp(-\Delta[1 - i/I_{C0(AP\rightarrow P)}]) \quad (1)$$

and

$$I_2 = \exp(-\Delta[1 - i/I_{C0(P\rightarrow AP)}]). \quad (2)$$

Δ is the MTJ thermal stability factor and I_{C0} denotes the critical current for STT switching, which corresponds to the switching time $t_0 = 1$ns. It has been shown that the time required to charge the capacitor C_k (k =1 or 2) by exactly 1V and a capacitance of 1nF is given by [16]

$$t_{C_i} = \frac{(1\ nF)(1\ V)}{I_i} = 1\ \text{ns} \times \exp\left(\Delta\left[1 - \frac{i}{I_{C0_i}}\right]\right). \quad (3)$$

In the thermally-activated switching regime (switching time t >10 ns), (3) is identical to the relationship between the critical switching time t_p and the critical switching current I_C of AP-to-P (P-to-AP) MTJ switching [16]

$$I_C = I_{C0}\left[1 - \Delta \ln(\frac{t_p}{t_0})\right]. \quad (4)$$

As the critical values of switching time and current are usually defined for the MTJ switching probability of 50% [16],

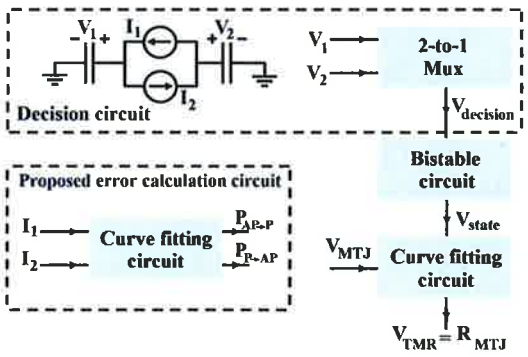

Fig. 5. Simplified equivalent circuit of the MTJ SPICE model and the proposed error calculation circuit.

the decision circuit enforces an immediate switching of the bistable circuit as soon as the switching probability is 50%. The curve fitting circuit is used to take the voltage-dependent effective TMR ratio [16] into account, which is important to determine the resistance-voltage characteristics of the MTJ. This SPICE model covers the major electrical characteristics of the STT-MTJs. It is, however, not possible to calculate the switching probabilities of the STT-MTJs required for reliability analysis and comparison of the STT-MTJ-based logic gates only based on this SPICE model (Fig. 6).

B. Modified STT-MTJ SPICE Model

Therefore, in order to calculate the STT-MTJ switching probability (P_{sw}), the theoretical expression for the thermally-activated switching regime [17] is used

$$P_{\mathrm{sw}} = 1 - \exp\left(-\frac{\tau}{t_0}\exp\left[-\Delta\left(1-\frac{I_{\mathrm{MTJ}}}{I_{\mathrm{C0}}}\right)\right]\right), \quad (5)$$

where I_{MTJ} is current flowing through the MTJ and τ is the pulse duration.

(5) has been experimentally verified in [18] and can be added to the STT-MTJ SPICE model for switching probability (error) calculations by using a curve fitting circuit shown in Fig. 5 characterized as

$$P_{\mathrm{AP}\to\mathrm{P}} = 1 - \exp\left(-\frac{\tau}{t_0}I_1\right) \quad (6)$$

and

$$P_{\mathrm{P}\to\mathrm{AP}} = 1 - \exp\left(-\frac{\tau}{t_0}I_2\right). \quad (7)$$

Fig. 6 compares the experimental results from [18] with the unmodified and the modified STT-MTJ SPICE models. It illustrates that although the decision signals V_1 in the (old) STT-MTJ SPICE predicts the correct critical switching current where the probability of the switching is 50%, it cannot fit the experimental data equally well. Therefore, the modified STT-MTJ SPICE model allows for calculating the reliabilities and error probabilities in the STT-MTJ-based logic gates.

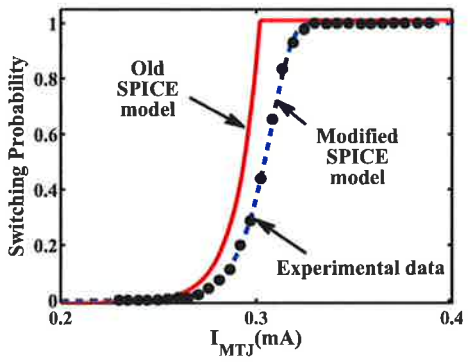

Fig. 6. AP-to-P STT-MTJ switching probability as a function of the applied current based on the modified STT-MTJ SPICE model compared to the decision signal V_1 from the (unmodified) SPICE model.

IV. Conclusion

In order to ensure a correct conditional switching behavior for any logic input pattern, IMP logic gates have to be properly modeled and optimized to minimize the error accumulations and switching failures of the TiO_2-based and MTJ-based gates, respectively. It is demonstrated that for avoiding a one-bit error in the TiO_2-based IMP gate, refreshing is required after a certain number of logic steps (10–20 steps) as the state drift errors accumulate. Due to the magnetic bistability of the MTJ, STT-MTJ-based IMP gates are free from error accumulation. It is shown that a modified SPICE model of the STT-MTJ fits the experimental data well to calculate the switching probabilities required for modeling and optimization of the circuit parameters of the stateful gates.

Acknowledgment

The work is supported by the European Research Council through the grant #247056 MOSILSPIN.

References

[1] J. Borghetti et al., "Memristive Switches Enable Stateful Logic Operations via Material Implication," *Nature*, vol. 464, pp. 873–876, 2010.
[2] H. Mahmoudi et al., "Implication Logic Gates Using Spin-Transfer-Torque-Operated Magnetic Tunnel Junctions for Intrinsic Logic-in-Memory," *Solid-State Electron.*, vol. 84, pp. 191–197, 2013.
[3] H. Mahmoudi et al., "MRAM-based Logic Array for Large-Scale Non-Volatile Logic-in-Memory Applications," *Proceedings of NANOARCH*, pp. 26–27, 2013.
[4] M. D. Pickett et al., "Switching Dynamics in Titanium Dioxide Memristive Devices," *J. Appl. Phys.*, vol. 106, p. 074508, 2009.
[5] E. Robinson et al., "Compact Method for Modeling and Simulation of Memristor Devices: Ion Conductor Chalcogenide-Based Memristor Devices," *Proceedings of NANOARCH*, pp. 1–4, 2010.
[6] S. Shin et al., "Compact Models for Memristors Based on Charge-Flux Constitutive Relationships," *IEEE Trans. Computer-Aided Design*, vol. 29, pp. 590–598, 2010.
[7] S. Benderli et al., "On SPICE Macromodelling of TiO_2 Memristors," *Electron. Lett.*, vol. 45, pp. 377–379, 2009.
[8] Á. Rák et al., "Macromodelling of the Memristor in SPICE," *IEEE Trans. Computer-Aided Design*, vol. 29, pp. 632–636, 2010.
[9] D. B. Strukov et al., "The Missing Memristor Found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.
[10] H. Abdalla et al., "SPICE Modeling of Memristors," *Proceedings of the ISCAS*, pp. 1832–1835, 2011.
[11] G. J. Simmons, "Generalized Formula for the Electric Tunnel Effect between Similar Electrodes Separated by a Thin Insulating Film," *J. Appl. Phys.*, vol. 34, pp. 1793–1803, 1963.
[12] H. Mahmoudi et al., "State Drift Optimization of Memristive Stateful IMP Logic Gates," *Proceedings of IWCE*, pp. 243–244, 2012.
[13] S. Kvatinsky et al., "Memristor-based IMPLY Logic Design Procedure," *Proc. IEEE Int. Conf. Comput. Design*, pp. 142–147, 2011.
[14] D. Strukov et al., "Exponential Ionic Drift: Fast Switching and Low Volatility of a Thin-Film Memristors," *Appl. Phys. A*, vol. 94, pp. 515–519, 2009.
[15] H. Mahmoudi et al., "Reliability Analysis and Comparison of Implication and Reprogrammable Logic Gates in Magnetic Tunnel Junction Logic Circuits," *IEEE Trans. Magn.*, vol. 49, pp. 5620–5628, 2013.
[16] J. D. Harms et al., "SPICE Macromodel of Spin-Torque-Transfer-Operated Magnetic Tunnel Junctions," *IEEE Trans. Electron Devices*, vol. 57, pp. 1425–1430, 2010.
[17] Y. Higo et al., "Thermal Activation Effect on Spin Transfer Switching in Magnetic Tunnel Junctions," *Appl. Phys. Lett.*, vol. 87, p. 082502, 2005.
[18] M. Hosomi et al., "A Novel Nonvolatile Memory with Spin Torque Transfer Magnetization Switching: Spin-RAM," *Tech. Dig. IEDM*, pp. 459–462, 2005.