Magnetic Tunnel Junctions for Future Memory and Logic-in-Memory Applications

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***Abstract*—Memories based on charge storage are gradually approaching the physical limits of scalability. Magnetoresistive random access memory (MRAM) with spin-transfer torque (STT) is a promising candidate for future universal memory. However, the reduction of the switching current density and/or switching time while maintaining high thermal stability are the main challenges of this memory cell. A substantial decrease of the switching time in in-plane magnetic tunnel junctions is achieved by a special design of the free magnetic layer. The scaling potential of this cell based on the thermal stability analysis is discussed. The designed non-volatile memory cell is promising for STT-MRAM arrays. Introducing non-volatility into logic circuits is critical to reduce the standby power and enable instant-on applications. Recently, circuits containing MRAM cells for logic were presented. The logic operations are implemented by using reprogrammable- and implication-based magnetic tunnel junction (MTJ) logic gates providing a new intrinsic logic-in-memory computational platform. A critical analysis of possible tradeoffs in different designs of stateful logic architectures is presented. The analysis indicates that MRAM-based logic is a well suited for high performance parallel non-volatile computations.**

***Keywords*—magnetic tunnel junction, spin-transfer torque, magnetoresistive RAM, logic-in-memory, non-volatile computations**

I. INTRODUCTION

Continuous miniaturization of CMOS devices is the driving force behind the tremendous increase in performance, speed, and density of modern integrated circuits. Numerous outstanding technological challenges have been resolved during this exciting journey. Among the most crucial technological changes recently adopted by the semiconductor industry was the introduction of a new type of multi-gate three-dimensional transistor [1]. This technology combined with strain techniques and high-k/metal gate dielectrics offers great performance and power advantages over the planar structures and allows steady scaling to 14nm feature size. There are good indications that device miniaturization with necessary technological breakthrough will continue its pace down to the 10nm technology node. In order to sustain further scaling a possible modification in the channel material with improved characteristics, which until recently was kept pristine, is foreseen. However, fundamental physical limitations such as leakage, high power densities, process variability, and elevated costs will gradually bring the scaling of the classical CMOS devices to an end. Therefore, investigating possible alternative technologies to replace or at least to supplement CMOS is important to further enhance the performance of logic devices and circuits.

The principle of MOSFET operation is fundamentally based on the charge degree of freedom of an electron: the electron charge interacts with the gate induced electrostatic field which can close the transistor by creating a potential barrier. Another intrinsic electron property, the electron spin, attracts much attention as a possible candidate for complimenting or even replacing the charge in future electron devices. The electron spin state is characterized by one of the two of its possible projections on a given axis and could be potentially used in digital information processing. In addition, it takes an amazingly small amount of energy to invert the spin orientation, which is necessary for low power applications.

Spintronic devices, especially MgO-based MTJs, are strong candidates to replace CMOS based memory due to their non-volatility and compatibility with CMOS technology [2]. A MTJ device consists of a free ferromagnetic layer, a fixed ferromagnetic layer with pinned magnetization direction, and a non-conductive tunnel barrier separating them. The magnetization direction of the free layer can be switched freely between a parallel (P) and an antiparallel (AP) state (with respect to the magnetization direction of the fixed layer) using an external magnetic field or the STT effect. The MTJ exhibits a low resistance state (LRS; P) across the tunnel barrier for the parallel magnetization alignment and a high-resistance state (HRS; AP) for the anti-parallel alignment. The STT switching technique [3, 4] allows purely electrical switching of the MTJ state between P and AP and vice versa thus eliminating the physical mismatch between reading and writing the information in the MTJ. The STT switching also enables smaller switching energies with scaling the MTJ dimensions down. MRAM with STT induced switching MTJs as memory cells combines the speed of static RAMs (SRAMs), the density of dynamic RAMs (DRAMs), and the non-volatility of flash memory, and thus has all the characteristics of a universal memory.

Distributing non-volatile memory elements over a CMOS logic circuit is expected to address some of the above described limitations to CMOS scaling by providing ultra-low power and

fast operation as it eliminates the static leakage (standby) power dissipation and reduces interconnection delay [5]. Furthermore, MTJ technology is attractive for building logic configurations which combine non-volatile memories and logic circuits (so-called logic-in-memory architecture) to overcome the leakage power issue [6, 7].

First, we review the recent advances and main challenges in building state-of-the-art STT-MRAM cells and their optimization. After that, a concept for an intrinsic logic-in-memory architecture based on the implication logic gate composed of two arbitrary memory cells in the STT-MRAM array is introduced.

II. MEMORY

Apart from good scalability, a new type of memory must exhibit low operating voltages, low power consumption, high operation speed, long retention time, high endurance, and a simple structure [8]. One of the most promising candidates among emerging technologies for future universal memory is STT-MRAM. Currently, STT-MRAM has been demonstrated on 64Mb test chips [9].

In conventional field-driven MRAM, switching the magnetization of a free layer is performed by applying a magnetic field. The writing operation is carried out by the current flowing through the wires. The current required for generating the magnetic field for the switching increases, when the wire cross-section decreases, leading to the problem of scaling MRAM cells. Therefore, MRAM cells based on a magnetic field switching exhibit a scalability limit of about 90nm. In contrast to field-driven MRAM, STT-MRAM does not require an external magnetic field. Switching between the two states (P and AP) occurs due to the spin torque exerted on a free layer by spin-polarized current flowing through the MTJ. In general, scalability is not a problem for the STT-MRAM cell, since reducing the size of the cell leads to a reduction of the current required for switching.

The theoretical prediction of the STT effect was made independently by Slonczewski [3] and Berger [4]. When electrons pass through the thick fixed magnetic layer, spins of electrons become aligned with the magnetization of the fixed layer. When these spin-polarized electrons enter the free layer, their spin orientations are getting aligned with the magnetization of the free layer within a transition layer of a few angstroms. Because of their spin orientation changed within the free layer, they exert a torque on the magnetization of the layer. It can cause magnetization switching, if the torque is large enough to overcome damping. Smaller torque values result in magnetization precession around the effective magnetic field.

The spin-polarized current is only a fraction of the total charge current. Therefore, relatively high current densities are required to switch the magnetization direction of the free layer. The reduction of the current density required for switching and/or the increase of the switching speed without compromising the thermal stability are the most important challenges in this area [10].

The magnetization switching can occur not only under the influence of the spin-polarized current but also spontaneously due to thermal fluctuations. This is an unwanted event which leads to loss of the stored information. Thus another important parameter of MRAM is the ratio of the thermal stability barrier height to the operating temperature T.

The thermal stability factor for MTJs with the magnetization direction perpendicular to the interfaces of the fixed and free layers is described by the interface-induced perpendicular anisotropy field H_K^{perp} as:

$$\Delta_{perp} = \frac{M_S \cdot \left(H_K^{perp} - 4\pi M_S\right) \cdot V}{2k_B T}. \quad (1)$$

Here, M_S is the saturation magnetizations, V is the volume of the free layer, k_B is the Boltzmann constant. To increase the thermal stability factor it is sufficient to increase the cross-section of the MTJs , however, due to a domain formation, this is limited to approximately 70nm diameter, therefore increasing the thermal stability factor of perpendicular MTJs above 40-50 requires a more complex cell structure.

Perpendicular MTJs yield higher density as compared to the in-plane magnetization MTJs. Another advantage of using perpendicular MTJs for STT-MRAM is the fact that the switching paths by spin transfer torque and thermal agitation are the same. Therefore, the critical switching current for perpendicular-MTJs is proportional to the thermal stability factor. However, although perpendicular MTJs with an interface-induced anisotropy show potential, they still require damping reduction and thermal stability factor increase engineering.

The thermal stability factor for in-plane MTJs is determined by the shape anisotropy magnetic field $H_K^{in-plane}$ as:

$$\Delta_{in-plane} = \frac{M_S \cdot H_K^{in-plane} \cdot V}{2k_B T}. \quad (2)$$

To increase the thermal stability factor it is sufficient to increase the thickness of the free layer and/or the aspect ratio. However, the switching under the influence of the spin current is due to precession and is thus following a path when the magnetization must get out of plane. This leads to an additional large contribution $2\pi M_S^2 V$ to the switching barrier to overcome which results in high switching current densities. Therefore, the search for new materials and innovative architectures for MTJ structures is urgently needed.

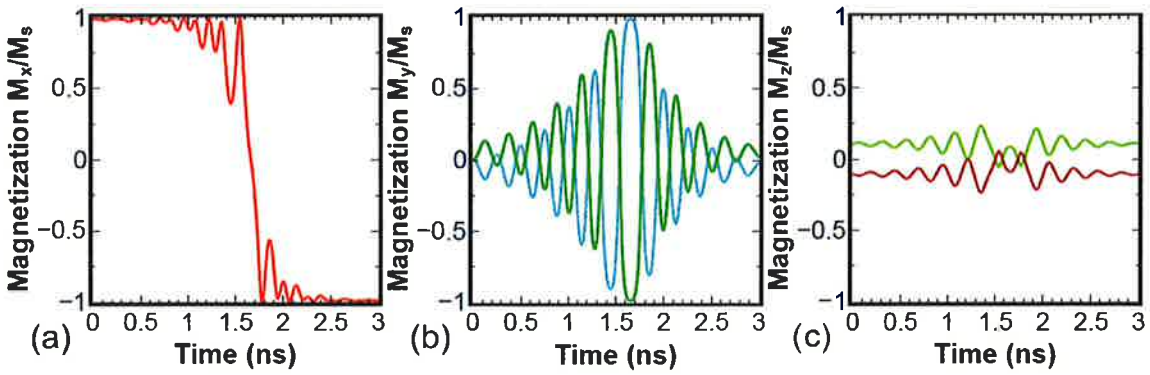

Fig. 1. Magnetization components versus time for an elliptical 52.5×25 nm^2 MTJ with a composite free layer.

A substantial decrease of the switching time in in-plane MTJs can be achieved by a special geometrical design of the free magnetic layer. To illustrate it, let us consider an in-plane MTJ with the free layer having the elliptical cross-section with the long and short axis along the *OX* and *OY* axis, correspondingly. The cross-section of the free layer is similar to the one of the fixed layer. When the current starts flowing, the spin transfer torque starts acting on the free layer. This results in an out-of phase precession motion of the magnetization of the end domains around the long axis. However, the torque in the central region remains marginal. As the amplitude of the end domains' precession increases, the central region preserves its initial orientation and prevents the whole layer from alternating its magnetization orientation. Therefore, the idea is to remove the central region along the short axis, which binds the two end domains together and prevents the switching. The end domains become virtually independent, which results in a substantial switching time and current reduction [11]. The peculiarities of the switching process are illustrated in Fig.1. The total magnetization along the *OX* axis alternates its direction after a current pulse as short as 2ns (Fig.1a). The dynamics of the magnetization orientations of the two semi-elliptic parts of the composite layers is shown in Fig.1b and Fig.1c. Fig.1b confirms that the switching of the two parts appear out-of-phase. Most importantly, the magnetizations of both parts and, therefore, the total magnetization remains in-plane during switching (Fig.1c). Therefore, the switching proceeds through the state, when the magnetizations of both parts of the free layer are along its shorter axis and anti-parallel to each other. A careful analysis demonstrates that this state provides the minimum energy barrier separating the two equilibrium magnetization states and thus determining the thermal stability of the structure. Thus, we conclude the in-plane STT-MRAM cell with the composite free layer ensures that the switching and thermal barriers are the same. As in a perpendicular MTJ, this guarantees faster switching by lower currents. In contrast to perpendicular MTJs, the thermal stability factor can be easily boosted by increasing the free layer thickness, which makes STT-MRAM with the composite free layer promising for future universal memory applications.

III. LOGIC-IN-MEMORY

Using spin-transfer torque to switch a magnetic tunnel junction is one of the most promising non-volatile storage technologies, which combines the advantages of CMOS compatibility, high speed, high density, unlimited endurance, and scalability. Distributing non-volatile memory elements over the CMOS logic circuit plane (so-called logic-in-memory architecture) can provide extremely low standby power consumption and instant start-up by holding the information in the MTJs and eliminating the need for refreshing pulses which are critical for CMOS-based memory elements. Furthermore, by using the MTJ technology the effective area and interconnect delay can be reduced due to easy three-dimensional integration of the MTJs on top of the CMOS layers.

However, in hybrid CMOS/MTJ circuits the MTJs are used only as ancillary devices which store the computation results. Therefore, sensing amplifiers are required for reading the data at each logic stage and providing the next stage with an appropriate voltage or current signal as input. This limitation increases the device count, delay, and power consumption. Furthermore, the generalization to large-scale logic systems is problematic.

Recently, MTJ-based implication logic gates (Fig.2a) have been proposed [12], in which the MTJs are used as the main devices for logical computations and thus intrinsically enable logic-in-memory architectures. By replacing the MTJ devices with one-transistor/one-MTJ (1T/1MTJ) cells (Fig.2b), the implication logic gates are realized in MRAM arrays to provide large-scale non-volatile magnetic circuits [13]. Due to the structural asymmetry caused by the resistor R_G, two MRAM arrays are required in this implementation. For performing the implication operation, a source (target) MTJ can be selected only in the MRAM array which is (not) serially connected to R_G. Therefore, read/write operations are required to readout the output of any logic operation from the target array and to write it into the source array as an input for the next logic steps. This asymmetry issue is addressed by using the access transistors as voltage-controlled resistors. In fact, when two voltage pulses with different amplitudes are

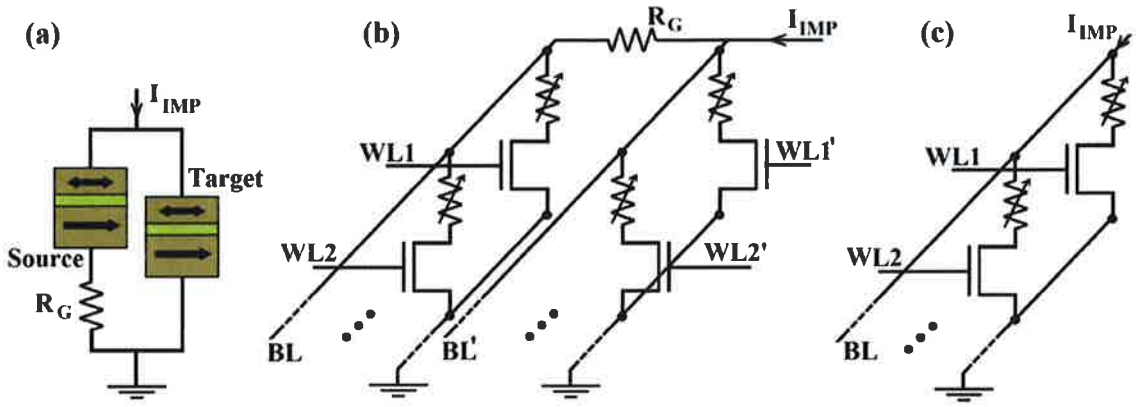

Fig. 2. (a) MTJ-based implication logic gate [12]. Asymmetric [13] (b) and symmetric [14] (c) MRAM-based implication logic arrays.

simultaneously applied to arbitrary word lines (WLs) in a MRAM array, the transistors have differently biased and thus exhibit different channel resistance.

(Fig.2c). This enables highly flexible computations without any need for intermediary read/write operations. Therefore, it addresses also the multiple non-volatile fan-out issue [14]. Furthermore, the MRAM-based implementation enables independent access to all input MTJs for STT writing and thus brings significant advantages related to scalability and energy consumption [15]. However, the non-zero ON-resistance of the access transistors decreases the effective TMR of the 1T/1MTJ cells by about10% [7] and this increases the average error probabilities by a factor of < 2 [14].

Based on the symmetric implication (Fig.2c), parallel MRAM arrays can be used to perform simultaneous operations on the same word lines to decrease the total number of required serial steps for implementing complex Boolean functions [16]. Parallel MRAM-based computation is performed by applying the same current pulses to arbitrary bit lines (BLs) and two voltage pulses to the WLs simultaneously, by using the bit line and word line drivers.

IV. Conclusion

An efficient coupling between the electrical and the magnetic degree of freedom makes STT-MRAM a viable candidate for future universal memory. Furthermore, the use of STT-MRAM cells as implication logic gates opens the way towards intrinsic logic-in-memory architecture, where the same elements are employed to store and to process the information.

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