Wed-C-11:00
Submicron XCT for failure analysis in advanced packaging
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In order to embed more functionality and performance into the same design space, 3D IC integration technology is one of the routes towards further miniaturization of ICs and consequently, printed circuit boards. 3D TSV (through silicon via) stacking of wafers or dies requires die-to-die interconnections to conduct electricity and heat. Typically micro bump contacts with solder (e.g. AgSn) and Cu TSV are used. Process and quality control of these advanced packaging processes and the resulting 3D products is challenging, but a necessity to avoid costly device failures due to packaging faults. We employed a lab-source microfocus X-ray computed tomography system to demonstrate the capability of non-destructive detection and characterization of such die-to-die interconnections with features in the micron range. Structural characteristics and flaws, such as electrical shorts, voids, filling faults, or composition features could be reliably identified. We demonstrate the use of submicron X-ray computed tomography for non-destructive process development, process monitoring and failure analysis in 3D TSVs stacks on a packaged test chip with dimensions 10 × 10 × 0.9 mm³ that consists of six chip layers with TSVs and microbumps as well as AgSn solder.

Wed-C-11:20
The effects of etching and deposition on the performance and stress evolution of open through silicon vias
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The effects of silicon etching using the Bosch process and LPCVD oxide deposition on the performance of open TSVs are analyzed through simulation. Using an in-house process simulator, a structure is generated which contains scalloped sidewalls as a result of the Bosch etch process. During the LPCVD deposition step, oxide is expected to be thinner at the trench bottom when compared to the top; however, additional localized thinning is observed around each scallop. The scalloped structure is compared to a structure where the etching step is not performed, but rather a flat trench profile is assumed. Both structures are imported into a finite element tool in order to analyze the effects of processing on device performance. The scalloped structure is shown to have an increased resistance and capacitance when compared to the flat TSV. Additionally, the scalloped TSV does not perform as well at high frequencies, where the signal loss is shown to increase. However, the scallops allow the TSV to respond better to an applied stress. This is due to the scallops' enhanced range of motion and displacement, meaning they can compensate for the stress along the entire sidewall and not only on the TSV top, as in the flat structure.

Wed-C-11:40
Advanced methods for mechanical and structural characterization of nanoscale materials for 3D IC integration
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Managing the emerging internal mechanical stress in chips particularly if they are 3D stacked is a key task to maintain performance and reliability of microelectronic products. Hence, a strong need of a physics-based simulation methodology/flow emerges. This physics-based simulation, however, requires materials parameters with high accuracy. A full-chip analysis can then be performed, balancing the need for local resolution and computing time. The key for an efficient simulation of a 3D stacked IC is a comprehensive database with material properties for multiple scales for the affected materials. Therefore, effective "composite-type" materials data for several regions of interest are needed. Advanced techniques to measure FEA- and design-relevant properties such as adhesion properties, local and effective Young's modulus, and effective CTE values are presented.

Wed-C-12:00
Stress Analyses of High Spatial Resolution on TSV and BEoL Structures
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Knowledge and control of local stress development in BEoL stacks and nearby TSVs in advanced 3D integrated devices is a key to their thermo-mechanical reliability. The paper presents a combined simulation / measurement approach to evaluate stresses generated in the result of the TSV and BEoL stack manufacturing and 3D bonding processes. Stress measurement methods of high spatial resolution capability (microRaman and FIB based stress release techniques) are used to obtain stress data from real components as manufactured. Finite element analysis (FEA) allows a more accurate interpretation of measurements results as well as a subsequent comprehensive analysis of failure behaviour. The paper gives an introduction to the applied local stress measurement on advanced multi-layer systems and 3D integration components referring to the state-of-art capabilities and limitations. The need of experimental stress data generation is illustrated on FEA examples. Illustration is given for FEA applications on 3D IC integration components currently lacking appropriate residual stress input for an assumed initial state.