RTN and PBTI-induced Time-Dependent Variability of Replacement Metal-Gate High-k InGaAs FinFETs

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***Abstract*—**We study RTN and PBTI in nanoscale InGaAs FinFETs fabricated on 300mm Si wafers. The average instability is found to be comparable to planar structures, but significantly larger when compared to Si devices. Although the novel devices follow the same time-dependent variability statistics and the corresponding area-scaling as their Si counterparts, a larger stochastic impact of single defects on the device characteristic is found to induce larger aging-related variance. We ascribe this to a more percolative channel conduction induced by still excessive interface and channel defectivity.

Introduction

High mobility channel FinFETs will be required for further CMOS performance enhancement in N7 and beyond [1]. Ge and III-V compounds are the frontrunners for *p*- and *n*-type channels respectively [2]. High intrinsic electron mobility (~3000cm^2/Vs [3,4]) has been recently demonstrated in InGaAs channel devices with "self-cleaning" [5] Al_2O_3–based dielectric stacks, with promising interface quality (D_{it} ~3-5×10^{11} cm^{-2}eV^{-1} [6]) and subthreshold swings (~75 mV/dec [3]). Moreover, imec has recently demonstrated the integration of *InGaAs FinFETs on 300mm Si wafers*, with replacement metal gate Al_2O_3/HfO_2 gate stack (Fig. 1) [7]. In this paper, we focus on the *PBTI reliability* of these InGaAs FinFETs. While the mean instability is found to be identical to previously studied planar structures [8] and significantly larger w.r.t. Si devices, *the nanoscale fins* with varying effective area (Table I) *enable microscopic insights into the instability via Random Telegraph Noise* (RTN) *and time-dependent variability* induced by capture/emission of channel electrons in/from oxide defects. We observe that *InGaAs FinFETs follow the same time-dependent variability statistics and the corresponding area-scaling as their Si counterparts* [9-12]. However, experimental data show *larger-than-Si device-to-device variability* in InGaAs devices: *we trace it to larger stochastic impact of single defects* on the device characteristics and *we discuss its possible origins*. We argue that while showcasing the best, i.e., tail, behavior demonstrates the potential of InGaAs, *correct understanding and description of the instability distributions in nanoscale non-planar devices (e.g., FinFETs and Nanowires) are essential for process optimization of the new technology*.

PBTI, Hysteresis and RTN

PBTI measurements in large area FinFETs reveal the *same reliability challenge* previously observed in planar InGaAs devices (Fig. 2, solid symbols). In particular, a detrimental weak voltage dependence of PBTI is consistently found (γ~1.5), ascribed to a wide distribution of defect levels in Al_2O_3 (Fig. 2b) [8]. *High pressure* H_2 and D_2 *anneals*, expected to passivate primarily dangling bonds, *did not yield any significant electron trapping reduction* (Fig. 2a, crosses), which therefore points to an intrinsic issue of this gate oxide. Along with excessive hysteresis induced by multiple charged defects with long emission times, frequent single electron (de-)trapping events inducing significant fluctuations (i.e., *noise*) in the I_D-V_G characteristic of nanoscale FinFETs have been observed (Fig. 3). Single defect charging with gigantic electrostatic impact (e.g., ΔV_{th} ~50mV, Fig. 4) are not rare. Such large fluctuations in nanoscale FETs are already understood in terms of a potential perturbation of the underlying channel percolation configuration induced by single charged oxide defects (Fig. 5) [10,13]. By collecting the observed single-defect-induced ΔV_{th} in a Cumulative Distribution plot (Fig. 6a), an exponential distribution is seen, same as in Si devices [9]. The average impact per charge η (i.e., ~ the inverse of the slope of the distribution) is found to scale inversely with area in InGaAs FinFET (Fig. 6b), also consistently with Si data [10,11]. However η is significantly larger (i.e. ~4×) w.r.t. the charge sheet approximation for the electrostatic impact of a single charge ($\eta_0=q/C_{ox}$, Fig. 6b dashed), and also w.r.t. Si FinFETs where we have previously observed η/η_0~2× (Fig. 6b dotted, based on experimental data in [10]). Since η is expected to scale proportionally with the oxide Capacitance Equivalent Thickness (CET) [14,15], InGaAs devices suffer a penalty due to the larger channel carrier centroid displacement from the interface (i.e., 'dark space') induced by quantum effects in a low DOS semiconductor [3,16]. The CET-dependence, however, cancels out when normalizing η by η_0 (cf. Table II)—the *larger (normalized) single defect impact* has to be therefore *ascribed to more percolative channel conduction*. We have previously shown that excessive N_{it} [17] and channel material defectivity [18] induce larger η (cf. Fig. 5). We argue these two factors are responsible for the larger normalized single defect impact in InGaAs devices.

Hysteresis distributions

Each nanoscale device is expected to include a Poisson-distributed number of charging oxide defects, each defect inducing the above discussed exponentially distributed ΔV_{th} [9]. Therefore, nominally identical devices can show very disparate hysteresis (Fig. 7). Note that *it is relatively common to find devices showing almost negligible hysteresis* (Fig. 7a)—*this is just a consequence of the stochastic nature of trapping in small area devices, and cannot be claimed as*

improved reliability of some devices. Fig. 8a shows V_{th} distributions on the up- and down-sweep of I_D-V_G hysteresis measurements of multiple devices. Along with the median V_{th}-shift, an increased variance is found in the down-sweeps. This and the hysteresis ΔV_{th} distribution (Fig. 8b) are again both clear consequences of the statistics previously proposed based on Si planar data (Eq. 1, Table II). Note that the hysteresis of each device is uncorrelated with the device V_{th0} (Fig. 8c), confirming the stochastic nature of the phenomenon. Consistent with the statistics (Eq. 3) is the median hysteresis observed to be independent of the device area (Figs. 9,10), as well as larger variance observed in small area devices (Fig. 9, bars) [17]. Based on measured hysteresis variance for varying device areas it is possible to derive η independently again through Eq. 3. In agreement with the RTN step heights study, η is found to scale inversely with the device area, and to be ~4× larger than η_0 and ~2× larger than in Si devices (Fig. 11, cf. Fig. 6b). A good agreement of the values extracted with the two methods serves as a *proof of the correctness of our statistical framework in describing time-dependent variability also for InGaAs FinFETs*.

Device-to-device PBTI variability

Fig. 12 shows relaxation traces measured on a set of nominally identical devices after the same PBTI stress. Individual discharge events with distributed step heights are visible. The median PBTI shift shows a typical ~log(t) relaxation trend (Fig. 12b), and it is found to be independent of the device geometries (Fig. 13). This result implies that *gate stack optimization for improved reliability pursued on simple planar test vehicles is valid also for FinFETs*. By considering datasets pertaining to increasing relaxation times (see Fig. 12a), PBTI distributions with decreasing $\langle \Delta V_{th} \rangle$ and therefore decreasing variance (cf. Eq. 3) are obtained (Fig. 14, symbols). These PBTI-induced ΔV_{th} distributions are clearly non-Gaussian; the asymmetry and the distinct relation between median and variance are well described by Eq. 1 assuming η/η_0 =6 (Fig. 14, lines). To understand this larger η/η_0 value, hysteresis distributions were measured with increasing maximum V_G (Fig. 15): the median shift follows a weak power law of the gate voltage (γ~1.5) consistently with large area device data (cf. Fig. 2); a weak dependence of η on the maximum stress is also observed (Fig. 15b), and ascribed to *progressively worse percolative channel conduction due to increasing amounts of charged near-substrate oxide defects* inducing additional potential perturbations (see Fig. 5). Nevertheless, at low operating voltages of relevance for III-V logic, the ratio η/η_0=4 observed above is confirmed.

Projections

Based on the experimental results summarized in Table III, Fig. 16 shows projected ΔV_{th} distributions at device end-of-life. Compared to Si n-FinFETs, ~10× *larger median shifts are expected* (Fig. 16b), *with significant additional variance to be addressed by additional design margins* (Fig. 16c). Such projections are valuable when optimizing new-technology designs [19]—the larger ΔV_{th} variance might be, e.g., tackled by designing with multi-fin devices, at some expense of wafer area (Fig. 16a).

Conclusions

In nanoscale devices I_D-V_G hysteresis and PBTI-induced ΔV_{th} need to be studied in terms of their statistical distributions. *InGaAs FinFETs showed both larger median shifts and aging-induced variance* w.r.t. Si counterparts. The latter was traced to *a larger stochastic impact of single defects on the device characteristic*, ascribed to the CET-penalty of low DOS semiconductors (i.e., wider 'dark space') and chiefly to a more percolative channel conduction induced by still excessive interface and channel defectivity. *Suppressing defectivity* in channel, interface, and gate oxide appears *crucial for successful introduction of III-V devices.* This path is orthogonal to introducing suitable dielectrics with favorable defect level distribution to suppress excessive electron trapping at operating voltages [20].

References

(1) M. Bohr, "The evolution of scaling from the homogeneous era to the heterogeneous era", in *Proc.* IEDM, pp. 1.1.1-6, 2011;

(2) K. J. Kuhn, "Considerations for Ultimate CMOS Scaling", in TED 59(7), pp. 1813-1828,2012;

(3) A. Alian *et al.*, "Impact of the channel thickness on the performance of ultrathin InGaAs channel MOSFET devices", in *Proc.* IEDM, pp. 16.6.1-4, 2013;

(4) S. Takagi, M. Takenaka, "High mobility CMOS technologies using III-V/Ge channels on Si platform", in *Proc.* ULIS, pp. 1-4, 2012;

(5) M.L. Huang *et al.*, "Surface passivation of III–V compound semiconductors using atomic-layer-deposition-grown Al_2O_3", in APL(87), pp. 252104.1–3, 2005;

(6) T. Hoshii *et al.*, "Reduction in interface state density of Al_2O_3/InGaAs metal-oxide-semiconductor interfaces by InGaAs surface nitridation", in JAP 112(7), pp. 073702.1-8, 2012;

(7) N. Waldron *et al.*, "An InGaAs/InP quantum well finfet using the replacement fin process integrated in an RMG flow on 300mm Si substrates", in *Proc.* VLSI, pp. 1-2, 2014;

(8) J. Franco *et al.*, "Suitability of high-k gate oxides for III–V devices: A PBTI study in $In_{0.53}Ga_{0.47}As$ devices with Al_2O_3", in *Proc.* IRPS, pp. 1-6, 2014;

(9) B. Kaczer *et al.*, "Origin of NBTI variability in deeply scaled pFETs", in *Proc.* IRPS, pp. 26-32, 2010;

(10) J. Franco *et al.*, "Impact of single charged gate oxide defects on the performance and scaling of nanoscaled FETs", in *Proc.* IRPS, pp. 1-6, 2012;

(11) C. Prasad *et al.*, "Bias temperature instability variation on SiON/Poly, HK/MG and trigate architectures", in *Proc.* IRPS, pp. 6A.5.1-7, 2014;

(12) S.H. Shin *et al.*, "Impact of nanowire variability on performance and reliability of gate-all-around III-V MOSFETs", in *Proc.*IEDM, pp. 1-4, 2013;

(13) A. Asenov *et al.*, "RTS Amplitude in Decananometer MOSFETs: 3-D Simulation Study", in TED 50(3), pp. 839-845, 2003;

(14) A. Ghetti *et al.*, "Comprehensive Analysis of Random Telegraph Noise Instability and Its Scaling in Deca-Nanometer Flash Memories", in TED 56(8), pp. 1746-1752, 2009;

(15) J. Franco *et al.*, "Reduction of the BTI time-dependent variability in nanoscaled MOSFETs by body bias", in *Proc.* IRPS, pp. 2D.3.1-6, 2013;

(16) K. Kalna *et al.*, "Benchmarking of Scaled InGaAs Implant-Free NanoMOSFETs", in TED 55(9), pp. 2297-2306, 2008;

(17) M. Toledano-Luque *et al.*, "Degradation of time dependent variability due to interface state generation", in *Proc.* VLSI, pp. T190-191, 2013;

(18) M. Toledano-Luque *et al.*, "Quantitative and predictive model of reading current variability in deeply scaled vertical poly-Si channel for 3D memories", in *Proc.* IEDM, pp. 9.2.1-4, 2012;

(19) H. Kukner *et al.*, "Scaling of BTI reliability in presence of time-zero variability", in *Proc.* IRPS, pp. CA.5.1-7, 2014;

(20) J. Franco *et al.*, "Understanding the suppressed charge trapping in relaxed- and strained-Ge/SiO_2/HfO_2 pMOSFETs and implications for the screening of alternative high-mobility substrate/dielectric CMOS gate stacks", in *Proc.* IEDM, pp. 15.2.1-4, 2013.

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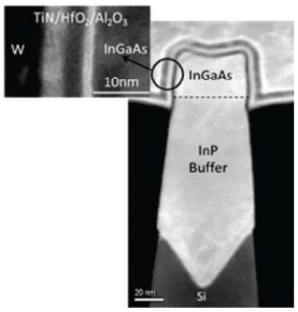

Table I – *Nominal* Device Dimensions

H_{fin}≈35nm	SINGLE	FIN	
Device	W_{fin} [nm]	L_G [nm]	A_{eff} [nm2]
A0	20	65	5850
A1	40	65	7150
A2	60	65	8450
A3	80	65	9750
A4	40	90	9900
A5	40	110	12100
A6	40	130	14300
A7	60	130	16900
A8	80	130	19500
A9	150	130	28600
A10	300	130	48100
A11	150	1000	220000
A12	500	500	285000

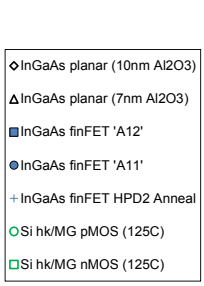

Fig. 1: TEM of a 50nm-wide InGaAs FinFET on a 300mm Si wafer [7] used in this work. Inset shows the gate stack consisting of 2nm Al_2O_3/3nm HfO_2 layers (expected EOT ~1.6nm). Table I reports *nominal* dimensions for the devices used in this work, later identified by the labels 'A0→A12'.

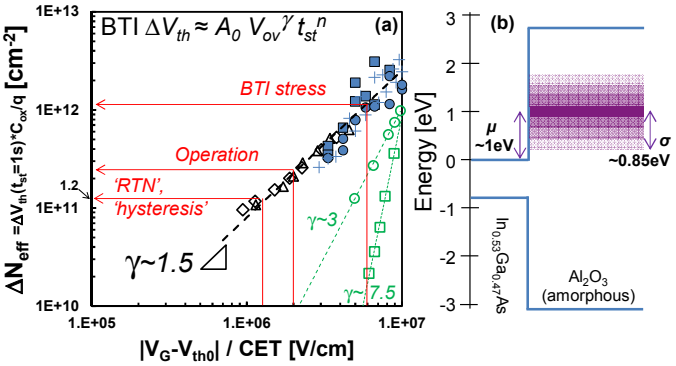

Fig. 2: **(a)** BTI shifts [$\Delta V_{th}(t_{stress}$=1s)] plotted in a CET-independent benchmark $\Delta N_{eff}(E_{ox})$ [$\Delta N_{eff}=\Delta V_{th}C_{ox}/q$, E_{ox}~V_{ov}/CET]. Similar shifts are observed for InGaAs planar [8] and FinFET devices without or with high pressure anneals (crosses). Note the large BTI shifts and the very weak voltage dependence (γ~1.5, formula inset) as compared to Si high-k/MG BTI data (green symbols), ascribed to **(b)** a wide energy distribution of oxide electron traps in Al_2O_3 [8].

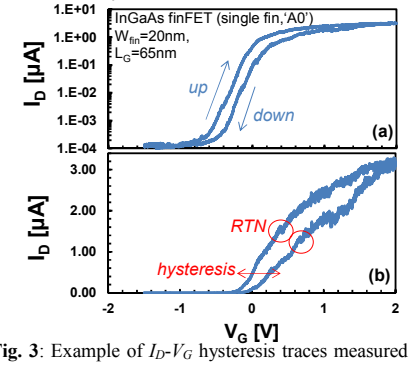

Fig. 3: Example of I_D-V_G hysteresis traces measured on nanoscale InGaAs FinFETs [**(a)** log-lin, **(b)** lin-lin scales]. Note the noise induced by (dis)charging of individual defects (RTN). Defects with $\tau_e \gg \tau_c$ remain charged after the V_G ramp-up, inducing hysteresis.

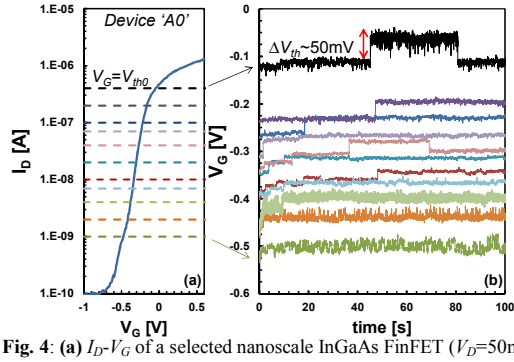

Fig. 4: **(a)** I_D-V_G of a selected nanoscale InGaAs FinFET (V_D=50mV). The biases corresponding to the indicated current levels (dashed lines) are maintained for 100 *s* to measure **(b)** RTN traces. An individual defect with gigantic impact on the device characteristic (ΔV_{th}≈50mV at V_G≈V_{th0} [10]) is consistently observed in this device.

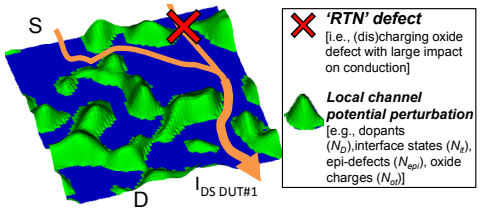

Fig. 5: A sketch of the current flow in a nanoscale channel, proceeding through percolation paths in a non-uniform potential profile [10,13,14]. An oxide defect located *on-top* of a percolation confinement point (×) can induce a large RTN fluctuation. Point charges of different nature (dopants [13-15], interface states [17], epitaxial-defects [18], *near-substrate* oxide charges [cf. Fig.15]) induce a more percolative conduction, thus enhancing the impact of individual defects.

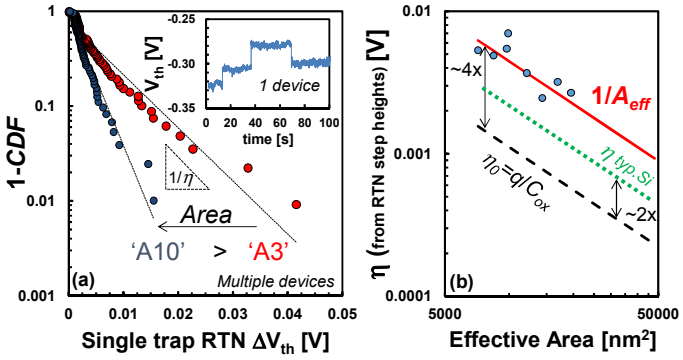

Fig. 6: **(a)** Complementary Cumulative Distribution of ΔV_{th} due to individual RTN defect (inset) observed in nanoscale InGaAs FinFETs. Note the wider exponential distribution for the smaller device area ('A3'<'A10', cf. Table I). **(b)** The average impact per defect η is inversely proportional to the device effective area, as for Si devices [10,11]. Note the large magnitude of η, ~4× larger than the charge sheet approximation for a single charge (dashed line $\eta_0=q/C_{ox}$) and ~2× larger w.r.t. Si finFETs (dotted line, from experimental data in [10]).

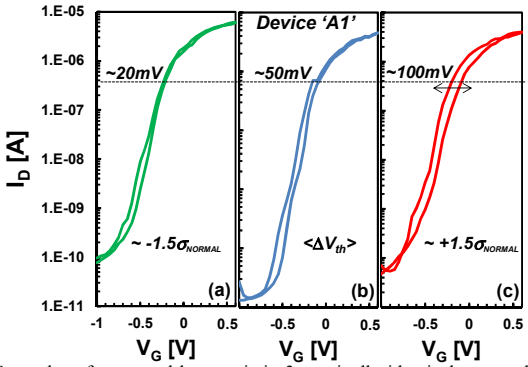

Fig. 7: Examples of measured hysteresis in 3 nominally identical nanoscale InGaAs finFETs (area 'A1', cf. Table I). Each device shows a different hysteresis magnitude, [**(a)**~20mV, **(b)**~50mV, **(c)**~100mV]. Despite the large median hysteresis, it is relatively easy to find devices showing reduced shifts. Note individual defect (dis)charging events inducing *noise* in the I_D-V_G traces.

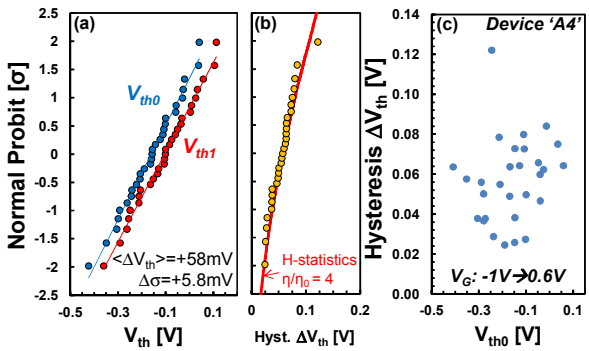

Fig. 8 (left): **(a)** Example of V_{th} distributions measured on the *up* (blue) and *down* (red) sweeps of hysteresis measurements (devices 'A4'), cf. Fig. 7. Hysteresis induces both a median V_{th}-shift (~58mV) and additional variance (Δσ~5.8mV). **(b)** The distribution of ΔV_{th} experienced by each device (symbols) is well described by the H-statistics (line; cf. Table II) [9]. **(c)** The ΔV_{th} measured in each device is uncorrelated with its initial V_{th}, confirming the stochastic nature of the phenomenon.

Table II: H-statistics (Ref. [9])
(Poisson-distributed number of charged defects with exponential-distributed impacts)

$$H_{\eta,\langle N_T\rangle}(\Delta V_{th}) = \sum_{n=0}^{\infty} \frac{e^{-\langle N_T\rangle}\langle N_T\rangle^n}{n!}\left[1-\frac{n}{n!}\Gamma(n,\Delta V_{th}/\eta)\right] \quad \text{Eq. (1)}$$

$$\text{Eq. (2)}\ \langle \Delta V_{th}(t)\rangle = \eta\,\langle N_T(t)\rangle,\ \sigma^2_{\Delta V_{th}}(t) = 2\eta\,\langle \Delta V_{th}(t)\rangle \ \text{Eq. (3)}$$

Average single defect impact (η): dependences [14,15,17,18]

$$\eta \propto \frac{CET\sqrt{N_{pp}}}{A},\quad \eta_0 = \frac{q}{C_{ox}} \propto \frac{CET}{A},\quad \frac{\eta}{\eta_0} \propto \sqrt{N_D + N_{it} + N_{epidefects} + \ldots}$$

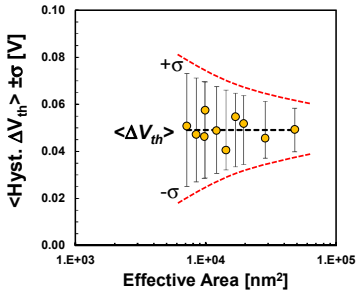

Fig. 9: Median hysteresis ΔV_{th} is shown to be independent of the device geometry [17]. This is a consequence of the average number of oxide defects per device $\langle N_T \rangle$ scaling proportionally with area (Fig. 10) and the average impact per defect η scaling inversely with area (cf. Table II, Eq. 2). However, larger variance is observed in smaller devices due to enhanced single defect impact η (cf. Eq. 3).

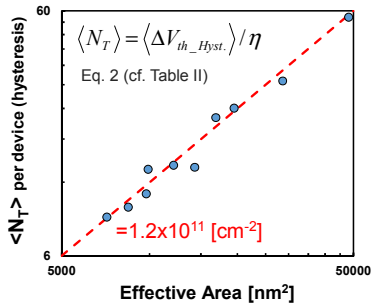

Fig. 10: The average number of defects contributing to the hysteresis increases proportionally with the device area [17]. Note: the same defect density in nanoscale devices as in large area planar and FinFET devices [cf. Fig. 2(a)] is found.

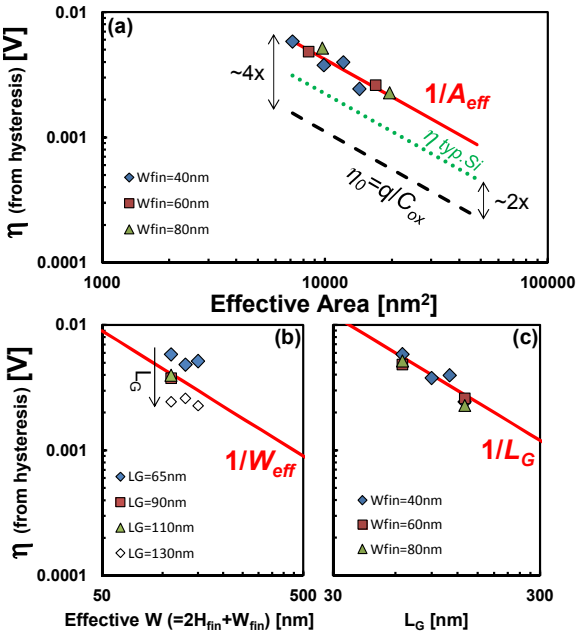

Fig. 11: Average single defect impact η extracted by modeling measured hysteresis distributions with H-statistics (cf. Eq. 3, Table II). η is observed to scale inversely with **(a)** the device effective area, and thus also with **(b)** the device effective width, and **(c)** the gate length. As for the extraction based on RTN traces (cf. Fig. 6), η values ~4× larger than η_0 and ~2× larger w.r.t. Si [10] are found. The consistency of the extracted η values confirms the validity of Eq.1 ('H-statistics') for describing the ΔV_{th} distributions also in InGaAs FinFETs.

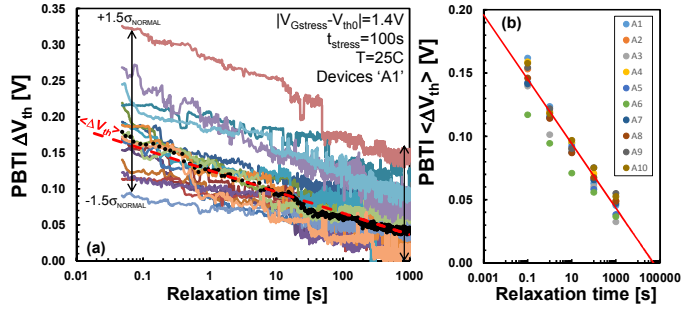

Fig. 12: **(a)** Example of PBTI relaxation traces measured in nanoscale InGaAs FinFETs (devices 'A1'). Individual defect discharge events are visible (cf. RTN traces in Fig. 4b) [9]. The median ΔV_{th} (dotted) is observed to follow a ~log(t) relaxation (dashed) from ~0.1 to 1000 s, **(b)** independently of the device geometry. As observed for planar structures [8], BTI recovery is faster in InGaAs devices as compared to Si (i.e., the ΔV_{th} recovers almost completely in a measurable period); hence, at short time scales of relevance for logic (i.e., ps), even larger than measured shifts are expected.

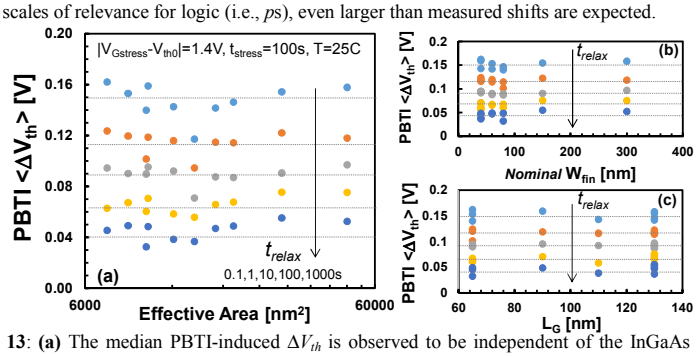

Fig. 13: **(a)** The median PBTI-induced ΔV_{th} is observed to be independent of the InGaAs FinFET effective area. No significant dependencies of the **(b)** fin width, nor **(c)** gate length are observed. Datasets for different relaxation times (i.e., for varying $\langle \Delta V_{th} \rangle$) are shown.

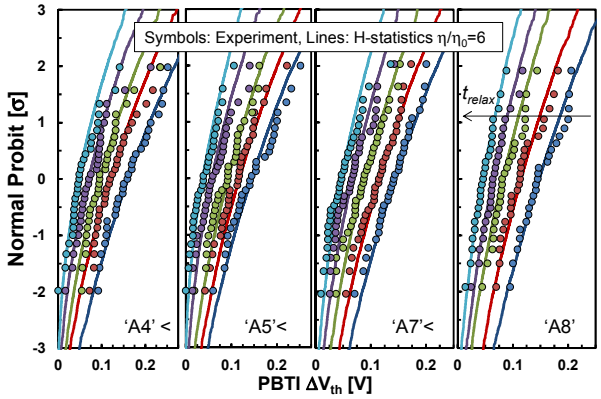

Fig. 14: The measured PBTI-induced ΔV_{th} distribution (symbols) are well described by the H-statistics with η/η_0=6 (lines). Data for 4 different nanoscale device areas ('A4'<'A5'<'A7'<'A8') are shown. Measured distributions for increasing relaxation times are shown for each area to highlight the relation between the median V_{th}-shift and the variance of the distribution, perfectly captured by the H-statistics (Table II).

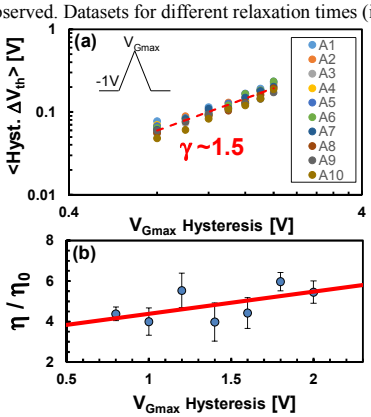

Table III – Target Operation and Extracted BTI Parameters

N-finFET	InGaAs	Si
Target Operating V_{DD} [V]	0.5	1
Operating overdrive =2/3 * V_{DD} [V]	0.33	0.66
Target CET: EOT+darkspace [nm]	1.8	1.4
Operating E_{ox} [MV/cm]	~2	~5
H_{fin} [nm]	35	35
Target W_{fin} [nm]	10	10
Target L_G [nm]	30	30
Effective Area (single fin) [nm²]	2400	2400
PBTI time exponent (n) [8,19]	0.1	0.16
η/η_0 (from Figs. 6,11) [10]	4	2
$\Delta N_{eff}(t_{st}$=1s) @Op.E_{ox} (from Fig.2)[cm⁻²]	~2e11	~1e10
$\Delta V_{th}(t_{st}$=10Y) @Op.E_{ox} [mV]	118	15

Fig. 15: **(a)** Independently of the device area, the median hysteresis shifts follow a power-law of the maximum applied V_G (inset), with exponent γ~1.5, consistently with large area planar and finFET (cf. Fig. 2a). **(b)** A weak dependence of the extracted η/η_0 values is noted and ascribed to progressive worsening of the percolative conduction (see Fig. 5). Even at low voltages a large η/η_0 value (~4×, compared to ~2× for Si [10]) is observed.

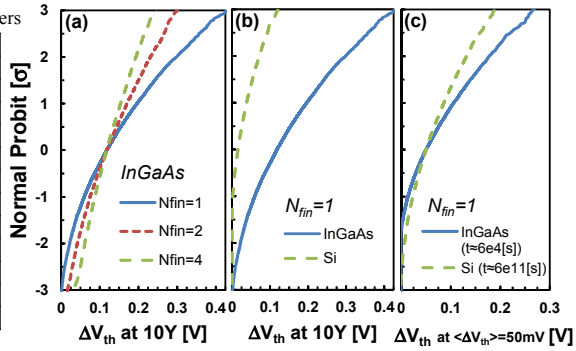

Fig. 16: Projections of device end-of-life ΔV_{th} distribution based on experimental data shown here and summarized in Table III. **(a)** The wide ΔV_{th} variance induced by the larger impact of individual defects in InGaAs FinFETs (i.e., η/η_0~4×) could be tackled by increasing the effective device area by using multi-fin devices (projections shown for N_{fin}=1,2,4), at some expense of wafer area; **(b)** compared to Si FinFETs, ~10× larger $\langle \Delta V_{th} \rangle$ at 10 year is expected, together with an increased variance. **(c)** Projected distributions for a fixed $\langle \Delta V_{th} \rangle$=50mV in InGaAs and Si finFETs highlight the additional variance.