Manufacturing of 3D Integrated Sensors and Circuits

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***Abstract*— 3D integration of functions such as sensors and circuit elements enables miniaturized and cost-effective smart systems. Wirebonds are replaced by Through Silicon Vias (TSVs) and Wafer Level Packaging (WLP) for shorter conductive paths and reduced form factor. This paper reviews prior art and presents a comprehensive set of data from volume manufacturing of 3D integrated optical sensors and circuits using a "via last" manufacturing flow. 3D specific yield detracting processes such as patterning of open TSVs, wafer bonding, and etching are analyzed and discussed. Functional test yields equivalent to standard CMOS process yields can be achieved.**

Keywords—3D integration; sensor; circuit; through silicon via; manufacturing; yield;

I. INTRODUCTION

Sensors in combination with integrated circuits play a key role in the realization of miniaturized smart systems. Optical sensors are particularly important for both, imaging applications and sensing of parameters as diverse as human health parameters, ambient light conditions and/or proximity, and nature of objects. Cost reduction and system miniaturization drive the introduction of Wafer Level Packaging (WLP) and 3D integration [1,2]. Replacing wirebonds from classical packaging with Through Silicon Vias (TSV) and solder bumps leads to a considerable package form factor reduction (footprint, height) as can be seen from Fig.1.

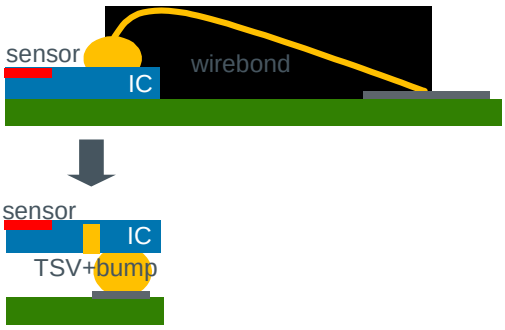

Fig. 1. Form factor reduction for SoC integrated sensor by replacing wirebonds with TSV and bumps.

Integrated Circuits (ICs) with System on Chip (SoC) optical sensors need to face the environment such that instead of flipchip WLP an electrical connection through the silicon chip, a TSV, is needed to achieve form factor benefits and shortened electrical conduction paths which enable, e.g., reduced signal noise.

If the optical sensor area can be chosen to match the integrated circuit's chip size, a 3D integrated sensor and IC structure with 100% optical fill factor can be achieved which is especially beneficial for high resolution imaging applications. Integration is performed by Wafer to Wafer (W2W) direct fusion bonding (Fig.2, left). Alternatively, if there is a mismatch between chip sizes, the sensor and the IC can be stacked Die to Wafer (D2W).

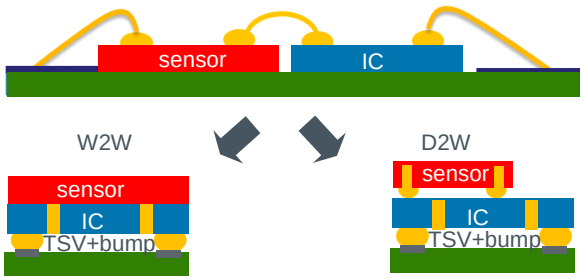

Fig. 2. Form factor reduction for sensor and IC system in a package by replacing wirebonds with TSV and bumps. Integration by W2W bonding for matched sensor and IC die sizes (bottom left) and D2W stacking, if the IC die size is larger than sensor die size (bottom right).

While there are many reports on theoretical and experimental results on 3D integration with TSV and WLP, manufacturing experience is still very limited [3] and there are only very few recent reports on first limited aspects of 3D manufacturing such as [4,5,6]. Therefore, it is an objective of this paper to document a first set of manufacturing data, a related analysis, and a discussion of manufacturing challenges.

II. EXPERIMENTAL

A. Fabrication of 3D integrated optical sensors and circuits

An open TSV technology with 100µm TSV diameter for enabling a 3D integrated photosensor IC as shown in Fig.2(left) and Fig.3(right) was developed and qualified for mass production by end of 2010 [7,8,9]. An active interposer technology with 80µm open TSV and backside metal redistribution layer was qualified recently.

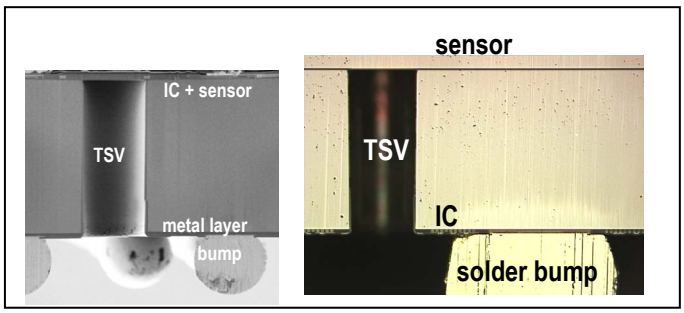

Fig. 3. SEM X-section of an active silicon interposer from Fig.1 (left) and a 3D integrated (photo-) sensor and integrated circuit from Fig.2 (right).

In both cases the TSV aspect ratio is 2.5. The via is isolated

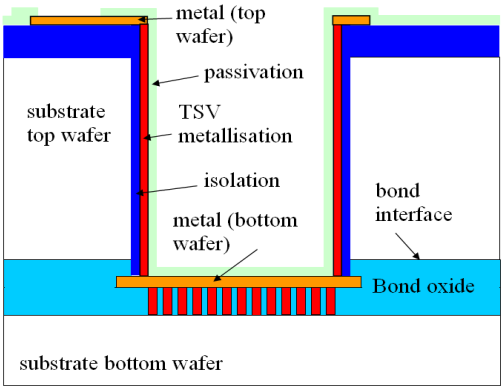

Fig. 4. Schematic cross-section of an open TSV (Kraft et al. [8]).

with a CVD oxide isolation spacer. W is used as conductive layer covered by standard CMOS passivation. A cross-section of the upper TSV edge is shown in Fig.5.

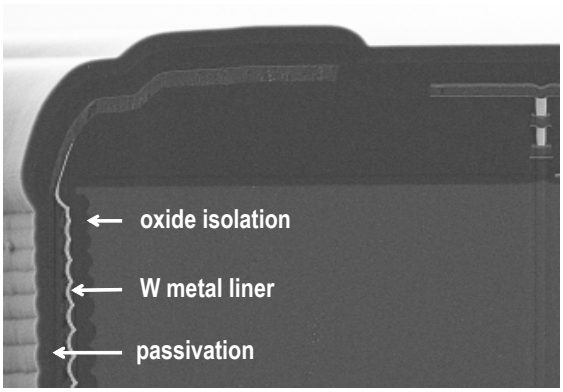

Fig. 5. Top edge cross-section of an open TSV.

III. RESULTS AND DISCUSSION

A. Reliability

Long term stability of the TSV process was investigated. Both, technology and product qualification, for the structures from Fig.3 were performed. Fig.6 shows an example of stability of the TSV resistance after thermal cycling. Further details are described in [9].

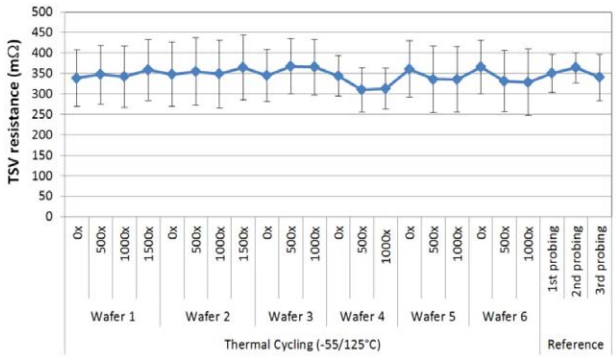

Fig. 6. TSV resistance as a function of thermal cycles versus reference (Cassidy et al. [9]).

A TSV breakdown voltage larger than 200V was achieved and the TSV bulk leakage was less than 1pA for voltages below 10V [9].

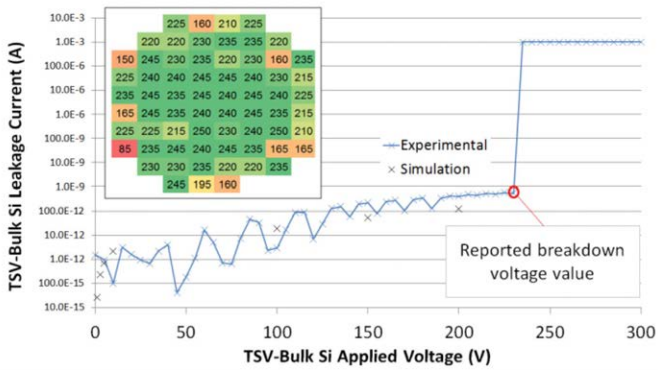

Fig. 7. TSV bulk Si leakage current as a function of applied voltage. Inset: TSV breakdown voltage [V] (Cassidy et al. [9]).

TSV technology qualification tests on a 0.525 x 0.9mm^2 daisy chain test chip were passed on large sample sizes (Table I). A Moisture Sensitivity Level (MSL) "1" was achieved.

TABLE I.

	Standard	Condition	Sample Size	Result
High Temperature Storage Life Test	JESD22-A103	150°C, 1000h	58.000pcs	pass
Unbiased HAST	JESD22-A118	130°C / 85% r.h, 168h	34.000pcs	pass
Temperature Cycle Test	JESD22-A104	-55°C / +125°C, 200c	22.000pcs	pass

Other test-chip and product reliability tests also showed a performance equivalent to standard CMOS data without TSVs.

B. *In-line and electrical parameters*

Fundamental process differences in 3D integrated ICs with open TSV versus standard CMOS processes, which can be seen from Fig.4 are (i) deep reactive ion etching (ii) spacer etching inside TSVs, (iii) the need for conformally depositing resist inside and outside TSVs or resist lamination over cavities for metal layer structuring, and (iv) void-free bonding of functional layers such as for the IC and the photosensor (Fig.2, right). All of these processes demand monitoring in manufacturing both, in-line and by electrical parameters. In-line metrology has been reviewed recently (e.g. [10,11]). While there is a general need for further development of metrology solutions there are currently no manufacturing–proven methods for non-destructive monitoring of layer thicknesses inside TSVs or for bond strength control. Bond-voids can, however, be monitored by Surface Acoustic Microscopy (SAM) as can be seen from Fig. 8.

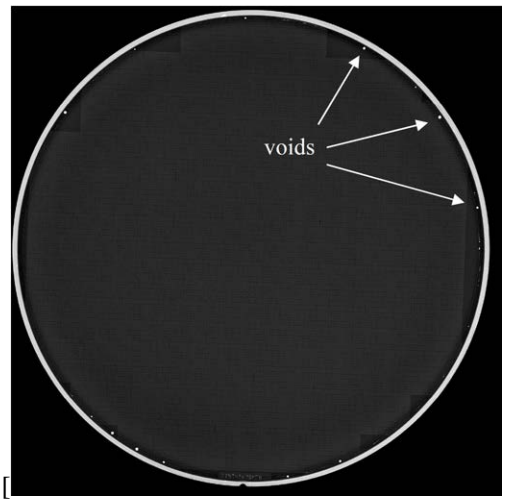

Fig. 8. SAM image of a direct bonded sensor and IC wafer pair. White spots near the wafer edge are voids (Kraft et al. [8]).

For bond strength control a reliable but destructive method has been developed (Micro-Chevron test, Fig.9 [11,13]). A model for crack propagation in permanently fusion-bonded structures such as Fig.2(right) was also developed and applied for lifetime estimates [12].

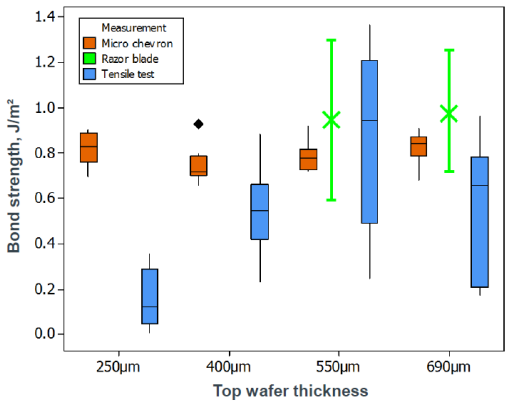

Fig. 9. Comparison of the accuracy of prior destructive bond-strength measurement methods with the Micro-Chevron test (Siegert et al. [13]).

Scribe line monitors for in-line measurement of electrical TSV parameters were also developed. Selected results demonstrating parameter stability during manufacturing are shown in Fig.10.

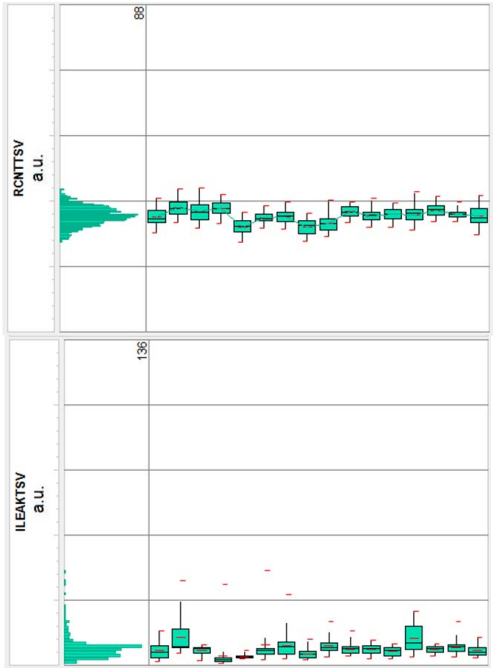

Fig. 10. Stability of wafer acceptance test parameters, such as TSV resistance (top) and TSV leakage (bottom), over multiple manufacturing lots.

C. *Manufacturing yield*

Manufacturing yields are monitored at wafer and component level. At wafer level full product related functional tests are performed after CMOS manufacturing and after 3D integration. The example of a typical wafer map (Fig.11) after TSV and bumping shows very high yields equivalent to CMOS process yields. This is a result of the strategy to use CMOS fabrication processes and materials wherever possible.

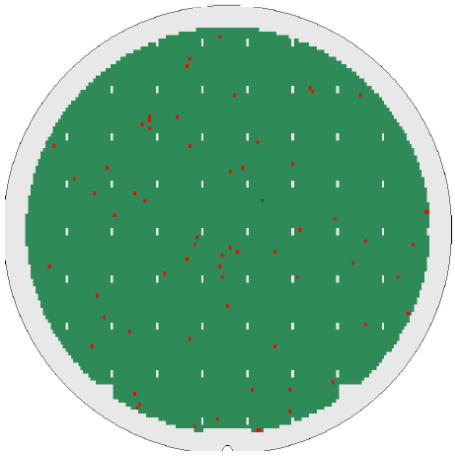

Fig. 11. Wafer map showing a typical production test result for the active interposer with SoC integrated sensor and IC as well as TSV, backside redistribution layer, and bumps as shown in Fig.2 (left). Red dots show failing sites. Overall yield is > 99.5% for a chip size of ~2mm^2.

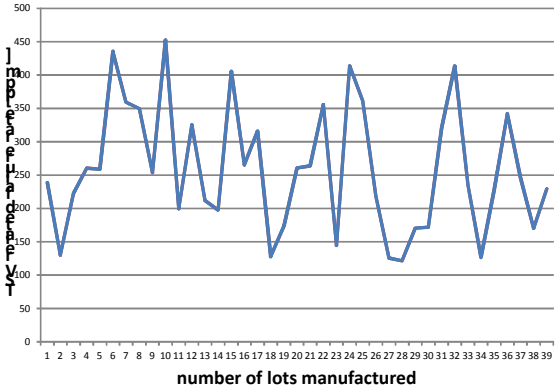

Fig. 12. Typical TSV related failure rate for mass production.

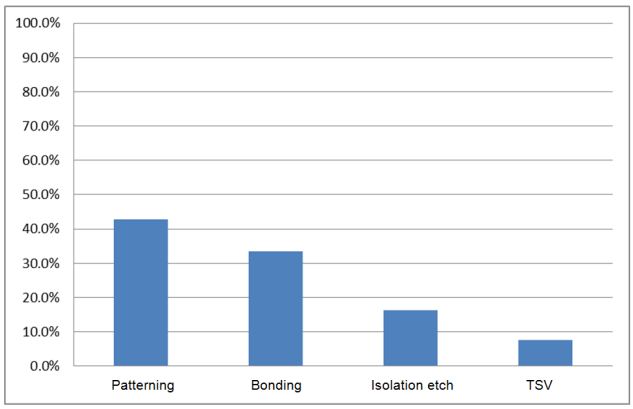

Fig. 13. Yield Pareto distribution for the TSV related failures for the IC with a 3D integrated photodiode shown in Fig.2 (right). The chip size is ~100mm^2.

The typical TSV related failure rate was found to be between 100 and 400ppm (Fig.12). The yield Pareto distribution shows that 40% of these failures are still related to patterning of layers for open TSVs, followed by wafer bonding (~30%), isolation etching including etch residues (~15%), and TSV patterning and etching (~8%).

IV. CONCLUSION

Comprehensive reports on 3D IC manufacturing are still not available. This paper has presented manufacturing data for a 3D integration technology with open isolated TSVs with tungsten metallization. Manufacturing of 3D integrated ICs with photosensors was found to be possible at yield levels comparable to standard CMOS process yields. Key challenges for future work in addition to further process development include the development of non-destructive in-line parameter monitoring methods for layer thicknesses and defects within open TSVs, fusion bond strength characterization methods, and defect analysis within TSVs. Further yield learning will require specific improvements for patterning of layers deposited into open TSVs, TSV isolation spacer formation, wafer bonding, and TSV etching with special focus on defect reduction for any of these modules. Further studies and manufacturing data especially for alternative concepts such as Cu-liner TSVs, "filled TSVs", or for "via middle" integration are on demand.

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