NBTI in $Si_{0.55}Ge_{0.45}$ cladding *p*-FinFETs: porting the superior reliability from planar to 3D architectures

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***Abstract*—SiGe channel planar pMOSFETs have been recently shown to offer improved NBTI reliability, owing to reduced hole trapping into pre-existing oxide defects and reduced interface state generation. In this paper we report a broad set of experimental data of SiGe cladding *finFETs* with varying fin widths, and we show that the intrinsically superior NBTI reliability can be ported to 3D architectures of relevance for N10 and beyond. The underlying physical mechanisms are discussed and compared to planar technologies.**

I. Introduction

High mobility channels will be required for next CMOS technology nodes [1]. While strained Ge is the front runner for ultimate bulk hole mobility [2], SiGe channels offer easier integration on Si wafers, reduced lattice mismatch enabling the implementation of compressive channel strain without the need of Strain Relaxed Buffer (SRB) architectures [3], while they enable the use of a standard SiO_2/HfO_2 dielectric stack provided a thin Si passivation layer (cap) is epitaxially grown on the SiGe channel [4]. Alternatively, a $SiGeO_x$ interfacial layer (IL) can be obtained by direct oxidation of the channel (no cap), with minimal formation of Ge suboxides, detrimental for both the interface quality and the device reliability [5], thanks to the limited Ge fraction in the SiGe alloy.

Already in 2010 [6] we have observed that SiGe channel pMOSFETs offer drastically improved NBTI reliability, owing to chiefly reduced hole trapping into pre-existing oxide defects, and to reduced interface state generation. We have ascribed the former effect to a favorable energy misalignment of the SiGe channel valence band with respect to dielectric defect levels (Fig. 1), and the latter effect to a reduced availability of Si-H precursor defects [7]. The superior NBTI reliability has been later confirmed by other groups [8]–[10] proving it to be an intrinsic property of this material system. However, so far the reliability boost was thoroughly studied only on planar structures.

In this paper, we report about the NBTI reliability of SiGe cladding *p*-FinFETs [11], consisting of a thin $Si_{0.55}Ge_{0.45}$ channel layer epitaxially grown on Si fins (Fig. 2). Such architecture obviously poses concerns for fin pitch scaling, but it consitutes a practical test vehicle towards future SiGe core finFET integration, and it enables in-situ epi-growth of both the SiGe channel and a thin Si cap. The encouraging results obtained in this simplified test vehicle and reported here suggest that the reliability improvement of SiGe *p*MOS technology can be ported from planar to 3D architectures of relevance for N10 and beyond [12].

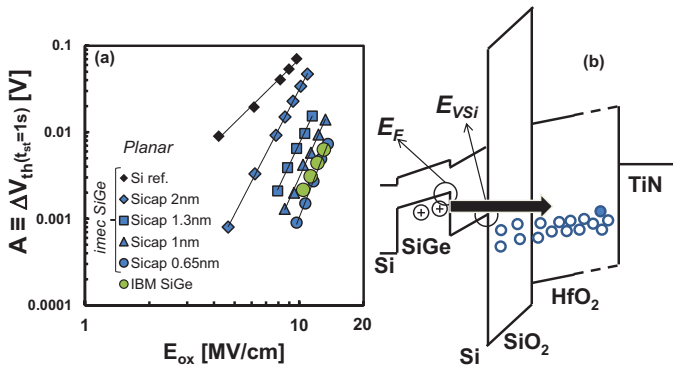

Fig. 1. **(a)** NBTI-induced ΔV_{th} in planar Si reference and SiGe channel pMOS [7]. Both a reduced NBTI and a steeper voltage acceleration have been observed in SiGe (imec and IBM [8], [9] data), and ascribed to **(b)** a reduced interaction with oxide defects thanks to a favorable energy alignment [7].

II. Experimental

NBTI degradation kinetics was studied in $Si_{0.55}Ge_{0.45}$ cladding finFETs and compared with Si reference finFETs with identical gate stack consisting of a chemically formed IL (imec clean [13]), ALD HfO_2 high-k (∼1.8nm) and a TiN metal gate. The CET in inversion of the fabricated gate stack was ∼1.6nm. Structures with varying fin width (W_{fin}, in the range 250 - 20 nm) were used to compare *planar-like* behavior to *sidewall-dominated* conduction. SiGe devices *with*

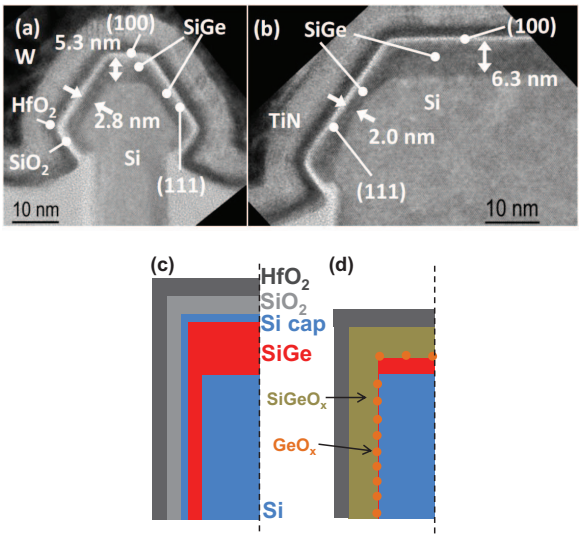

Fig. 2. TEM micrographs of SiGe cladding fins with Si cap, nominal fin width **(a)** 20nm, **(b)** 130nm. Notice the thinner SiGe on the sidewalls. **(c)** Idealized gate stack sketch for SiGe cladding finFET *w/* and **(d)** *w/o* Si cap. In the latter case, the direct oxidation of the SiGe channel might induce the formation of detrimental Ge suboxides, limited by the relatively low Ge fraction in the SiGe channel.

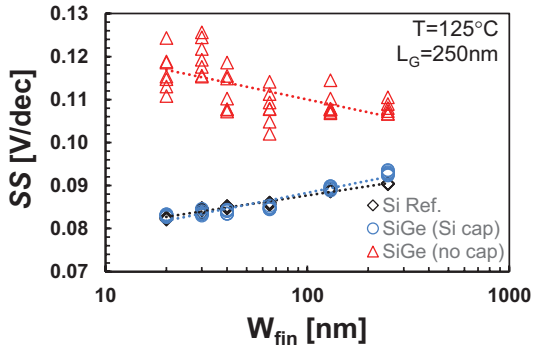

Fig. 3. Subthreshold swing vs. W$_{fin}$. Si cap passivation yields optimal, Si-like interface quality; note the improved electrostatics for narrowing W$_{fin}$. Direct oxidation of SiGe (no cap) yields degraded interface due to GeO$_x$ formation, particularly on sidewalls (narrow W$_{fin}$) where the thinner SiGe might be fully oxidized.

and *without* Si cap were considered: while the former approach yields optimal, *Si-like* interface quality, the latter approach offers reduced fabrication complexity at the cost of degraded interface quality. This is illustrated in Fig. 3: the SiGe devices *w/* Si cap showed a steep subthreshold slope (*SS*), comparable with the Si reference devices at all W_{fin}, while the SiGe devices *w/o* Si cap showed degraded *SS* ascribed to higher interface state density. Moreover, in Si and SiGe devices *w/* Si cap, a steeper *SS* is observed at narrow W_{fin} thanks to the improved gate electrostatics control proper of the finFET architecture. On the contrary, for SiGe devices *w/o* Si cap, a degraded *SS* was observed at narrow W_{fin}. The TEM picture revealed a thinner SiGe layer deposited on the sidewalls (cf. Fig. 2): when a Si cap is not deposited, the exposed thin SiGe layer on the sidewalls might be completely oxidized during IL formation, with enhanced formation of detrimental Ge suboxides. This can explain the degraded interface quality and *SS* at narrow W_{fin} (cf. Fig. 3, triangles).

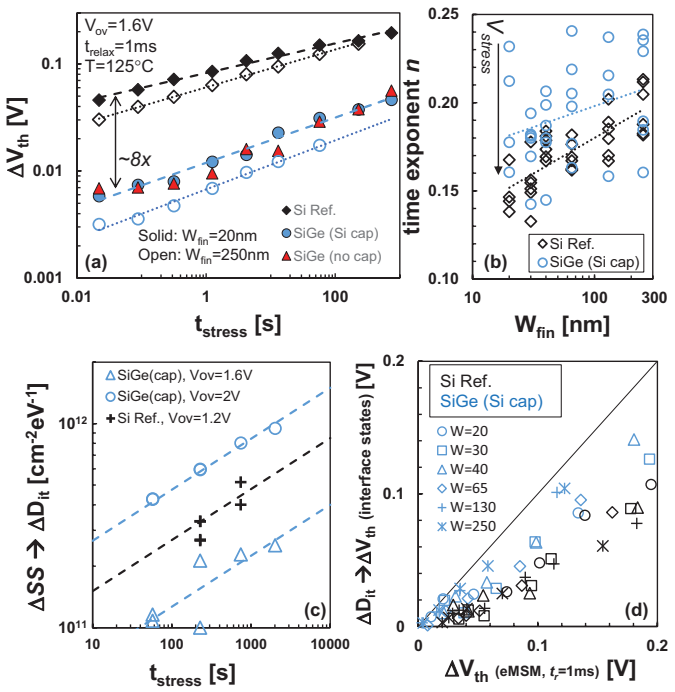

Fig. 4. **(a)** ΔV_{th} vs. t_{stress} measured at V_{ov}=1.6V in Si Ref., SiGe with Si cap and SiGe without Si cap finFETs; similar time evolution are observed for narrowest (20nm, solid symbols) and widest (250nm, i.e., planar-like, open symbols) fins. A significantly reduced NBTI is observed in SiGe devices (note: below the 1mV measurement resolution for planar-like SiGe *w/o* Si cap, cf. Figs. 5,6). **(b)** NBTI time exponents for varying W_{fin} and stress voltages on Si and SiGe. **(c)** Interface state generation monitored by subthreshold swing degradation: the same time dependence ($n_{N_{it}} \sim 0.25$) is observed for Si and SiGe. **(d)** Correlation plot of the total ΔV_{th} measured with the eMSM technique (1m*s* delay) and the ΔV_{th} induced by interface state generation (various stress times and voltages). A larger contribution of the latter component to the total degradation is observed in SiGe due to the significantly reduced trapping component [cf. Fig. 1 (b), and Fig. 5].

Structures made of 5 parallel fins were used to avoid stochastic NBTI degradation in nanoscale devices [14]. All the stress experiments were performed at 125°C. The extended Measure-Stress-Measure (eMSM, [15]) was used to capture NBTI-induced threshold voltage shift (ΔV_{th}) within 1m*s* delay from stress removal. Additionally, interface state generation (ΔD_{it}) was assessed by monitoring the subthreshold swing degradation (ΔSS) in a dedicated set of stress measurements with increasing duration, exploiting the relation [16]:

$$\Delta D_{it} = \frac{\Delta SS \times C_{ox}}{ln(10)k_BT} \quad . \tag{1}$$

III. Results and Discussion

In this Section we first review the general NBTI trends observed in Si and SiGe cladding finFETs. We show that SiGe channel *p*-finFETs offer consistently superior reliability as compared to Si, at all fin widths here considered (Subsection A). We then discuss in details fin width dependences observed in SiGe devices and not present in their Si counterparts (Subsection B). With a careful analysis of the experimental data we show that these dependences are extrinsic effects related to the integration of the test vehicle here used (i.e., cladding of a Si fin with a thin SiGe layer), and therefore are

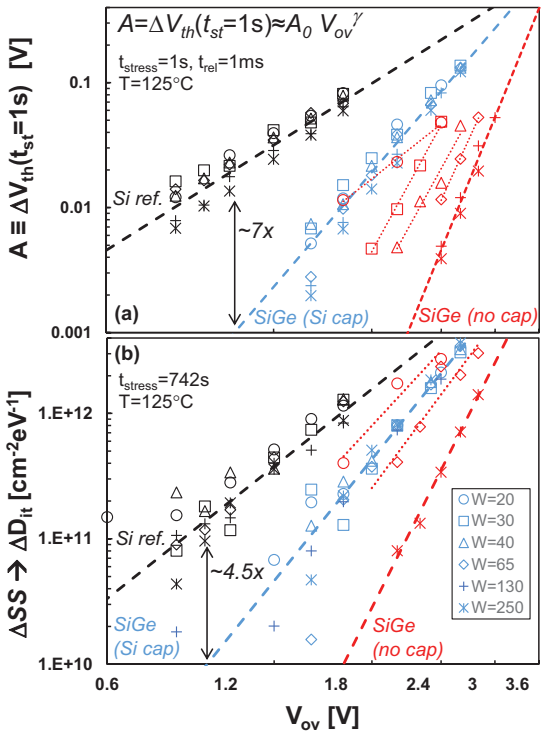

Fig. 5. **(a)** Voltage dependence of ΔV_{th}: SiGe finFETs *w/* Si cap show a significant NBTI reduction and a steeper voltage dependence as compared to Si reference devices, irrespective of the fin width, and consistently with planar data [cf. Fig. 1 (a)]. SiGe devices *w/o* Si cap show further improved NBTI at large W_{fin}; the improvement is partially lost at narrow W_{fin} due to insufficient SiGe coverage of the sidewalls (cf. Figs. 2, 8). **(b)** Similar observations apply to the interface generation component. Note SiGe channels show a larger reduction of the total ΔV_{th} ($\sim$ 7×) as compared to the ΔD_{it} reduction ($\sim$ 4.5×), related to the reduced underlying hole trapping component, consistently with planar device studies [7].

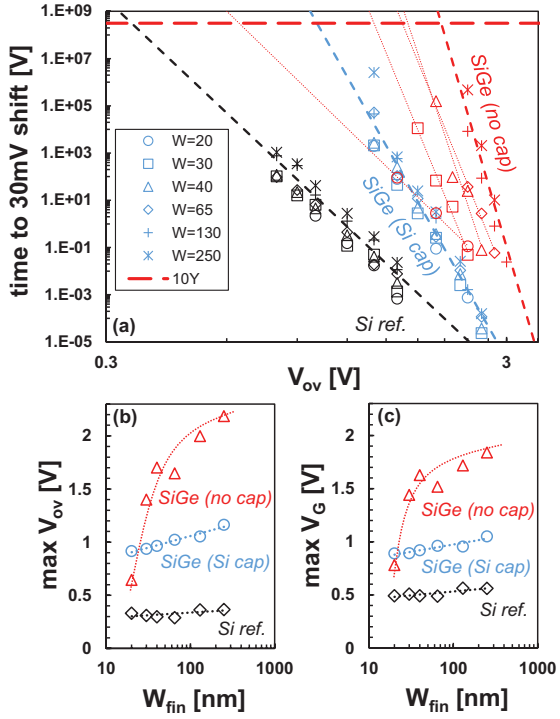

Fig. 6. **(a)** Extrapolated times to failure (defined as ΔV_{th}=30mV) for Si, SiGe *w/* and *w/o* Si cap finFETs of varying W_{fin}. SiGe devices can be operated reliably for 10 years at 125°C with larger **(b)** overdrive voltage, or **(c)** gate voltage [note: SiGe devices have lower $|V_{th0}|$ as compared to Si, cf. Fig. 8 (a)]. At narrow W_{fin} the reliability improvement is slightly reduced for SiGe *w/* Si cap due to quantization effects in thinner sidewall channel [cf. Fig. 7 (c)], while the improvement is almost completely lost for SiGe *w/o* Si cap due to insufficient sidewall coverage (fully oxidized SiGe, cf. Fig. 8). Both effects are related to fin cladding integration and are expected not to constitute showstoppers for future SiGe core finFETs.

not expected to impede the reliability optimization of future SiGe core finFETs at scaled fin widths.

A. Superior NBTI reliability

Fig. 4 (a) shows the ΔV_{th} measured by the eMSM technique during NBTI stress, following typical apparent power law dependence of the stress time:

$$\Delta V_{th} = A_0 \times V_{ov}^{\gamma} \times t_{stress}^{n} \quad . \tag{2}$$

Similar to planar devices, a significantly reduced ΔV_{th} is observed in SiGe devices, irrespective of W_{fin}. The time exponent n ranges between 0.14 and 0.24 (note: fixed t_{relax}=1m*s*), with slightly larger values for SiGe as compared to Si [Fig. 4 (b)]. On the contrary, the ΔD_{it} shows similar time evolution in SiGe and Si devices [Fig. 4 (c), $n_{N_{it}} \sim 0.25$), suggesting that the same bond breaking process at the Si/SiO_2 interface, i.e., the de-passivation of H-passivated Si dangling bonds (Pb_0), takes place also in SiGe devices as we previously argued for planar devices [17]. However, due to the reduced hole trapping component in SiGe devices, ΔD_{it} contributes a larger fraction of the total NBTI shift [Fig. 4 (d)], explaining the slightly steeper time dependence [18] observed in the eMSM measurements [see Fig. 4 (b)].

The drastically reduced overall degradation in SiGe finFETs ($\sim$ 7×) consistently correlates with a steeper NBTI voltage dependence as compared to Si reference devices [Fig. 5 (a)], previously ascribed to the energy decoupling between channel holes and oxide defect levels [7]: at low operating voltages of relevance for N10 and beyond, a very limited fraction of oxide defect levels appear to be energetically favorable for hole trapping. SiGe *w/o* Si cap show further improved NBTI at large W_{fin}: as in planar devices [7], without a Si cap the energy decoupling between channel holes and oxide defect levels is maximized [i.e., no spill-over of holes and no voltage drop onto the Si cap, cf. Fig. 1 (b)]. Nevertheless, the improvement is partially lost at narrow W_{fin}: as shown in the next Section, this is an extrinsic effect due to the insufficient SiGe coverage of the sidewalls (cf. Figs. 2, 8), yielding a parasitic Si fin sidewall conduction and the relatively poor NBTI reliability proper of Si channel devices.

Similar observations apply to the ΔD_{it} component [Fig.5 (b)]. We note that the larger reduction of the total ΔV_{th} [Fig. 5 (a)] as compared to the ΔD_{it} reduction [$\sim$ 4.5×, Fig. 5 (b)], confirms a significant reduction of the underlying hole trapping component. As a result, SiGe channel finFETs offer a longer device time-to-failure as compared to Si counterparts [Fig. 6 (a)], or alternatively a 10 year reliable operation at higher operating overdrive [Fig. 6 (b)] or V_{DD} [Fig. 6 (c)], of relevance for high performance application.

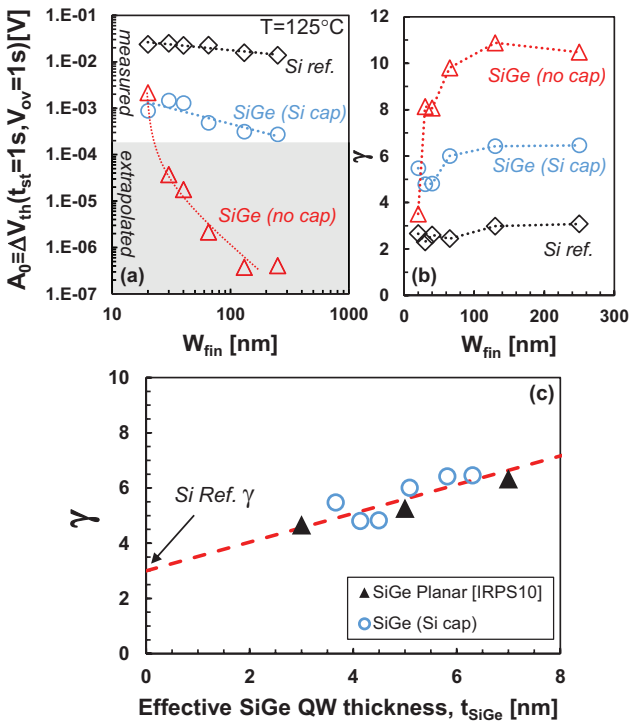

Fig. 7. **(a)** NBTI-induced ΔV_{th} at constant stress condition (V_{ov}=1V, t_{st}=1s, T=125°C) for Si, SiGe *w/* and *w/o* Si cap, as a function of W_{fin}. While NBTI is almost independent of the fin width in Si devices, an inverse W_{fin} dependence is observed in SiGe devices, correlated with **(b)** a reduced voltage dependence exponent (γ). The weak W_{fin} dependence in SiGe fins *w/* Si cap is ascribed to **(c)** quantization enhancing hole trapping in thinner sidewall channels, quantitatively consistent with planar data for varying SiGe thicknesses. The stronger, extrinsic W_{fin} dependence in SiGe fins *w/o* Si cap is instead ascribed to fully-oxidized SiGe layer on sidewalls (cf. Fig. 8).

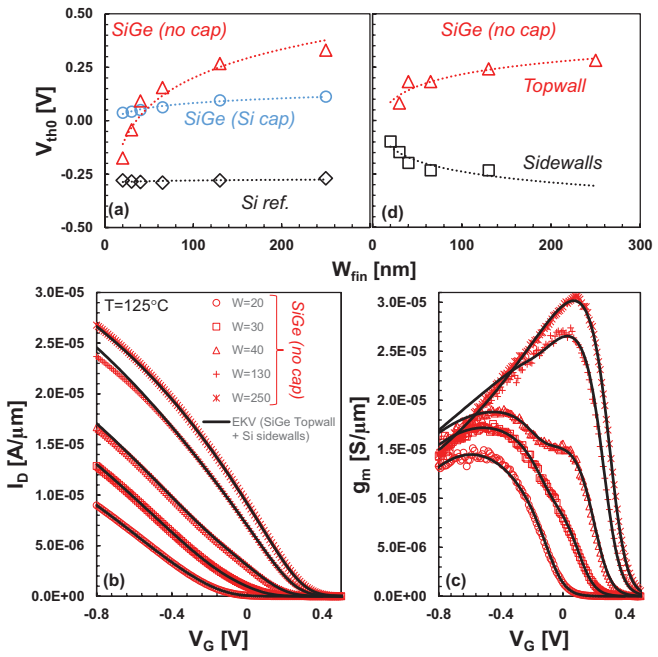

Fig. 8. **(a)** Fresh threshold voltage of Si, SiGe *w/* and *w/o* Si cap p-finFETs with varying W_{fin}. SiGe devices *w/o* Si cap show extrinsic V_{th0} roll-up (i.e., toward more negative values) at narrow W_{fin}, ascribed to the existence of a Si channel on the sidewalls due to full oxidation of the thin deposited SiGe layer. **(b)** Normalized $I_D - V_G$ curves confirm this observation: reduced drive is observed in narrow fins, while **(c)** transconductance curves clearly show a kink at intermediate W_{fin}, where the contribution of the SiGe channel topwall and of the Si channel sidewalls are comparable. EKV model [19] fitting of the curves unveils **(d)** the W_{fin} dependence of the threshold voltage of the two parallel channels.

B. Fin width dependences

A closer analysis of the NBTI power law parameters reveals that while for Si finFET similar power law prefactor [i.e., ΔV_{th} at fixed V_{ov} and stress time, see Eq. (2)] and voltage dependence exponent γ [Fig. 7 (a)-(b)] are observed for varying W_{fin}, SiGe devices show relatively larger shifts and lower γ in narrow fins. As discussed in Section II, a TEM analysis of the SiGe devices revealed a reduced SiGe channel thickness on the sidewalls as compared to the top wall: from previous planar studies, enhanced NBTI is expected in thinner SiGe quantum wells (QW) due to quantization effectively lowering the Fermi level in the channel, thus increasing the carrier-defect energy coupling [7]. Based on the TEM analysis, we calculated for every fin width an equivalent QW thickness as a weighted average of the sidewalls and topwall thicknesses, i.e.:

$$t_{SiGe} \approx \frac{2H_{fin}t_{SiGe}^{side} + W_{fin}t_{SiGe}^{top}}{2H_{fin} + W_{fin}} \quad , \qquad (3)$$

(Note: H_{fin}, t_{SiGe}^{top}, and t_{SiGe}^{side} were estimated from TEM picture to be ~20, ~7, ~2 nm, respectively). By replotting the γ values measured on fins of varying widths vs. the calculated equivalent SiGe QW thickness, the finFET data quantitatively match the SiGe planar data [Fig. 7 (c)]. This confirms that the slightly reduced NBTI reliability at narrow fins in SiGe devices *with* Si cap is not an intrinsic issue but an integration issue of the fin cladding approach here used.

The data for SiGe *w/o* Si cap instead revealed, on top of this gradual NBTI increase for decreasing W_{fin}, a sudden reliability loss for W_{fin} <40nm [Figs. 6 (b)-(c),7 (a)-(b)]. We hypothesize this to be due to the thinner SiGe layer deposited on the sidewalls being completely oxidized if a Si cap is not used, particularly because of faster oxidation rate of SiGe as compared to Si. This would imply the channel conduction on the topwall being through a SiGe channel, while it being through the inner Si fin on the sidewalls where the SiGe layer might be completely consumed. The hypothesis is confirmed by a careful study of the device $I_D - V_G$ curve as a function of W_{fin}. A steep roll-up of the device threshold voltage [V_{th0}, Fig. 8 (a)] is observed at narrow fins, with V_{th0} being similar to the Si reference for W_{fin}=20nm. While the topwall-dominated widest fins show *SiGe-like* V_{th0} and current drive, the sidewall-dominated narrowest fins show more negative V_{th0} and reduced drive [Fig. 8 (b)]. More interestingly the intermediate W_{fin} structure clearly shows a kink in the measured transconductance curve [Fig. 8 (c)], proving the existence of two parallel channels (i.e., *SiGe-like* on the topwall and *Si-like* on the sidewall). The $I_D - V_G$ and $g_m - V_G$ curves measured in devices with intermediate W_{fin} are perfectly reconstructed by a weighted combination of the sidewall and topwall conductions as described by EKV model [19] fitting of the widest and narrowest fins [Fig. 8 (b)-(c), lines]. By this de-embedding procedure it is possible to visualize the W_{fin}-dependence of the V_{th0} of the two parallel channels [Fig. 8 (d)]: the V_{th0} of the SiGe topwall

channel rolls-up for reducing W_{fin} due to quantization (i.e., effective bandgap widening), while the V_{th0} of the inner Si sidewall channel rolls-off in the narrow fins as expected for full depletion.

This careful analysis supports the conclusions that the sudden reliability loss at narrow fins in SiGe finFETs *w/o* Si cap is another extrinsic issue related to the used fin cladding approach: due to full oxidation of the thinner SiGe layer on the sidewalls, the conduction in narrow fin structures takes place in the inner parasitic Si channel, yielding *Si-like* V_{th0}, current drive, and (poorer) NBTI reliability. Due to its root cause, the reliability loss at narrow fin widths is expected to be readily solved in SiGe *core* fins of relevance for N10 and beyond.

IV. Conclusions

The broad set of experimental data of SiGe cladding finFETs here reported proves that the intrinsically superior NBTI reliability of SiGe channels can be ported to 3D architectures. Although some W_{fin}-dependence of NBTI has been observed, it has been proven to be completely related to integration issues (i.e., thinner SiGe on sidewalls, eventually fully consumed) of the preliminary test vehicle here used. These extrinsic issues are expected to be readily solved in SiGe *core* fins of relevance for real production.

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