

## A universal nonvolatile processing environment

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After decades of successful miniaturization, soaring investment costs and increasingly severe physical limits will bring CMOS scaling to a halt in the foreseeable future. Spintronics has attracted attention as a possible remedy, due to its non-volatility, high endurance, fast operation, and CMOS compatibility. New spintronic devices based on magnetic tunnel junctions (MTJs) utilizing all-electrical control, such as spin-torque (ST) transfer RAM and ST oscillators, have been successfully developed. However, the promising spintronic solutions with respect to speed and power consumption shown to date [1, 2] employed MTJs to store the information only, while the actual computation is still carried out via CMOS transistors.

We propose a universal nonvolatile processing environment, consisting of an ST majority gate (STMG) [3] and a nonvolatile magnetic flip-flop [4], see Fig. 1(a). The flip-flops are adjacent to the STMGs in an array and act as shared local buffers. We discuss a possible realization of an easily extendible 1-bit full adder consisting of just a single STMG and three non-volatile flip-flops.

A further essential building block in modern electronics is the oscillator. To date ST oscillators have required an external  $B$  field, limiting their practical implementation. We have demonstrated that the magnetic flip-flop structure provides an ST oscillator [5], with an improved design shown in Fig. 1(b) [6]. This high-frequency oscillator needs no external  $B$  field and complements the proposed nonvolatile processing environment. We discuss additional strategies to boost the maximum oscillator output power by using two three-layer in-plane MgO-MTJs.

The resulting nonvolatile processing environment has a highly regular structure, is computationally complete, and reduces information transport due to its shared buffers. Thus, it is viable as a universal post CMOS logic technology.

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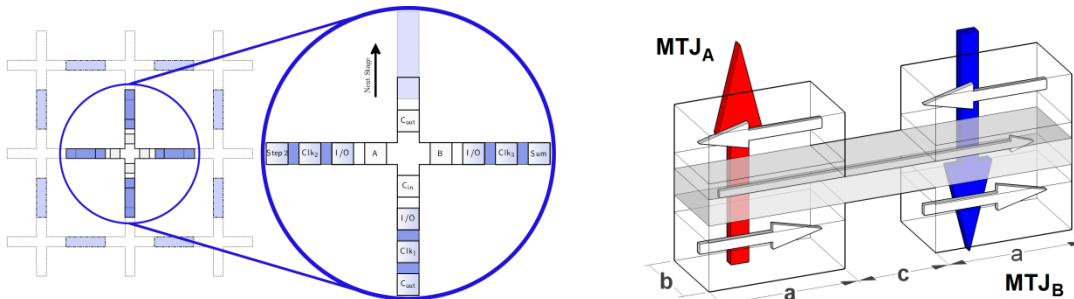


Fig. 1. (a) Spin torque majority gates (crosses) perform computation, while the nonvolatile flip-flops (rectangles) act as shared buffers. A single STMG and three flip-flops are sufficient to realize a concatenated 1-bit full adder; (b) Schematic illustration of a spin-torque oscillator based on two MTJs. The colored arrows indicate the direction of the current for each of the MTJs.

1. D. Chabi *et al.*, *IEEE Trans. Circ. Syst.* **61**, 1755 (2014).
2. W. Zhao *et al.*, *Proc. Great Lakes Symp. VLSI* (2011), p. 431.
3. D. E. Nikonov *et al.*, *Electron Dev. Lett.* **32**, 1128 (2011).
4. T. Windbacher *et al.*, WO 2014/154497 A1 (2014).
5. T. Windbacher *et al.*, *J. Appl. Phys.* **115**, 17C901 (2014).
6. A. Makarov *et al.*, *Proc. SSDM* (2013), p. 796.