Hot-Electron-Related Degradation in InAlN/GaN High-Electron-Mobility Transistors

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***Abstract*— Hot-electron temperature (T_e) in InAlN/GaN high-electron-mobility transistors (HEMTs) was determined using electroluminescence spectroscopy as a function of gate voltage and correlated with the T_e distribution determined by hydrodynamic simulations. Good agreement between measurement and simulations suggests that hot electrons can locally reach temperatures of up to 30 000 K at $V_{ds} = 30$ V, i.e., two to three times higher than that typically obtained for similar AlGaN/GaN HEMTs. The consequence of such high T_e in InAlN/GaN HEMTs is illustrated by electrical stressing in OFF and semi-ON state at $V_{gd} = 100$ V. Prominent channel degradation was observed for devices stressed in semi-ON state, suggesting hot-electron driven degradation. Threshold voltage and drain current transient analyses indicate that hot electrons increase the density of traps in the GaN channel underneath the gate as well as surface/interface traps located in the gate-to-drain access region.**

***Index Terms*— Electrical stress, electroluminescence (EL), hot electrons, hydrodynamic (HD) simulation, InAlN/GaN high-electron-mobility transistor (HEMT), reliability.**

I. Introduction

HIGH-electron-mobility transistors (HEMTs) based on InAlN/GaN heterostructures [1] represent an extremely promising technology for RF power devices for telecommunication and satellite applications [2]–[5]. InAlN/GaN HEMTs with record current gain cutoff frequency of 400 GHz have been demonstrated [6]. In addition, several promising concepts for normally off switching transistors for power converter applications have been proposed in [7] and [8]. The main advantage of InAlN/GaN HEMTs over those utilizing AlGaN/GaN heterostructure is in almost a three-time higher electron concentration in the channel. This is due to the higher spontaneous polarization at the heterointerface, even in the absence of the piezoelectric polarization component in these devices, in contrast to the piezoelectric polarization inherently present at AlGaN/GaN interface as a result of tensile strain in the AlGaN barrier layer. Although not fully clear up to date, the stress in the AlGaN layer is likely to enhance degradation of the AlGaN/GaN HEMTs, such as surface cracking [9], [10] and more often surface pitting, i.e., amorphous material inclusions into crystalline lattice [11]–[14] at the drain side of the gate edge upon high electrical field. As InAlN can be lattice matched on GaN, enhanced robustness against electromechanical-related degradation modes can be expected. No such degradation mode of InAlN/GaN devices has been reported so far. However, there are only few studies devoted to the analysis of degradation mechanisms in InAlN/GaN HEMTs [15]–[18]. In general, a pronounced degradation of channel resistance upon high-field electrical stressing has been reported and attributed to hot electron [15], [16] or hot-phonon effect [17]. Interestingly, Kuzmik *et al.* [16] predicted electron temperature (T_e) as high as 20 000 K in the transistor's channel; however, any experimental evidence for such high T_e is still missing.

In this paper, T_e in InAlN/GaN HEMTs' channel was experimentally measured using electroluminescence (EL) spectroscopy and analyzed in conjunction with hydrodynamic (HD) simulations. Our analysis indicates that hot electrons can locally reach T_e of 30 000 K. Therefore, InAlN/GaN HEMTs were stressed in OFF and semi-ON state at $V_{gd} = 100$ V and analyzed by means of electrical characterization. More pronounced degradation of HEMTs submitted to semi-ON state stress compared with OFF state suggests hot-electron driven degradation, which is discussed in relation to dehydrogenation of point defects in the GaN channel.

II. Experimental and Simulation Details

$In_{0.17}Al_{0.83}N$/AlN/GaN (13 nm/1 nm/1.2 μm) heterostructure with lattice-matched InAlN layer was grown by metal-organic chemical vapor deposition (MOCVD) on sapphire

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substrates. Hall measurements yielded an electron mobility of $\sim$560 $cm^2V^{-1}s^{-1}$ and a 2-D electron gas (2-DEG) density of $\sim 2.2 \times 10^{13}$ cm^{-2}. Lower 2-DEG mobility resulted from the application of the AlN seeding layer inserted between the sapphire substrate and GaN buffer. From our experience, the seeding layer ensured lower buffer leakage and higher breakdown voltage compared with InAlN/GaN heterostructures directly grown on the sapphire substrate, on the expense of lower mobility. After mesa etching and Ti/Al/Ni/Au ohmic contact formation, optical lithography was used to define 1.8 μm-long and 25 μm-wide rectangular-shaped Ni/Au Schottky gate contacts without field plate. Finally, the wafers were passivated by 10-nm-thick Al_2O_3 layer grown by MOCVD at 600 °C without any postdeposition treatment. Finalized devices showed threshold voltage ($V_{\rm th}$) and maximum drain current ($I_{d,\max}$) of -4.7 V and 0.7 A/mm, respectively.

EL spectroscopy was used to determine T_e from a high-energy tail of the EL spectrum as a function of $V_{\rm gs}$ at $V_{\rm ds} = 30$ V [19]–[21] using a Renishaw inVia spectrometer with a 50 × (NA = 0.5) objective from the top side of the wafer. All spectra were corrected with the system response function and only devices with negligible yellow luminescence contribution were considered [22], which, if present, could affect a fitting result. To analyze the measured T_e in more detail, the spatial distribution of T_e was also determined by the HD simulations performed with the 2-D device simulator Minimos-NT, which is well suited for numerical analysis of GaN HEMTs [23], [24]. The HD transport model is a four-moment energy transport model [25] and provides the best physics-based description of the problem at a reasonable computational cost. Keeping in mind intervalley scattering can notable affect T_e distribution, a two-valley approach has been employed to approximate intervalley transfer at high fields. Here, a weighted mean of mobility in the lowest Γ valley and higher U valleys (assuming six equivalent valleys) was built with transport parameters (mobility, energy relaxation times, etc.) extracted from own Monte Carlo simulations [24]. A system of six partial differential equations: Poisson, current continuity, energy balance for electrons and holes, and the lattice heat flow (to account for self-heating effects) equations, is solved self-consistently. These equations have material-specific parameters, such as the bandgap energy, electron mobility, thermal conductivity, and so on. The dependence of these parameters on temperature, carrier energy, and so on is described elsewhere [18]–[24]. InAlN/GaN HEMTs with 6-μm source-to-drain distance and the gate placed symmetrically between source and drain were used for the EL measurements and simulations. For comparison, EL spectra were also measured on commercial AlGaN/GaN HEMTs with 30-nm-thick $Al_{0.3}Ga_{0.7}N$ layer and 1.8-μm-thick GaN buffer grown on SiC substrate and similar geometry (6-μm source-to-drain distance and 3-μm gate-to-drain distance) operated at $V_{\rm gs} = 0$ V and $V_{\rm ds} = 30$ V. Finally, the channel temperature was investigated by micro-Raman thermography [26] with 488-nm laser excitation source.

HEMTs with 12-μm source-to-drain distance (3.1-μm source-to-gate and 7.1-μm gate-to-drain distance) were subjected to OFF and semi-ON state stress with $V_{\rm gs} = -7$ and -3 V, respectively, for 10 h at room temperature. Note that, within the experimental error, similar values of T_e were determined for devices with 6- and 12-μm source-to-drain opening for the same conditions. It came from the simulations that both devices exhibit almost similar electric field and thus T_e distribution. A number of devices were stressed at $V_{\rm gd} = 50$, 75, and 100 V. However, only negligible permanent changes were observed for the devices stressed at $V_{\rm gd} < 100$ V. Therefore, only the results of the representative devices stressed at $V_{\rm gd} = 100$ V are presented in the following (I_d during semi-ON state stress was about 160 mA/mm). Output and transfer characteristics in dc and pulsed mode (gate voltage was pulsed from quiescent bias of -5 V to a desired value with 100-ns-long pulse with 0.1% duty cycle, while $V_{\rm ds}$ was dc biased) together with total resistance and end resistance measurements [16], [27] to determine the intrinsic channel resistance ($R_{\rm CH}$), and source (R_S) and drain (R_D) resistances, respectively, were used to characterize the devices. Measurements were performed before and one week after the stress, to assess the permanent device degradation. $R_{\rm CH}$ was obtained from the slope of the total resistance (R_T) measured with varying $V_{\rm gs}$ at $V_{\rm ds} = 0.2$ V. The R_S and R_D were then determined separately from the end resistance data as $R_{S(D)} = R_{S(D)}^{\rm end} - R_{\rm CH}/2$.

To assess stress-induced trap generation in the devices, I_d transient analysis similar to [20] and [28] was performed on the fresh and stressed HEMTs at different temperatures. Here, I_d transients were measured in the logarithmic scale at $V_{\rm gs} = 1$ V and $V_{\rm ds} = 0.5$ V after applying a filling pulse with $V_{{\rm gs},F} = -5$ V and $V_{{\rm ds},F}$ in the range 0–20 V. The measured I_d transients were fitted with a function given by a sum of 15 exponentials of the form $A_i \exp(-t/\tau_i)$, where t denotes time, τ_i-S are the time constants logarithmically divided along the measurement time, and A_i-S are the corresponding pre-exponential factors for $i = 1, \ldots, 15$. The fitted transients were then numerically derivated according to $\log_{10} t$ to visualize the peaks with position giving the characteristic trap time constant and amplitude related to relative trap density. For analyzing bulk traps underneath the gate only, $V_{\rm th}$-transient technique similar to [29] and [30] was applied to the gate contacts of the stressed devices. In this technique, $V_{\rm th}$ transients given as $\Delta V_{\rm th} = V_{\rm th}(t = 0) - V_{\rm th}(t)$ were determined from the capacitance transients measured in a two-terminal configuration (source and drain contacts grounded) at $V_g = -5$ V after a filling pulse of $V_{g,F} = 0$ V application. The $V_{\rm th}$ transients measured at different temperatures were analyzed in the same way as those of I_d transients.

III. Results and Discussion

A. Electron Temperature Determination

Fig. 1 shows the EL spectra measured on the InAlN/GaN HEMT for different $V_{\rm gs}$ at the drain side of the gate in the middle of the transistor's finger (see the inset of Fig. 1). The spectra show a typical Maxwellian distribution [19]–[21], consistent with intraband radiative electron

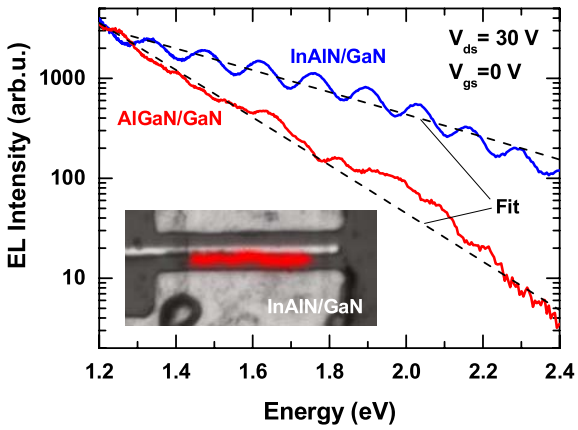

Fig. 1. EL spectra of InAlN/GaN and reference AlGaN/GaN HEMTs operated at $V_{ds} = 30$ V and $V_{gs} = 0$ V. The oscillations in the spectra are related to Fabry–Perot interference fringes and therefore artifacts. Inset shows the overlap of optical and EL image of InAlN/GaN HEMT taken at $V_{ds} = 30$ V and $V_{gs} = 0$ V.

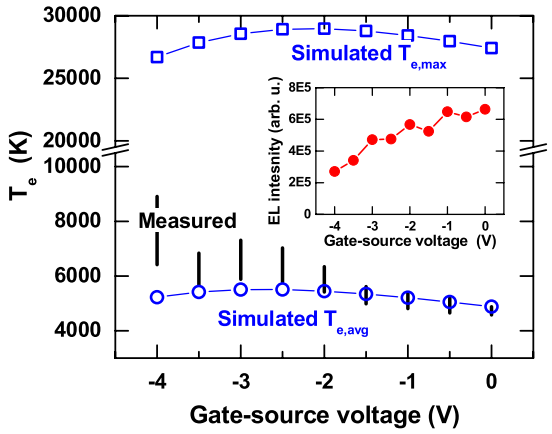

Fig. 2. Comparison between measured and simulated $T_e - S$ as a function of V_{gs} obtained at $V_{ds} = 30$ V. The vertical bars represent T_e determined from linear fits to the experimental data in the range of 1.2–2.4 and 1.4–2.2 eV. The data calculated using HD simulations (at the same bias conditions) are presented in a form of maximum ($T_{e,max}$) and averaged ($T_{e,avg}$) values. $T_{e,max}$ represents a peak value of the T_e distribution extracted along the channel at a distance of 30 nm below the quantum well, while $T_{e,avg}$ should correspond to the measured T_e (see the text and Fig. 3). Inset shows the EL intensity as a function of V_{gs}.

transition [31]. The EL spectra can be thus interpreted using Maxwell–Boltzmann distribution in a form

$$\mathrm{EL} \sim \left[k_B(T_e - T_{\mathrm{lat}})\right]^{3/2} E^{1/2} \exp\left[-\frac{E}{k_B(T_e - T_{\mathrm{lat}})}\right] \quad (1)$$

where E is the photon energy, T_{lat} is the lattice temperature (determined by the Raman thermography), and k_B is Boltzmann's constant. It has been pointed out that the complexity of the light emission process in Si-based devices results in more complex relation between hot-electron distribution and photon energy distribution (i.e., EL spectrum) [32]. However, as the mechanism of EL in GaN-based devices is still under debate, hot-carrier energy distribution was assumed to correspond to that of photons.

T_e as a function of V_{gs} determined using (1) by fitting to the experimental data in the energy range of 1.2–2.4 eV (low values) and 1.4–2.2 eV (high values) is shown in Fig. 2 by vertical bars, illustrating the confidence band of the fitting.

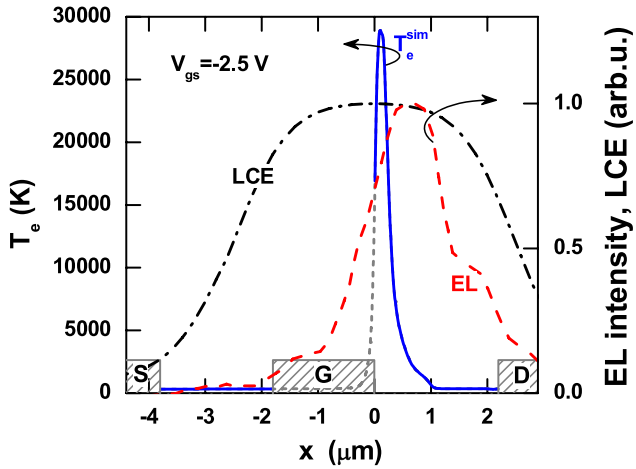

Fig. 3. Illustration of spatial averaging of the simulated T_e distribution (solid line, extracted along the channel at a distance of 30 nm below the quantum well). In the averaging, the product of the spectrometer LCE (dash-dotted line) and the measured EL intensity profile (dashed line) was used as a weighting function. Gate shadowing was considering by excluding T_e values laid underneath the gate (dashed area) from the averaging (short dashed line).

As the first approximation, the observed Fabry–Perot oscillation was neglected for the fitting procedure, since the signal spreads evenly across spectrum, assuming negligible impact on extracted T_e. The inset shows the corresponding EL intensity as a function of the gate bias. The experimentally measured T_e increases from ~4700 to ~8000 K with decreasing V_{gs}. This is due to electric field increasing with increasing V_{gd}, while the total EL intensity decreases as the channel is pinched off with decreasing V_{gs}. For comparison, AlGaN/GaN HEMT operated at $V_{ds} = 30$ V and $V_{gs} = 0$ V yielded T_e of ~2600 K, i.e., nearly two-fold lower value compared with InAlN/GaN HEMTs. A higher T_e in the InAlN/GaN HEMTs compared with AlGaN/GaN counterparts can be understood as a result of higher polarization field (giving higher 2-DEG concentration) and thinner barrier layer for the former [1], resulting in higher vertical electric field necessary to control the channel [16]. Therefore, upon semi-ON or OFF state operation, a number of channel electrons are deflected toward the buffer with considerable higher energy.

As optical spectroscopy has a finite spatial resolution, the T_e values extracted from the EL spectra represent electron energy averaged over relatively large area of the GaN channel. A higher T_e can therefore be expected in the highly localized electric field peak. To analyze this in more detail, HD simulations of T_e and T_{lat} were performed for the devices analyzed here, and the summary of the results is given in Fig. 2. Interestingly, for InAlN/GaN HEMTs, maximum T_e increases from ~27 000 to ~29 000 K with V_{gs} decreasing from 0 to −2.5 V, and then it decreases to ~27 000 K for $V_{gs} = -4$ V. The maximum T_e values are significantly higher than those measured by EL due to the spatial averaging in the measurement. It was found from the simulation data that, due to monotonic increase of the electric field with V_{gd}, electron velocity decreases. Electron energy, being proportional to the product of electric field and electron velocity, then results in the bell-shaped electron temperature as a function of V_{gs}. This trend is in line with the Monte Carlo simulations of hot

electrons in AlGaN/GaN HEMTs [33], where a larger portion of electrons exceeded energies of 2.5 eV in device operated in semi-ON state compared with OFF state. The maximum T_e for the reference AlGaN/GaN HEMT at $V_{gs} = 0$ V was found to be 11 400 K (not shown). We note that our 2-D simulations did not account for the virtual gate effect that can mitigate electric field peak at the gate edge. However, in the steady-state saturation regime of the device reached during the EL measurements, most of trapping states located in the gate-to-drain access region can be expected to be detrapped, thus having less important impact on the resulting T_e.

To test the validity of the simulation, we considered the spatial averaging in the T_e measurement compared with very narrow distribution of hot electrons [full-width at half-maximum (FWHM) ~250 nm] from simulations. In addition, part of the light emission is screened by the gate contact, which needs to be considered as well. To quantitatively account for these effects, the simulated T_e profiles were averaged in the access region parts of the transistor (top-view measurements) with a weighting function given by the product of normalized light collection efficiency (LCE) of the spectrometer and EL intensity profile measured at a given V_{gs}, as shown in Fig. 3 for $V_{gs} = -2.5$ V. LCE was determined from the convolution between charge-coupled device image area (five pixels corresponding to ~5.3 μm) and the optical resolution (given by Voigt distribution with FWHM ~0.6 μm). Such weighting function considers both the actual spatial distribution of the emitted light together with the collection efficiency of the spectrometer. The averaged T_e values are shown in Fig. 2, and a very good agreement between the measured values and those obtained from the simulations can be inferred, in particular, when the EL signal was large and error bars therefore small. Discrepancy between the experimental and simulated data obtained for $V_{gs} = -4$ V can be understood as a consequence of the simplifications introduced in the model mentioned above, neglected hot electrons injected from the gate, and lower light intensity at low-current levels resulting into a larger error in the measurement, as illustrated by the vertical bars in Fig. 2. The averaging of the simulated T_e distribution for AlGaN/GaN HEMT resulted in a value of 2300 K (not shown), i.e., similar to the experimental value (2600 K).

Regarding the extracted T_e from EL measurements, to our knowledge, there are no experimental data reported in the literature for InAlN/GaN HEMTs, in contrast to the many results for AlGaN/GaN devices. Shigekawa *et al.* [19] extracted T_e of 2000–2400 K at $V_{gd} = 30$ V, while in [21]–[34] and [35], similar T_e of 1700 K was reported at $V_{gd} = 40$, 28.5, and 10 V, respectively. A substantially higher T_e of 5000 K at $V_{gd} = 30$ V was determined in [20] from backside wafer EL measurement, thus without gate shadowing. Measurement performed here on the commercial AlGaN/GaN HEMTs yielded T_e of 2600 K at $V_{gd} = 30$ V, agreeing reasonably well with those measured by EL collected from the top side [19], [21], [34], [35]. As T_e determined here for InAlN/GaN HEMTs is two to three times higher compared with that for AlGaN/GaN devices, hot-electron degradation can be expected to be the major concern for InAlN/GaN devices. The analysis suggests that T_e as high as 30 000 K can be locally reached at $V_{gd} = 33$ V, corresponding to electron energy similar to 2.6 eV.

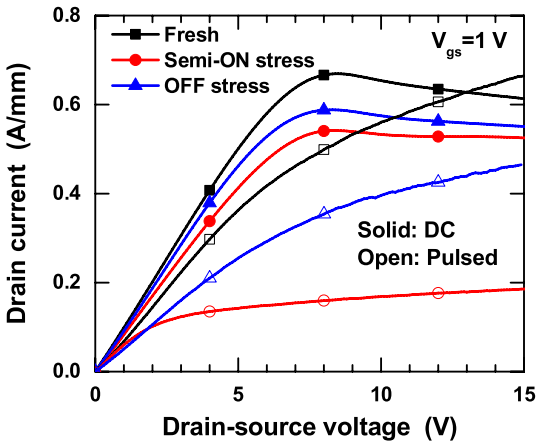

Fig. 4. Output characteristics of InAlN/GaN HEMTs measured in dc (solid symbols) and pulsed (open symbols) mode before and one week after OFF and semi-ON state stress performed at $V_{gd} = 100$ V. For clarity, only characteristics for $V_{gs} = 1$ V are shown. For pulsed measurements, gate voltage was pulsed for 100 ns from quiescent bias of -5 V while the drain was dc biased.

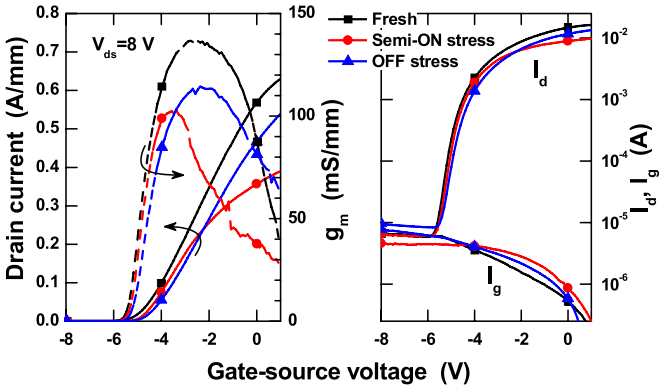

Fig. 5. DC transfer (solid lines) and transconductance (dashed lines) characteristics of InAlN/GaN HEMTs in linear (left) and semilog (right) scale, measured at $V_{ds} = 8$ V before and one week after OFF and semi-ON state stress. Note negligible increase in the gate leakage (left) after stressing in both bias conditions.

B. Electrical Stressing

Fig. 4 shows the output characteristics measured in dc and pulsed mode before and after OFF and semi-ON state stress. Regarding the dc measurements, maximum I_d decreased by about 14% and 19% after OFF and semi-ON state stressing, respectively. Stronger degradation after semi-ON state stressing was observed also for static ON state resistance (R_{ON}, determined from the linear part of the output characteristics), where R_{ON} decreased by about 9% and 12% after stressing in OFF and semi-ON state stressing, respectively. Output characteristics measured in the pulsed mode also shown in Fig. 5 suggest strongest degradation after semi-ON state stressing, indicating trap generation in the intrinsic region of the transistor [36].

The transfer characteristics before and after stressing are shown in Fig. 5. Much stronger degradation in the

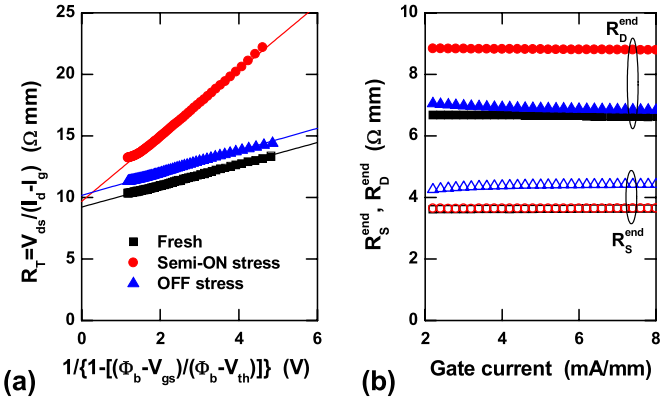

Fig. 6. (a) Separation of the channel resistance R_{CH} and the access resistances $R_S + R_D$, proportional to the slope and intercept of the linear fit to the data, respectively. (b) Direct measurement of the source and drain end resistances as a function of gate current, performed before and one week after OFF and semi-ON state stressing.

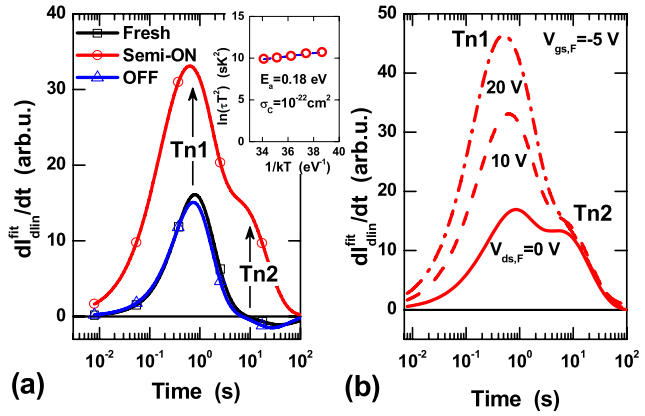

Fig. 7. (a) Analysis of the I_d transients measured on InAlN/GaN HEMTs at room temperature before and one week after OFF and semi-ON state stressing, showing dominant peak labeled as Tn1 with activation energy of 0.18 eV (inset, $T = 25$–65 °C). A new peak labeled as Tn2 became apparent for semi-ON stressed device only. (b) Analysis of the I_d transients measured on the device stressed in semi-ON state with different V_{ds} applied during the filling pulse ($V_{ds,F}$) and keeping $V_{gs,F} = -5$ V. While Tn1 amplitude strongly increases with $V_{ds,F}$ increase, Tn2 amplitude remains invariant of $V_{ds,F}$.

TABLE I
SUMMARY OF THE ELECTRICAL PARAMETERS OF INALN/GAN HEMTS BEFORE AND AFTER OFF AND SEMI-ON STATE STRESS

Parameter	Fresh	OFF stress	Semi-ON stress
R_{CH} (Ωmm)	0.8	0.9	2.7
R_S (Ωmm)	3.2	4.0	2.3
R_D (Ωmm)	6.2	6.2	7.5
R_{ON} (Ωmm)[a]	10.3	11.2	12.1
V_{th} (V)	-4.7	-4.4	-4.7
$I_{d,max}$ (A/mm)[b]	0.67	0.58	0.54

[a]Determined from the linear part of the output characteristics.
[a]Extracted at V_{ds}=8 V and V_{gs}=1 V.

transconductance (g_m) took place after stressing in semi-ON state compared with OFF state; as apart from the maximum value degradation, a strong decrease in g_m for higher V_{gs} was observed. In contrast, a similar trend of g_m dependence on V_{gs} can be inferred from Fig. 5 for fresh and OFF-state stressed devices. On the other hand, a notable V_{th} shift from -4.7 to -4.4 V took place only for devices stressed in the OFF state, while it remained the same after semi-ON stressing. As apparent from the semilog plot of the transfer and input characteristics, the gate leakage current (I_g) did not degrade for neither of the here considered stress conditions. These results suggest a stronger degradation of HEMTs stressed in semi-ON state. Moreover, the difference in $g_m - V_{gs}$ trend and V_{th} shift suggest distinct differences in the degradation mechanisms for HEMTs submitted to OFF and semi-ON state stressing. Note the slightly lower saturation I_d measured by the transfer characteristic compared with that from the output characteristic for HEMT stressed in semi-ON state. This can be attributed to increased trapping in the device after the stressing.

To analyze the location of the degradation, R_{CH}, R_S, and R_D were measured before and after stress, as shown in Fig. 6. The results are summarized in Table I together with V_{th}, maximum I_d, and R_{ON}. A good agreement between $R_S + R_{CH} + R_D$ and R_{ON} determined independently can be inferred from Table I, validating the performed analysis. R_{CH} was found to increase significantly from 0.8 for fresh device to 2.7 Ω mm (by more than 200%) after semi-ON stressing. This was accompanied with a slight increase in R_D (by 30%) and slight decrease in R_S. However, decrease in R_S could be an artifact originated from the R_{CH} extraction, e.g., stronger degradation of the intrinsic region close to the drain side would lead to R_S underestimation. In contrast, only negligible change in R_{CH} took place for OFF state stress, and slight increase in R_S from 3.2 for fresh device to 4 Ω mm for stressed device was observed, while R_D remained unchanged after OFF state stressing.

To correlate intrinsic and access resistances degradation with stress-induced trap generation, I_d and V_{th} transients were measured and analyzed on fresh and stressed devices. Fig. 7(a) shows the analysis of I_d transients of fresh and stressed HEMTs measured at room temperature. In all devices, a dominant electron-like detrapping process with time constant (τ) of ~800 ms can be inferred from the analysis (labeled as Tn1 in the following). Almost the same trapping signature was determined for fresh and OFF state stressed device, suggesting negligible Tn1 trap generation. In contrast, semi-ON state stressing resulted in strong increase in Tn1 amplitude (by ~100%), suggesting increase in Tn1 trap density. In addition, a new electron-like detrapping process labeled as Tn2 became visible after semi-ON state stressing, manifesting itself as a shoulder of Tn1 with time constant similar to 10 s.

The activation energy (E_a) and capture cross section (σ_C) of Tn1 determined from the Arrhenius plot [see the inset of Fig. 8(a)] was found to be 0.18 eV and $\sim 10^{-22}$ cm^2, respectively, for all devices. Such small E_a and σ_C suggest that Tn1 does not represent a bulk trap emission process. Instead, it can be assigned to the electron emission from the surface/interface traps in the transistor access region, governed by the hopping process, as proposed in [37] and [38]. To support this interpretation, I_d transients of the device stressed in semi-ON state were measured after applying a filling pulse with $V_{ds,F} = 0$, 10, and 20 V ($V_{gs,F} = -5$ V), and the results are shown in Fig. 7(b). The amplitude of

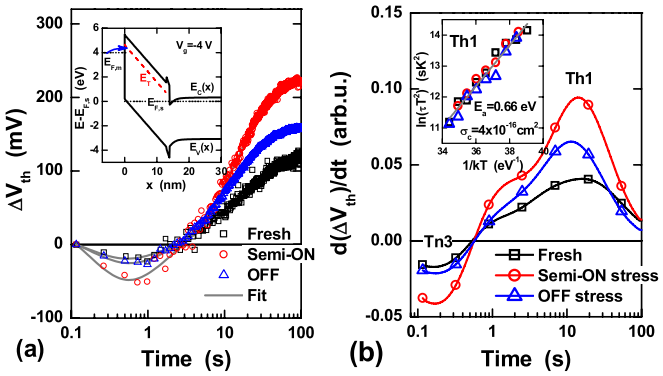

Fig. 8. (a) $V_{\rm th}$ transients measured on InAlN/GaN HEMTs at room temperature before and one week after OFF and semi-ON state stressing. (b) Corresponding analyses show similar dominant hole-like emission process (Th1) and electron-like emission process (Tn3) in devices before and after stressing, with stress-induced changes in the peak amplitudes. Inset of (a) depicts the interpretation of Th1 process as trapping of electrons in the InAlN barrier. Electrons are supposed to be injected from the gate via thermionic field emission. Arrhenius plot of the Th1 emission process [inset of (b), T = 25–65 °C] yielded the same E_a of 0.66 eV for fresh and stressed devices.

Tn1 was found to increase linearly with the $V_{{\rm ds},F}$ amplitude, i.e., increasing the lateral electric field during the trap filling. This behavior is consistent with hopping-driven emission from surface/interface traps located in the gate-to-drain region that are filled ever further away from the drain side of the gate edge with increasing $V_{{\rm ds},F}$. The data in Fig. 7(a) therefore indicate that semi-ON state stress results in increased density of pre-existing surface/interface traps located in the gate-to-drain access region. In contrast, generation of such traps is negligible during OFF-state stress. This is consistent with the R_D data (Table I) and, to some extent, also with pulsed output characteristics, as R_D was found to increase only after semi-ON stressing. Note that generation of faster traps (τ < 10 ms) during OFF-state stress can be attributed to some knee voltage walkout of the pulsed output characteristics (Fig. 4), while this effect was not observable by the I_d transient and end resistance measurements. Due to dominant Tn1 process, it was not possible to extract trap signature of Tn2 process, therefore it is not discussed in the following.

Unlike I_d transient, $V_{\rm th}$ transients are mostly sensitive to traps located underneath the gate, i.e., also those potentially affecting $R_{\rm CH}$ via mobility degradation. The $V_{\rm th}$ transients measured on fresh and stressed devices at 25 °C are shown in Fig. 8 together with the corresponding analyses. As can be inferred from Fig. 8(b), two emission processes were identified in all devices: 1) an electron-like detrapping process with τ of ∼100 ms labeled as Tn3 and 2) a broad hole-like emission process with τ centered at about 20 s labeled as Th1. While only negligible increase in Tn3 amplitude was observed after OFF state stressing, it increased significantly (by 150%) after semi-ON state stressing. The amplitude of Th1 increased by about 60% and 130% after OFF and semi-ON state stressing, respectively.

Unfortunately, it was not possible to determine E_a and σ_C of Tn3 due to a limited time response of the standard capacitance meter. Nevertheless, this process could be assigned to electron emission of bulk traps located in the GaN buffer, as it was filled even with V_g = 0 filling pulse. Note that V_{gs} > 0 V would be necessary to fill traps near the conduction band of the InAlN barrier layer. Th1 process showed well-defined E_a and σ_C of 0.66 eV and 4×10^{-16} cm^2, respectively, for fresh as well as stressed devices. Hole trap feature has been reported for InAlN/GaN HEMTs using gate controlled constant-I_d deep-level transient spectroscopy [39]. The hole-like emission process observed here is, however, unlikely to be related to a real hole emission. Even though generation of holes in InAlN can be expected already at $V_{\rm gs}$ = −4 V [as deduced from the Poisson–Schrödinger calculation of the band diagram shown in the inset of Fig. 8(a)], generated holes would be immediately injected into the metal. Instead, hole-like emission process can be attributed to electron trapping in the InAlN barrier. The electrons injected from the gate by thermionic field emission can be captured by traps, as shown in the inset of Fig. 8(a). Similar effect has been recently reported for Al_2O_3/AlGaN/GaN MOS HEMTs [30]. In contrast to monotonic increase of $V_{\rm th}$ with time observed in [30], the faster electron emission observed here affects the trapping process at the beginning of the transient. The measured E_a can be then interpreted as a difference between the metal Fermi level and the trap level in InAlN.

$V_{\rm th}$ transient analysis therefore indicates prominent generation of pre-existing type of traps in the GaN buffer after semi-ON state stress, while both OFF state and semi-ON state stresses are likely to increase the density of pre-existing traps in the InAlN barrier layer. This is consistent with the stress-induced $R_{\rm CH}$ changes, assuming stronger effect of GaN bulk traps located close to the channel compared with those located at the InAlN surface. Finally, we note that even though dc transfer characteristics showed similar $V_{\rm th}$ for devices before and after semi-ON state stress, $V_{\rm th}$ transient analysis revealed more profound $V_{\rm th}$ drift for the stressed device. However, counteracting Tn3 and Th1 processes can effectively cancel out each other at a steady-state condition reached during the dc measurement.

C. Hot-Electron Degradation

Strong degradation of $R_{\rm CH}$ and saturation I_d measured in the pulsed mode in the devices submitted to semi-ON stressing together with no degradation of the gate leakage current suggest hot-electron driven degradation in InAlN/GaN HEMTs. This is consistent with stress-induced degradation of $R_{\rm CH}$ in InAlN/GaN devices reported in [15]–[17], keeping in mind possible punchthrough effect in short-channel devices analyzed in [16], explaining faster onset of $R_{\rm CH}$ degradation upon OFF state compared with semi-ON state stressing. Following the assignment of the trapping processes in the previous section, $R_{\rm CH}$ degradation can be related to Tn3 electron emission in the GaN bulk deduced from the $V_{\rm th}$-transient analysis, keeping in mind a good correlation between the stress-induced changes in the magnitude of $R_{\rm CH}$ and Tn3 amplitude. Ionized donor levels responsible for Tn3 emission could serve as efficient scattering centers in the transistor's channel. On the other hand, generation of preexisting (Tn1) and new surface/interface traps in the gate-to-drain (Tn2) can

be related to less dominant R_{D} degradation, whereas possible trapping in the InAlN barrier can be related to both hot-electron related trap generation as well as gate electron injection at large $V_{\mathrm{gd}} = 100$ V. Therefore, in terms of hot-electron trap generation in GaN HEMTs, the emission process Tn3, ascribed to GaN bulk trap emission, is likely to represent the most relevant trap. Work toward characterizing the trap level signature is ongoing.

Regarding the physical mechanism under hot-electron degradation in the GaN buffer, a release of hydrogen by hot electrons from a pre-existing defect, such as hydrogenated Ga vacancy, N antisite, or divacancy, has been proposed in [40]–[42]. The energy necessary for hydrogen removal from triply hydrogenated Ga vacancy and divacancy and placing the atom into H_2 molecule has been calculated to be 2.2 and 2.0 eV, respectively [42]–[44]. If we assume this mechanism to take place, it comes from the T_e analysis that hot electrons have enough energy to strip one or more electrons from both defects during stressing, even though other mechanism cannot be ruled out.

IV. Conclusion

Hot-electron temperature was analyzed in InAlN/GaN HEMTs using EL spectroscopy and HD simulations. T_e in the range of 4700–8000 K was determined for InAlN/GaN HEMTs as a function of V_{gs} at $V_{\mathrm{ds}} = 30$ V. Similar AlGaN/GaN HEMT yielded T_e of 2600 K at $V_{\mathrm{gs}} = 0$ and $V_{\mathrm{ds}} = 30$ V. Good agreement between measurement and averaging of the calculated T_e distribution indicates that hot electrons can locally reach temperature of up to 30 000 K. To illustrate the effect of high T_e, InAlN/GaN HEMTs were stressed at $V_{\mathrm{gd}} = 100$ V. Strong R_{CH} degradation taking place only upon semi-ON state suggests hot-electron driven degradation. The V_{th} and I_d transient analyses revealed four trap emission processes affected by hot-electron degradation. Among them, electron emission with $\tau \sim 100$ ms at room temperature, ascribed to pre-existing GaN buffer trap, was proposed to be related to the hot-electron-induced R_{CH} degradation. Possible mechanism for the trap generation via dehydrogenation was discussed.

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