On the Material Depletion Rate due to Electromigration in a Copper TSV Structure

R. L. de Orio*, S. Gousseau[†‡§], S. Moreau[‡], H. Ceric[¶‖], S. Selberherr[¶],
A. Farcy[†], F. Bay[§], K. Inal[§], and P. Montmitonnet[§]
*School of Electrical and Computer Engineering, UNICAMP,
Av. Albert Einstein 400, 13083-852 Campinas - SP, Brazil.
[†]STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles, France.
[‡]CEA-LETI, MINATEC Campus, 17 rue des Martyrs, F-38054 Grenoble, France.
[§]MINES-ParisTech CEMEF, UMR CNRS 7635, 1 rue Claude Daunesse, 06904 Sophia Antipolis Cedex, France.
[¶]Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, A-1040 Wien, Austria.
[‖]Christian Doppler Laboratory for Reliability Issues in Microelectronics, Austria.

Abstract— **We investigate the material depletion rate from a fatal void due to electromigration in a Cu interconnect structure ended by a TSV. Experiments show the formation of a fatal void above the TSV. Its volumetric growth rate is practically constant for an extended period, but at longer times a significant increase is observed. We have carried out numerical simulations to reproduce the aforementioned void growth behavior. The model incorporates the void size dependence on the incoming flux of vacancies due to electromigration. The simulation results have provided a good description for the void volume and for the growth rate increase for the entire time window of the experiments.**

I. Introduction

Three-dimensional (3D) integration is a promising technology which allows the fabrication of Integrated Circuits (ICs) which go beyond the conventional scaling. It has become a major development field for the microelectronics industry. Some of the main advantages enabled by this technology are the addition of more functionalities on a chip with a higher packing density, providing better performance and less power consumption [1]. A key structure to realize 3D integration is the Through Silicon Via (TSV), a connection from the front to the back side of a chip [2]. Thus, the TSV consists of a conducting via fabricated trough a silicon substrate, which can be used to connect components of different integration levels [1].

Reliability is a critical issue for new emerging technologies, in particular, for TSVs [3]. Electromigration (EM) is one of the main reliability concerns in back-end of line (BEOL) interconnects. EM failure mechanisms have been extensively studied for copper dual-damascene interconnects, where failure is characterized by the resistance increase with time associated to EM induced material transport. Typically, resistance measurements show an initial period with very small resistance change, followed by a subtle increase phase and further linear growth [4]. Frank *et al.* [5] have shown that for structures with a TSV formed on a pad at the cathode end of line the resistance development is somewhat different. They have observed that the subtle resistance increase phase does not occur, so that the interconnect resistance remains initially constant and then starts to increase following a logarithmic time dependence.

In this work we analyze the material depletion rate from a fatal void due to EM in a typical Cu TSV structure. Experiments have shown the growth of a fatal void at a constant rate for most of the tested time window. However, at later times a sudden faster growth rate is observed. We have proposed a model to describe the aforementioned void growth based on the void size dependence of the incoming flux of vacancies due to EM. Based on this model numerical simulations of the the EM-induced vacancy flux around the void as a function of the void size have been carried out.

II. Experimental Setup

The studied TSV structure is shown in Fig. 1. It is fabricated with a typical damascene process. The voiding area and the structure dimensions are given in Fig. 1(b).

The experimental set-up consist of a SEM JEOL 7500F, a heating system, and a Keithley 2402a module to, respectively, characterize the sample, heat it up to the test temperature, and electrically stress the test structure in its package and measure the electrical resistance (4-point method).

The test structure (Fig. 1) is designed with 2 levels: a top metallic level with the measurement pads, and a bottom metallic line. The connection between the two levels is ensured by one TSV on the anode side and four TSVs on the cathode side. This design ensures that any critical defect is always on the anode TSV side, straight above the TSV in M_{top} or under in M_{bot}, depending on the electron flow. The experiment starts with the first case which is easier in terms of observations and sample preparation.

Concerning the size of the structure, the TSVs are 15 μm long with a diameter of 3–4 μm. Both metal lines are 350 nm thick. The top line is 14 μm wide, while the bottom line is 4 μm wide, with an enclosure of 2 μm under the TSV. The sample is protected by a passivation layer with a thickness of 1.1 μm. The geometry and fabrication process are described in more detail in [6]. The sample preparation consists of removing the passivation without removing the SiN layer

 978-1-4799-7274-6/14/$31.00 ©2014 IEEE

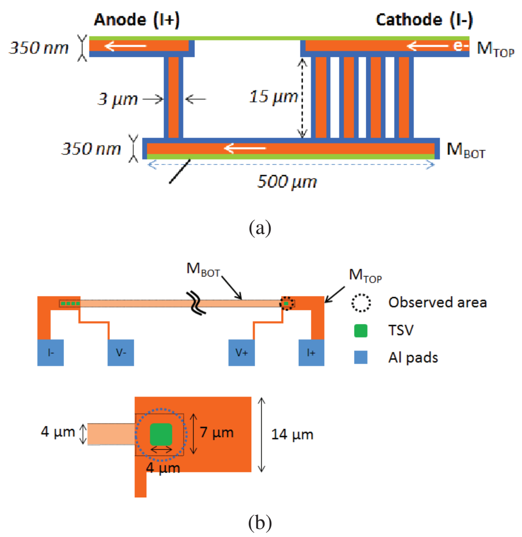

Fig. 1. (a) Electromigration test structure. (b) Details of the test structure [7].

(40 nm), in order to keep the failure mechanism unchanged. The layer is removed by a combination of plasma etch (O_2 and CF_3 gazes) and chemical etch (hydrofluoric acid, HF).

The accelerated test conditions are 350 °C and 25 mA. The sample is observed in the top view.

III. Modeling

EM creates an atomic flux in the direction of the electron flow in a metal line. Thus, this flux causes material depletion on one side of the line and material accumulation on the opposite one. The aforementioned material depletion is commonly described by an accumulation of vacancies. Therefore, the vacancy flux $\vec{J_v}$ driven by EM can be written as

$$\vec{J_v} = D_v C_v \frac{e|Z^*|\rho\vec{j}}{kT}, \tag{1}$$

where D_v is the effective vacancy diffusivity, C_v is the vacancy concentration, $e|Z^*|$ is the effective charge, ρ is the electrical resistivity of the metal, $\vec{j}$ is the current density, k is the Boltzmann's constant, and T is the temperature. Considering that an initial cylindrical void is located above the TSV in the top metal layer (M_{top}) of the anode side of the test structure shown in Fig. 1, the void is fed with the vacancies driven by the current $I+$. The rate of vacancies reaching the void is given by [5]

$$\frac{\partial N_v}{\partial t} = A_l J_v, \tag{2}$$

where A_l is the line cross sectional area. Vacancies are captured by the void, so that the rate of volume change is

$$\frac{\partial V}{\partial t} = \alpha\Omega_v \frac{\partial N_v}{\partial t} = \alpha\Omega_v A_l J_v, \tag{3}$$

where α ($0 < \alpha < 1$) is the ratio of vacancies captured, which leads to void growth, $\Omega_v = f\Omega$ is the vacancy volume, where Ω is the atomic volume and f is the ratio of the vacancy volume in relation to the atomic one. Given the void above the TSV is cylindrical and spans the line thickness, its volume is

$$V = \pi r^2 h, \tag{4}$$

where r is the void radius and h is the line thickness. Using (3) and (4), the rate of volume change is given by

$$\frac{\partial V}{\partial t} = 2\pi hr\frac{\partial r}{\partial t} = \alpha\Omega_v A_l J_v. \tag{5}$$

This equation shows that the rate of void growth can be estimated, if the flux of incoming vacancies is known. We analyze below two cases regarding the vacancy flux.

- Constant flux:
  Assuming that the flux J_v remains constant, which implies that the rate of vacancies captured by the void is constant, (3) and (5) describe a constant rate for the volumetric growth of the void. Consequently, the void volume has a linear increase with time,

  $$V(t) = V_0 + \alpha\Omega_v A_l J_v (t - t_0), \tag{6}$$

  where V_0 and t_0 are given initial values.

- Variable flux:
  The assumption of a constant flux means that the void size has no impact on the capture rate of vacancies and on the flux driven by EM. In this case the volumetric growth of the void is always linear with time, as discussed above. However, the growth of the void is accompanied by changes in the atomic concentration, current density, mechanical stress, etc. around it. Furthermore, these changes are more and more pronounced as the void becomes larger. This means that the constant rate of vacancy capture is not really applicable, which implies a deviation from the linear volumetric growth as will be shown in Section IV.
  Considering that the vacancy flux captured by the void depends on its size, (5) is rewritten as

  $$\frac{\partial V}{\partial t} = \alpha\Omega_v A_l J_v(V). \tag{7}$$

  Given $J_v(V)$, (7) can be integrated, so that the time to grow a void of a given volume V becomes

  $$t(V) = t_0 + \frac{1}{\alpha\Omega_v A_l} g(V), \tag{8}$$

  where

  $$g(V) = \int_{V_0}^{V} \frac{dV'}{J_v(V')}, \tag{9}$$

  and V_0 is an initial volume corresponding to time t_0. Performing numerical simulations of the flux around the void as a function of void size and applying (9) allows to relate a given void volume with time, so that the data can be compared to the experimental results.

IV. RESULTS

As a consequence of the material transport caused by EM a fatal void is formed in the line above the TSV. This is the region expected to have the highest vacancy flux divergence. The Cu line is surrounded by a TiN layer at the bottom and at the sides and by a SiN layer on top, so these interfaces act as blocking boundaries for the vacancy flux. The void development leading to the failure is shown in Fig. 2. Three voids are present in the vicinity of the TSV. The voids grow and join forming a larger single void right above the TSV, which will be responsible for the EM-induced failure.

The resistance change with time associated to the void growth is shown in Fig. 3. The resistance change is very small up to approximately 327 h, when a sudden increase of more than 10% is observed. After this jump, the resistance of the structure increases linearly with time. This is commonly observed in typical Cu damascene interconnects during EM experiments, where the current is forced to flow through the very thin barrier layer which surrounds the metal line after the void spans the whole line thickness. A similar behavior is obtained here, as after the resistance jump the current flows through the thin TiN layer. Furthermore, the void is larger at the Cu/SiN interface than at the Cu/TiN interface [7]. This suggests that the former is the main path for vacancy transport to the void. It should be pointed out, however, that a logarithmic resistance increase was previously observed in experiments with similar structures [5], [8].

The increase of the total void volume over time is shown in Fig. 4. The volume grows at a smaller rate up to 700 h and thereafter the growth rate increases significantly. Moreover, the void volume shows a linear growth up to 700 h (cf. Fig 4). Considering the modeling presented in Section III, it is clear that this linear increase of the void volume with time is consistent with the constant flux assumption. However, it cannot describe the volume change after 700 h. After this time, there's coalescence of other voids in the line.

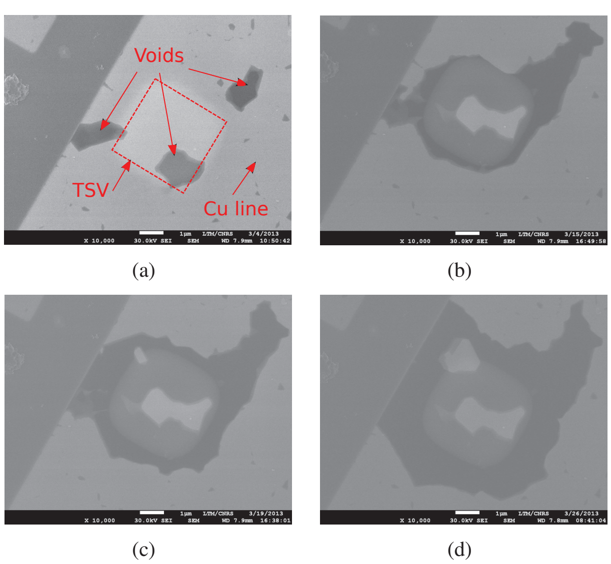

Fig. 2. Growth of the void above the TSV due to EM. (a) 66 h. (b) 336 h. (c) 432 h. (d) 592 h.

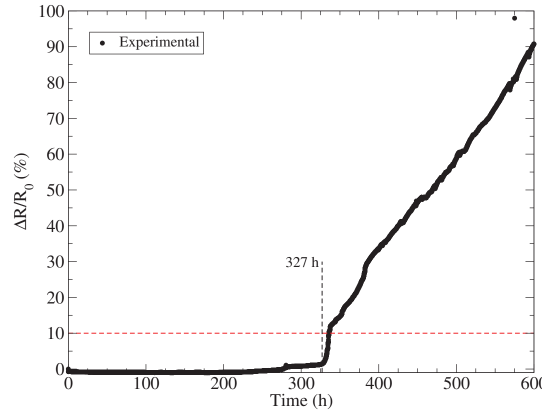

Fig. 3. Typical resistance change with time.

The measured volumetric depletion rate V/t is shown in Fig. 5. The depletion rate is practically constant at 0.0269 μm^3/h for up to 700 h and exhibits a larger rate afterward. Again, consistency between the constant flux model and the experimental results is obtained up to 700 h.

The qualitative analysis of Fig. 4 and Fig. 5 indicates that the constant flux model provides a reasonable approximation for a time up to 700 h. However, for longer times a significant deviation from the linear volume increase or constant volumetric growth rate is observed.

In order to take the flux variation into account as the void grows numerical simulations have been carried out. The simulations were performed using the finite element tool FEDOS [9]. The void is described by a field parameter as in a diffuse interface model [10]. The average vacancy flux around the void is calculated as a function of the void volume, $J_v(V)$, where the void is assumed to be cylindrical. Fig. 6 shows the field parameter for three different volumes and Fig. 7 shows the flux variation (relative to the flux in the line) with the void volume.

The calculated flux is inserted into (9) and a numerical integration is performed. In this way a relationship between the void volume and time is determined according to (8). The simulation results for $V(t)$ and the volumetric depletion rate V/t are shown in Fig. 4 and Fig. 5, respectively, together with the experimental data.

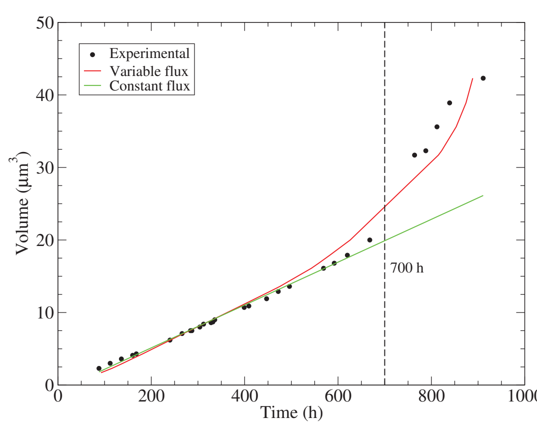

Fig. 4. Void volume as a function of time.

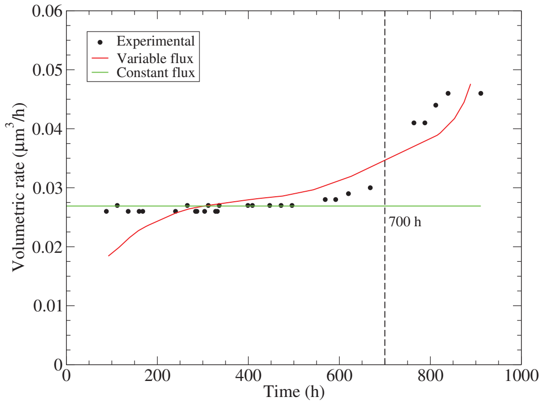

Fig. 5. Rate of volume growth (V/t) as a function of time.

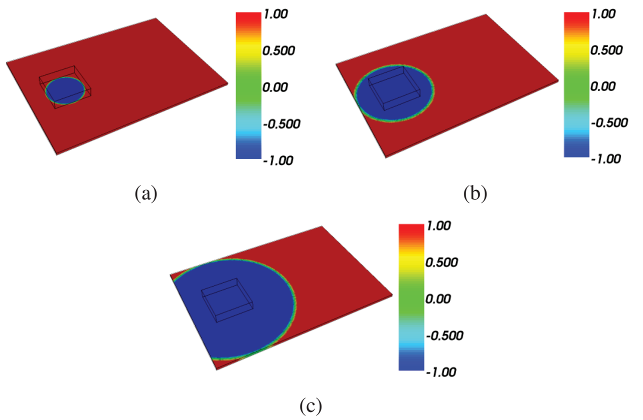

Fig. 6. Numerical simulation of the void growth. The field parameter value of -1 (blue) corresponds to the void, +1 (red) to the metal bulk, while the void surface is represented by values between -1 and +1.(a) Void radius = 2 μm. (b) Void radius = 4 μm (c) Void radius = 7 μm.

In general, the experimental and the simulation results are in good agreement. From Fig. 5 we observe a larger error for the volumetric depletion rate at very early times. This is expected, because the accurate time for void nucleation is not known. Thus, the initial conditions of (8), V_0 and t_0, are not well determined. We have set $V_0 = 1.7\ \mu\text{m}^3$, which is equal to the first measured void volume. In this way, fitting (8) to the experimental data yields $t_0 = 92.3$ h. This value is significantly larger than the 66 h obtained experimentally for the same void volume, which explains the smaller rate at shorter times as shown in Fig. 5. Moreover, the model is certainly less accurate at the early stages of the void development, because it assumes a single cylindrical void, while the experiments show the existence of three smaller voids above the TSV region. Nevertheless, the simulations yield a very good description for the increase of the void volume with time (Fig. 4), while providing a reasonable estimation of the material depletion rate (Fig. 5) based on a model which can be easily evaluated.

V. Conclusion

EM experiments in a Cu TSV structure showed growth of a fatal void above the via. The void volume increases linearly, i.e. the material depletion rate is constant, for most of the testing time. However, a rapid increase of the depletion rate was observed at longer times. These have been reproduced by modeling the effect of void size on the material depletion rate through the vacancy flux. Numerical simulations of the void volume and of the growth rate increase with time resulted in a good agreement with the experimental data.

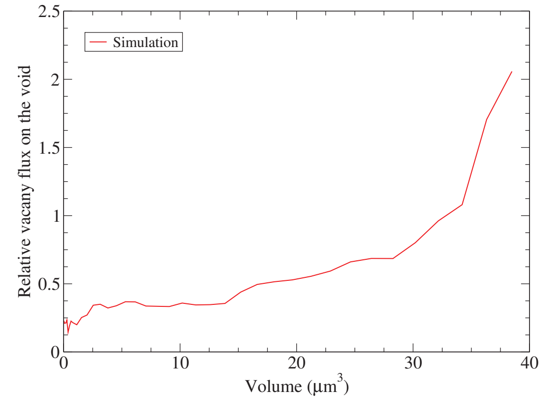

Fig. 7. Flux around the void (relative to line flux) as a function of volume.

Acknowledgment

This work was partially supported by the Austrian Science Fund FWF, project P23296-N13 and partially by the French national program “Programme d’Investissements d’Avenir, IRT Nanoelec” ANR-10-AIRT-05. The travel expenses were partially supported by grant 2014/18210-4, São Paulo Research Foundation (FAPESP) and partially by PROEX/CAPES.

References

[1] J.-Q. Lu, K. Rose, and S. Vitkavage, “3D Integration: Why, What, Who, When?” *Future Fab Intl.*, vol. 23, pp. 25–27, 2007.
[2] M. Motoyoshi, “Through-Silicon Via (TSV),” *Proc. of the IEEE*, vol. 97, pp. 43–48, 2009.
[3] M. Koyanagi, “3D Integration Technology and Reliability,” *Proc. Intl. Reliability Physics Symp.*, pp. 328–324, 2011.
[4] L. Doyen, E. Petitprez, P. Waltz, X. Federspiel, L. Arnaud, and Y. Wouters, “Extensive Analysis of Resistance Evolution due to Electromigration Induced Degradation,” *J. Appl. Phys.*, vol. 104, p. 123521, 2008.
[5] T. Frank, C. Chappaz, P. Leduc, L. Arnaud, F. Lorut, S. Moreau, A. Thuaire, R. E. Farhane, and L. Anghel, “Resistance Increase due to Electromigration Induced Depletion under TSV,” *Proc. Intl. Reliability Physics Symp.*, pp. 347–352, 2011.
[6] P. Leduc, L. D. Cioccio, B. Charlet, M. Rousseau, M. Assous, D. Bouchu, A. Roule, M. Zussy, P. Gueguen, A. Roman, O. Rozeau, M. Heitzmann, J.-P. Nieto, L. Vandroux, P.-H. Haumesser, R. Quenouillere, A. Toffoli, P. Sixt, S. Maitrejean, L. Clavelier, and N. Sillon, “Enabling Technologies for 3D Chip Stacking,” *Proc. Intl. Symp. on VLSI Technology, Systems and Applications*, pp. 76–78, 2008.
[7] S. Gousseau, S. Moreau, D. Bouchu, A. Farcy, F. Bay, K. Inal, and P. Montmitonnet, “First *in Operando* SEM Observation of Electromigration-Induced Voids in TSV Structure,” *Proc. 39th Intl. Symp. for Testing and Failure Analysis (ISTFA)*, pp. 59–68, 2013.
[8] R. L. de Orio, H. Ceric, and S. Selberherr, “Electromigration Failure in a Copper Dual-Damascene Structure with a Through Silicon Via,” *Microelectron. Reliab.*, vol. 52, pp. 1981–1986, 2012.
[9] H. Ceric, “Numerical Techniques in Modern TCAD,” Dissertation, Technische Universität Wien, 2005.
[10] D. N. Bhate, A. Kumar, and A. F. Bower, “Diffuse Interface Model for Electromigration and Stress Voiding,” *J. Appl. Phys.*, vol. 87, no. 4, pp. 1712–1721, 2000.