Stress Considerations for System-On-Chip Gas Sensor Integration in CMOS Technology

Lado Filipovic* and Siegfried Selberherr

Institute for Microelectronics, Technische Universität Wien, Gußhausstraße 27-29, 1040 Vienna, Austria
Email: {filipovic|selberherr}@iue.tuwien.ac.at

For several decades, researchers have aspired to combine all the necessary components for a gas sensor with microelectronic circuits in order to create an integrated smart gas sensor device. However, these devices will only be embraced by industry and consumers, if their cost of production is reduced [1]. The drive for affordable processing, which is integratable in CMOS technology, has lead to the implementation of novel techniques for the deposition of the sensing metal oxide layer and the use of three-dimensional integration with through-silicon vias (TSVs).

This work analyzes, by means of modelling and simulation, the stress effects of this integration, including the effects of TSV etching and metal oxide deposition on the stress development in the devices' conducting layers and in the surrounding silicon. Two types of TSVs are investigated including a filled copper TSV and one with an open cavity and tungsten-lined sidewalls. The influence of sidewall scallops, present as a result of the deep reactive ion etch process, on the build-up of stress in the region is analyzed and a keep out zone (KOZ) for the TSV is suggested by studying the deviatoric stress tensors and the von Mises stress through the silicon wafer.

The thermal stress resulting from the spray pyrolysis deposition of the metal oxide sensing layer, performed at 400ºC, is investigated along with the residual stress which builds up between connecting islands during metal growth described by the Volmer-Weber model. The gas sensor device operates on top of a micro-hotplate which is heated to temperatures between 300ºC and 550ºC during operation in order to enable the metal oxide to detect multiple gases in the environment. The localized heating generated by the hotplate results in an increased stress in the metal oxide and in the surrounding silicon wafer, suggesting the need for a KOZ around the hotplate.

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References

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***Corresponding author:**
Lado Filipovic, Dr.techn.
Institute for Microelectronics
Technische Universität Wien
Gußhausstraße 27-29 / E360
A - 1040 Wien, Austria
Email: filipovic@iue.tuwien.ac.at
Tel: +43 1 58801-36036
Fax: +43 1 58801-36099