

Novel Buffered Magnetic Logic Gate Grid

T. Windbacher, A. Makarov, V. Sverdlov, and S. Selberherr

Institute for Microelectronics, TU Wien, Vienna, A-1040, Austria

The nowadays performance limiting power dissipation due to leakage has become a critical burden. A simple way to reduce power dissipation is to shut down idle circuit parts. However, when hibernated circuit parts are activated again, their previous state must be recovered. In order to avoid energy and time consuming recovery cycles non-volatile elements must be added to realize the desired instant ON capability. In this work the combination of non-volatile magnetic flip flops and spin transfer torque majority gates to a novel buffered magnetic logic grid is proposed. The buffered logic grid features a highly regular structure, a small layout foot print, and it reduces the information transport due to its shared buffer. The realization of an easily concatenable one-bit full adder based on the novel buffered magnetic logic gate grid is explained.

Introduction

After many decades of steep progress in the semiconductor industry the performance gain due to CMOS scaling will stop in the foreseeable future. This stems from the sharp rise in factory costs and the growing severeness of physical limits (1). Static power consumption and interconnection delay (2) have become a critical burden in state of the art technology. A simple way to reduce power losses due to leakage and, with it, the total power consumption is to shut down idle circuit parts.

However, this rather simple approach has a significant disadvantage. The power cut causes the loss of all the information stored in the circuit. Thus, when a circuit part is reactivated, its previous state must be recovered, which raises power consumption and exacerbates interconnection delay problems. Therefore, in order to avoid energy and time consuming recovery cycles, non-volatile elements must be added to realize the desired instant ON capability (3).

Here, spintronics is very appealing due to its non-volatility, fast switching, and high endurance (4). Even though some feasible solutions are already available and competitive with respect to energy consumption and speed, i.e. magnetic tunnel junction (MTJ) MRAM (5) and non-volatile CMOS MTJ hybrid circuits (3), they are still not able to challenge pure CMOS with regard to integration density. The reason is that the spintronic elements (commonly MTJs) are introduced as mere memory, while the actual computation is carried out by a CMOS circuit. Therefore, additional transistors are required to read and write the MTJs, which rather leads to a decrease in integration density. Therefore, we proposed a magnetic non-volatile flip flop (6) and a magnetic non-volatile shift register (7), which perform the actual computation also in the magnetic domain, thus, reducing complexity and allowing extremely dense layout foot prints.

In this work we present a novel non-volatile magnetic logic gate grid facilitating non-volatile magnetic flip flops (8), (9) as shared buffer memory and spin transfer torque majority gates (STMG) as logic gates (10). First, the basics for the non-volatile flip flop and its operation principle will be explained, then the second essential component, the STMG, will be further elaborated. Third, a general description of the novel buffered magnetic logic gate grid covering its structure and general operation principle follows. As an example, the realization of a one-bit full adder is shown to give a more tangible description of the proposed buffered magnetic logic grid, and finally our findings are condensed and summarized in the conclusion.

Non-volatile magnetic flip flop

Working principle

As explained, the proposed flip flop does not only hold the information in the magnetic domain, but also carries out the logic operations via the spin transfer torque effect. Thus, a much denser and simpler layout can be realized by benefiting from the advantageous features of spintronics.

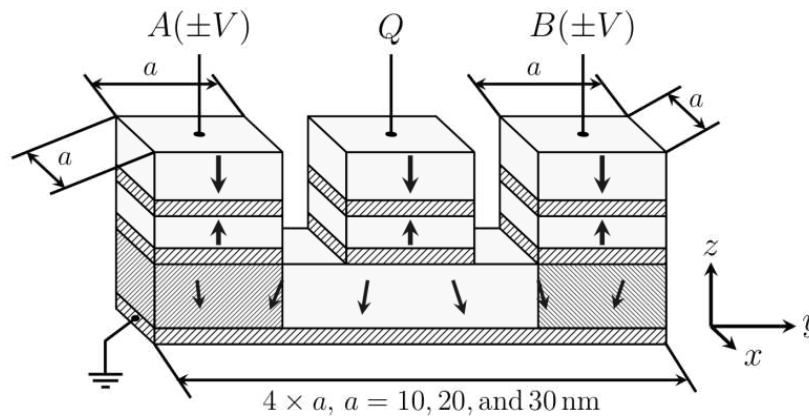


Figure 1. Illustration of the proposed non-volatile magnetic flip flop. The two inputs A and B are operated by current pulses. Logic "0" and "1" is encoded in the pulse polarity. The readout takes place at Q by facilitating the GMR or the TMR effect to determine the logic state stored in the common free layer (high or low resistance).

In order to fully comprehend the operation of the non-volatile magnetic flip flop and later its interaction with the STMG in the buffered magnetic logic gate grid, one has to first explain some of the devices' details and prerequisites. The non-volatile magnetic flip flop consists of three anti-ferromagnetically coupled polarizer stacks and all three stacks possess an out-of-plane magnetization (see Fig. 1). Two stacks are used for input (A and B) and one stack (Q) is used for readout. It is further assumed that the stray fields originating from the anti-ferromagnetically coupled polarizer stacks are negligible. The polarizer stacks are connected to a common free layer with a uniaxial out-of-plane anisotropy K_1 via non-magnetic interlayers (e.g. Cu, MgO or Al_2O_3). Thus, the magnetic orientation of the common free layer can be read out either by the giant magnetoresistance effect (GMR) or the tunneling magnetoresistance (TMR) as a high resistance state (HRS) or a low resistance state (LRS), depending on the relative

orientation between the common free layer orientation and the magnetization orientation of the readout polarizer stack Q. The two distinctive resistance states, HRS and LRS, are mapped to the logic values "0" and "1", respectively.

The devices' thickness is always oriented parallel to the z-axis, the devices' length along the y-axis, and the devices' width is oriented parallel to the x-axis. The applied polarities are mapped to logic "1" and "0" for positive and negative current pulses, respectively. Taking into account a grounded metal layer at the bottom of the free layer and a positive voltage applied to one of the contacts (A, B, or Q), a current flow from the contacts through the free layer towards the bottom contact will be induced (against the z-axis). This flow direction is defined as the positive current direction. At the same time electrons will flow in the opposite direction (positive z-axis).

If now a negative current pulse through one of the input stacks, e.g. A, is applied, the electrons passing through the polarizer stack align to the polarizer magnetization orientation. The polarized electrons cross over to the free layer, relax to the local free layer orientation, and cause a spin transfer torque acting on the local magnetization in the corresponding portion of the free layer. Depending on the relative orientation between the electrons' polarization vector and the local common free layers' magnetization orientation, the generated torque either strives to hold the magnetization orientation in its current position or tries to push it into its opposite stable position. Thus, depending on the input currents' polarity and the common free layers' magnetization orientation the acting torque either drives precessions and eventually will flip the common free layers' magnetization, or damps precessional motions and attempts to hold the magnetization in its current orientation.

In the case of two simultaneously applied current pulses at both input stacks A and B, two spin transfer torques are induced. Depending on the orientation of the two spin transfer torques, they either add constructively (currents possess the same polarity), which accelerates switching, or they oppose each other (currents have opposite polarities), which damps switching.

Therefore, two sufficiently long and high enough current pulses can be used to either SET/RESET (identical polarities) the common free layer as well as HOLD (opposing polarities) the current orientation of the free layer. This behavior represents sequential logic, or more precisely matches flip flops and latches (see Tab. I).

TABLE I. Truth table for the non-volatile magnetic flip flop. A and B are the inputs, Q represents the output, and i describes the i-th time step.

A	B	Q(i)
0	0	0
0	1	Q(i-1)
1	0	Q(i-1)
1	1	1

Simulation setup

To proof the devices' operability, we carried out a series of rigorous simulation studies (6,11,12). The required physical model is covered by the Landau-Lifshitz-Gilbert equation (13,14)

$$\frac{d\vec{m}}{dt} = \gamma \left(-\vec{m} \times \vec{H}_{\text{eff}} + \alpha \left(\vec{m} \times \frac{d\vec{m}}{dt} \right) + \vec{T} \right), \quad [1]$$

with \vec{m} denoting the reduced magnetization, γ the electron gyromagnetic ratio, α the dimensionless damping constant, and \vec{H}_{eff} the effective field. The precessional motion due to the effective magnetic field \vec{H}_{eff} is described by the first term in [1]. A power dissipation proportional to $\frac{d}{dt} \vec{m}$ is introduced by the second term and the last term adds the spin transfer torque \vec{T} . In the case of non-magnetic layers made out of copper the spin transfer torque \vec{T} is given by (15)

$$\vec{T} = \frac{\hbar}{\mu_0 e} \frac{J}{l M_S} \frac{P \Lambda^2}{(\Lambda^2+1)+(\Lambda^2-1) \vec{m} \cdot \vec{p}} (\vec{m} \times \vec{p} \times \vec{m} - \epsilon' \vec{m} \times \vec{p}). \quad [2]$$

\hbar denotes the Planck constant, μ_0 the magnetic permeability, J the applied current density, l the free layer thickness, M_S the magnetization saturation, P the spin current polarization, \vec{p} the unit polarization direction of the polarized current, and Λ a fitting parameter handling non-idealities. The spin transfer torque model for the spin valve exhibits an in-plane $\vec{m} \times \vec{p} \times \vec{m}$ and a small ϵ' out-of-plane component $\vec{m} \times \vec{p}$ (16).

The effective field \vec{H}_{eff} contains contributions from the uniaxial anisotropy, exchange, and demagnetization energy and is gained from the functional derivative of the total free energy density (17).

Our simulations show not only that the device works under ideal conditions, but is also able to tolerate quite high levels of static and thermal disturbances (12). Fig. 2a and Fig. 2b show two examples illustrating our findings. Fig. 2a depicts the switching probability for the SET/RESET operation under the influence of a thermal field of 300K and a variable static random field. The static random field is normally distributed, features a mean value of zero, and its standard deviation is scaled in relation to the saturation magnetization M_S ($H_{i,\text{rand}} = \xi_i \cdot s \cdot M_S$, ξ_i denotes a normally distributed random number and s the disturbance strength). As can be readily seen in Fig. 2a and Fig. 2b, the common free layers with sizes of 10nm×40nm×3nm and 20nm×80nm×3nm switch perfectly for the SET/RESET operation (100%) as well as for the HOLD operation (0%) up to the high level of 50% of M_S disturbance strength.

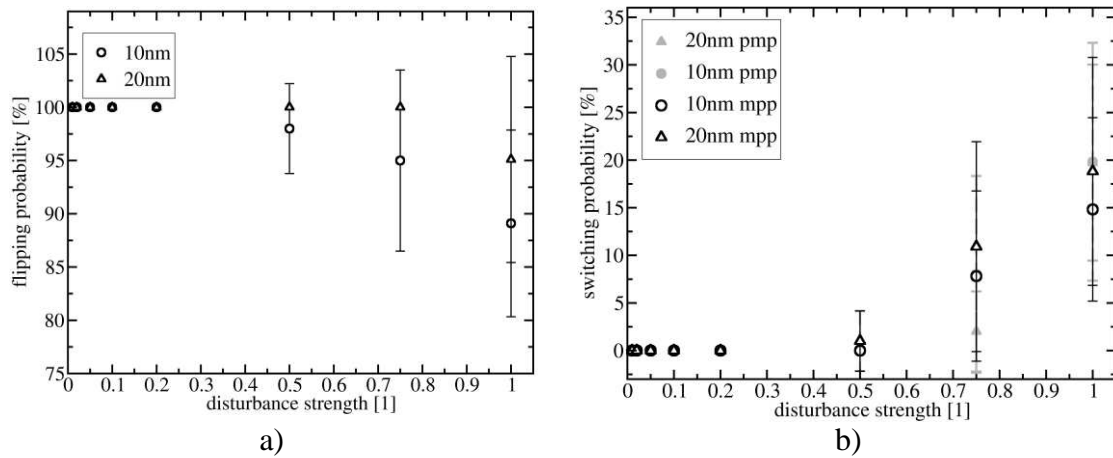


Figure 2. a) Flipping probability as a function of disturbance strength for the SET/RESET operation. b) Flipping probability as a function of disturbance strength for the HOLD operation. The three letters after the layer width denote the polarities of the input pulses and the initial free layer orientation ($- = m, + = p \rightarrow A, B, Q_0$).

Spin transfer torque majority gate

The STMG is perfectly compatible with the non-volatile magnetic flip flop, since it can be built with the same material stacks for polarizers and the common free layer, and the input information is also encoded by the pulse polarity (4). However, there are some essential differences. The STMG comprises four anti-ferromagnetically coupled polarizer stacks. Three polarizer stacks are for input A, B, and C, and one polarizer stack is for readout Q (see Fig. 3). They are connected to a cross shaped common free layer with a perpendicular magnetic uniaxial anisotropy by non-magnetic interconnection layers. This way the three input pulses generate three spin torques on the common free layer. Assuming all three torques are equal in strength (same pulse amplitude), there is no input pulse combination which is capable of evenly balancing the acting input torques. Thus, there is always a surplus from at least one uncompensated torque so that the majority of input torques decides on the operation outcome. Especially intriguing is that by fixing one of the inputs to logic "0" or "1" the majority gate offers a two input AND and OR gate, respectively (cf. Tab. II). In order to complement the majority logic to a functional complete system, which is necessary to compute arbitrary logic functions, logic negation must be added to the system. We propose to flip the polarity of the input pulse to realize the NOT operation, since it is the simplest way to invert the acting torque (see [2]).

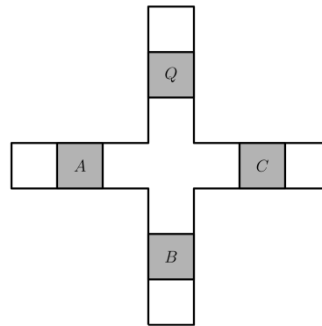


Figure 3. Illustration of a spin transfer torque majority gate. A, B, C depict the three input polarizer stacks and Q the polarizer stack for readout. The side view is analog to the stack structure shown in Fig. 2.

TABLE II. Truth table of a three input (A, B, C) and one output (Q) majority gate. By fixing one of the inputs to logic "0" or "1", AND and OR gates can be realized.

A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Buffered magnetic logic gate grid

Up to now two logic device types, i.e. sequential and combinatorial, have been explained. Both are CMOS compatible and can be used to supplement CMOS logic. Nonetheless, the energy cost of moving data exceeds that of computing nowadays (18). Therefore, it is of utmost importance to reduce the energy and time consuming information transport.

Our proposal to achieve this goal is a buffered magnetic logic gate grid which combines the spin transfer torque majority gates and the non-volatile flip flops. The devices are arranged in a periodic grid like structure (see Fig. 4). The common free layers of the non-volatile flip flops and the spin transfer torque majority gates are positioned in two different depth levels and overlap at their respective ends, where they are interlinked by non-magnetic layers. Thus, the overlapping regions can be exploited to transfer information between the devices via spin transfer torque. For instance, let us consider the copy operation from the central STMG to the hatched flip flop on the left side shown in Fig. 4. By contacting the top and the bottom of the overlapping region one is able to apply current pulses through the stack of the overlapping region. This way the electrons traversing the overlapping stack get first polarized by the common free layer of the STMG, before they enter the non-volatile flip flop. Thus, the magnetization orientation of the STMG's free layer is encoded in the direction of the spin transfer torque acting in the overlap region of the non-volatile flip flop. If one now adds a synchronous clocked signal at the second input of the non-volatile flip flop, the information will be copied to the flip flop's free layer (cf. Tab. I and (7)). Since the common free layer of the STMG and the non-volatile flip flop take considerably longer time at a fixed current density to switch, if only one input is active, compared to the switching time, when all inputs are powered simultaneously, there is a time window for safe copy operations. Analogously, information can be read from the surrounding flip flops for majority operations in the STMG. Again, the key is the switching time shift caused by the number of applied currents.

Thus, a highly regular structure is realized, which allows parallel execution of operations on the logic gates and offers a shared buffer between neighboring gates. This also minimizes the energy and time spent for the information transport. It further holds

the benefit of a very dense layout and supports a shift away from the Von Neumann architecture and its currently performance limiting continuous information flow between physically separated memory and computation units. Even more, the generic layout of the structure not only eases manufacturing, but also enables, together with the majority gates, highly reconfigurable logic and flexible allocation of employed resources, like the number of used gates and buffers, depending on the requirements of the task at hand.

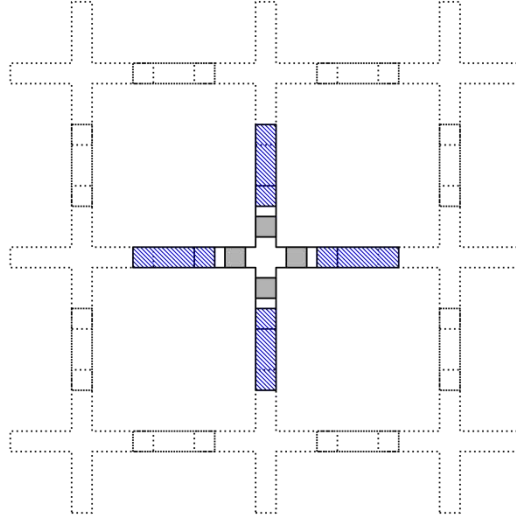


Figure 4. Illustration of the proposed buffered magnetic logic grid. The non-volatile flip flops (rectangles) act as shared buffer and the spin torque majority gates perform the logic operations (crosses). If an electron enters a free layer it is polarized according to the free layer's magnetization orientation, when it crosses over the free layer of an adjacent device the generated spin transfer torques orientation mediates the information stored in the previous layer.

One-bit full adder

To illustrate the idea in a more tangible way, the practical example of an easily concatenable one-bit full adder will be explained in the following (cf. Fig. 5). The considered one-bit full adder possesses three inputs A , B , C_{in} and two outputs Sum and C_{out} .

The carry bit C_{out} is defined as (19):

$$C_{out} = \text{MAJORITY}(A, B, C_{in}) = A \cdot B + A \cdot C_{in} + B \cdot C_{in} \quad [3]$$

and the Sum as:

$$Sum = A \text{ XOR } B \text{ XOR } C_{in} = A \cdot B \cdot C_{in} + A \cdot \bar{B} \cdot \bar{C}_{in} + \bar{A} \cdot B \cdot \bar{C}_{in} + \bar{A} \cdot \bar{B} \cdot C_{in} \quad [4]$$

Since the MAJORITY and NOT form a functional complete basis, the calculation of the sum can be mapped to a sequence of majority and NOT operations:

$$\begin{aligned} \text{MAJORITY}(A, B, C_{in}) &\rightarrow \text{FF1} \\ \text{MAJORITY}(A, B, \bar{C}_{in}) &\rightarrow \text{FF2} \end{aligned} \quad [5]$$

$$\begin{aligned} \text{MAJORITY}(\overline{\text{FF1}}, \text{FF2}, C_{in}) &\rightarrow \text{FF3} \\ \text{FF1} &\rightarrow C_{out} \\ \text{FF3} &\rightarrow \text{Sum} \end{aligned}$$

In a first step the $\text{MAJORITY}(A, B, C_{in})$ is calculated and subsequently copied into a first flip flop FF1 (cf. Fig. 5). Then $\text{MAJORITY}(A, B, \text{NOT}(C_{in}))$ is performed and copied into a second flip flop FF2. Finally the Sum is calculated by reusing the results from the previous steps stored in FF1 and FF2 and performing $\text{MAJORITY}(\text{NOT}(\text{FF1}), \text{FF2}, C_{in})$ in the STMG, which again is copied into a third flip flop FF3. Thus, C_{out} and Sum are calculated and stored via a well defined set of subsequent majority and copy operations. Since C_{out} and Sum are held in the flip flops FF1 and FF3 and these are also accessible to neighboring gates, their information can be (re)used for further processing. The carry bit C_{out} stored in FF1 can be used as carry bit C_{in} for a next one-bit full adder stage realized by an adjacent STMG. After the calculation of C_{out} and the copying to FF1 a subsequent one-bit full adder can already start to calculate C_{out} and Sum for the next stage and does not need to wait, until the previous one-bit full adder is finished. This demonstrates the capability of the proposed buffered magnetic logic grid to perform parallel calculations as well as its capacity to reduce the required information transport over a common bus.

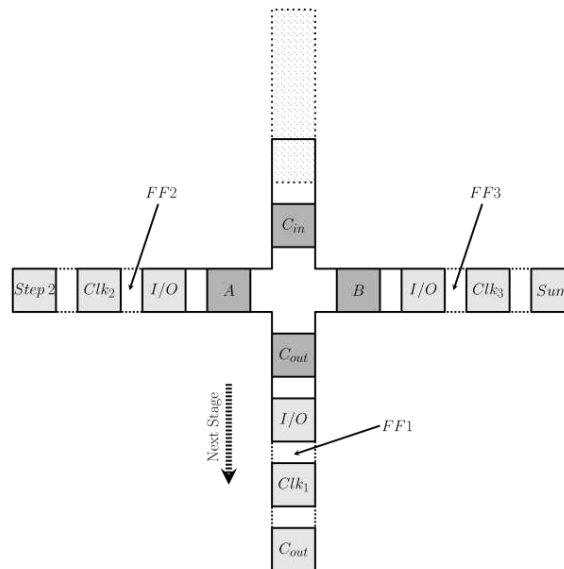


Figure 5. Example of a one-bit full adder realized with a single majority gate and three flip flops as buffers.

Conclusion

A novel buffered magnetic logic grid has been proposed. It consists of spin transfer torque majority gates and non-volatile flip flops, which are arranged in a periodic grid like structure. The spin transfer torque majority gates act as logic gates, while the flip flops act as local shared buffer. The resulting structure is highly regular, non-volatile, reduces the necessary information transport, and offers highly reconfigurable logic and resource allocation. In order to illustrate the operation of the buffered magnetic logic grid an easily concatenable one-bit full adder is demonstrated.

Acknowledgments

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