Spin-Based CMOS-Compatible Devices

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Abstract. With CMOS feature size rapidly approaching scaling limits the electron spin attracts attention as an alternative degree of freedom for low-power non-volatile devices. Silicon is perfectly suited for spin-driven applications, because it is mostly composed of nuclei without spin and is characterized by weak spin-orbit interaction. Elliot-Yafet spin relaxation due to phonons' mediated scattering is the main mechanism in bulk silicon at room temperature. Uniaxial stress dramatically reduces the spin relaxation, particularly in thin silicon films. Lifting the valley degeneracy completely in a controllable way by means of standard stress techniques represents a major breakthrough for spin-based devices. Despite impressive progress regarding spin injection, the larger than predicted signal amplitude is still heavily debated. In addition, the absence of a viable concept of spin manipulation in the channel by electrical means makes a practical realization of a device working similar to a MOSFET difficult. An experimental demonstration of such a spin field-effect transistor (SpinFET) is pending for 25 years now, which at present is a strong motivation for researchers to look into the subject. Commercially available CMOS compatible spin-transfer torque magnetic random access memory (MRAM) built on magnetic tunnel junctions possesses all properties characteristic to universal memory: fast operation, high density, and non-volatility. The critical current for magnetization switching and the thermal stability are the main issues to be addressed. A substantial reduction of the critical current density and a considerable increase of the thermal stability are achieved in structures with a recording layer between two vertically sandwiched layers, where the recording layer is composed of two parts in the same plane next to each other. MRAM can be used to build logic-in-memory architectures with non-volatile storage elements on top of CMOS logic circuits. Non-volatility and reduced interconnect losses guarantee low-power consumption. A novel concept for non-volatile logic-in-memory circuits utilizing the same MRAM cells to store and process information simultaneously is proposed.

1 Introduction

The breathtaking increase in density, speed, and performance of modern integrated circuits has been supported by the continuous miniaturization of CMOS devices. Numerous outstanding technological challenges have been resolved on this exciting journey. However, even though the transistor size is scaled down, the load capacitance per unit area of a circuit stops decreasing. This suggests

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that the on-current must stay constant in order to maintain appropriate high speed operation. Even more, in ultra-scaled MOSFETs with semi-ballistic transport in the channel the conductance determined by the number of transversal propagating modes ceases to depend on the channel length. This results in an approximately constant power dissipation of a single MOSFET regardless of its channel length, which would lead to a rapid increase of dissipated heat with the transistor density further increased. An obvious saturation of MOSFET miniaturization puts clear foreseeable limitations to the continuation of the increase in the performance of integrated circuits. Thus, research for finding alternative technologies and computational principles is paramount.

The principle of MOSFET operation is fundamentally based on the charge degree of freedom of an electron: the electron charge interacts with the gate induced electric field which can close the transistor by creating a potential barrier. Another intrinsic electron property, the electron spin, attracts at present much attention as a possible candidate for complementing or even replacing the charge degree of freedom in future electron devices. It is characterized by two possible projections on a given axis and can be potentially used in digital information processing. In addition, only a small amount of energy is needed to alter the spin orientation, which is necessary for low power applications. The electron spin as a vector may be pointed not only up or down but rather in any direction on a unit Bloch sphere. This opens the way to use the whole Bloch sphere of states to process and store information by initializing, manipulating, and detecting the spin orientation. A successful implementation of a quantum computer utilizing the spin states on the Bloch sphere requires the possibility of efficient spin initiation, coherent manipulation, and reliable read-out. Although encouraging results were achieved, the development of a robust two- and three-qubit gate is a pressing challenge for proceeding to a larger computational network.

Silicon predominantly (92 %) consists of ^{28}Si nuclei with zero magnetic spin. The spin-orbit interaction is also weak in the silicon conduction band. Because of these properties electron spin states of conduction electrons in silicon should show better stability, lower decoherence and longer spin lifetime, which makes silicon a perfect candidate for spin-driven device applications. Even though these features are promising and silicon processing technology is well established the demonstration of basic elements necessary for spin related applications, such as injection of spin-polarized currents into silicon, spin transport, and detection, were demonstrated only recently. Although it should be straightforward to inject spin-polarized carriers into silicon from a ferromagnetic contact, due to a fundamental conductivity mismatch between a ferromagnetic metal contact and the semiconductor, the problem was without solution for a long time. A special technique [1] based on the attenuation of hot electrons with spins anti-parallel to the magnetization of the ferromagnetic film allows creating an imbalance between the electrons with spin-up and spin-down in silicon thus injecting spin-polarized current. The spin-coherent transport through the device was studied by applying an external magnetic field causing precession of spins during their propagation from source to drain. The detection is performed with a similar hot electron spin

filter. Although the drain current is fairly small due to the carriers' attenuation in the source and drain filters, as compared to the current of injected spins, the experimental set-up represents a first spin-driven device which can be envisaged working at room temperature. Contrary to the MOSFET, however, the described structure is a two-terminal device. Nevertheless, the first demonstration of coherent spin transport through an undoped 350μm thick silicon wafer [2] has triggered a systematic study of spin transport properties in silicon [3].

2 Silicon SpinFET

The SpinFET is a future semiconductor spintronic device with a superior performance. A SpinFET is composed of ferromagnetic source and drain contacts, linked by a non-magnetic semiconductor channel region [4]. The effective spin-orbit interaction in the channel depends on the perpendicular electric field, so that the spin of an electron injected from the source starts precessing. Only the electrons with their spin aligned to the drain magnetization can leave the channel contributing to the current. The current modulation is achieved by tuning the strength of the spin-orbit interaction by applying the gate voltage. In order to realize the SpinFET, an efficient spin injection and detection, spin propagation, and spin manipulation by purely electrical means must be achieved [5]. Spin injection in silicon from a ferromagnetic metal electrode is compromised by an impedance mismatch problem [6]. A solution to this impedance mismatch problem is the introduction of a potential barrier between the ferromagnetic metal and the semiconductor [7]. An experimental demonstration of a signal which should correspond to spin injection in doped silicon at room temperature was first performed in 2009 [8] using an $Ni_{80}Fe_{20}/Al_2O_3$ tunnel contact. Electrical signals at temperatures as high as 500 K have been reported in [9]. Regardless of the success in demonstrating the signal which should correspond to the spin injection at room temperature, the magnitude of the signal obtained within the three-terminal measurement scheme is a several orders of magnitude larger than the theoretical value [3]. The reasons for the discrepancies are heavily debated [3,10]. A plausible explanation suggested recently [11] interprets the large signal to be rather due to the trap assisted tunneling magnetoresistance.

When spin is injected, the possibility to transfer the excess spin injected from the source to the drain electrode is essential. The excess spin is not a conserved quantity. While diffusing, it gradually relaxes to its equilibrium value which is zero in a non-magnetic semiconductor. An estimation for the spin lifetime at room temperature obtained is ranging between 0.1 to 10ns [3], depending on doping. This corresponds to the spin diffusion length $l = 0.2\text{-}2\mu$m. The spin lifetime is determined by the spin-flip processes [12,13]. In silicon the spin relaxation due to the hyperfine interaction of spins with the magnetic moments of the ^{29}Si nuclei (the natural abundance is 4.7 %) is only important at low temperature, while the spin relaxation by the Elliot-Yafet mechanism [12,13] due to electron-phonon scattering is dominant at room temperature. The Elliot-Yafet mechanism is mediated by the intrinsic interaction between the orbital motion of

an electron and its spin and electron scattering. When the microscopic spin-orbit interaction is taken into account, the Bloch function with a fixed spin projection is not an eigenfunction of the total Hamiltonian. Because the eigenfunction contains a contribution with an opposite spin projection, even spin-independent scattering with phonons generates a small probability of spin flips [14].

In bulk silicon the main contribution to spin relaxation is due to optical phonon scattering between the valleys residing along different crystallographic axis, or f-phonons scattering [15,16]. A relatively large spin relaxation reported in electrically-gated lateral-channel silicon structures [17,18] indicates that the extrinsic interface induced spin relaxation mechanism is important. This may pose an obstacle in realizing spin-driven CMOS-compatible devices, and a deeper understanding of the fundamental spin relaxation mechanisms in silicon inversion layers, thin films, and fins is needed.

The theory of spin relaxation must account for the most relevant scattering mechanisms in thin silicon-in-insulator films: electron-phonon interaction and surface roughness scattering. In order to evaluate the corresponding spin relaxation matrix elements, the wave functions with opposite spin projections must be found. We employ the Hamiltonian which takes into account the only relevant valley pair along the [1]-axis [19]. The Hamiltonian must include confinement and, most importantly, an effective spin-orbit interaction. Shear strain lifts the degeneracy between the unprimed subbands [20]. The enhanced valley splitting rapidly reduces the main contribution to spin relaxation due to inter-valley scattering. This results in a giant spin lifetime enhancement shown in Fig. 1. Shear strain used to enhance the performance of modern MOSFETs is extremely efficient in enhancing the spin lifetime and the spin diffusion length in silicon thin films.

Silicon is characterized by weak spin-orbit interaction and is not considered as a candidate for a SpinFET channel material. In actual thin films the inversion symmetry is broken, and a relatively large value for the spin-orbit coupling [21] is predicted by atomistic calculation $\beta \approx 2\mu$eVnm [22], in agreement with the value reported experimentally [23]. The channel length needed to achieve a substantial tunneling magnetoresistance (TMR) modulation is close to a micron [24].

3 Spin-Transfer Torque Magnetic RAM

The basic element of magnetic random access memory (MRAM) is a magnetic tunnel junction (MTJ). The three-layer MTJ represents a sandwich of two magnetic layers separated by a thin spacer which forms a tunnel barrier. While the magnetization of the pinned layer is fixed, the magnetization orientation of the recording layer can be switched between the two stable states parallel and anti-parallel to the fixed magnetization direction. A memory cell based on MTJs is scalable, exhibits relatively low operating voltages, low power consumption, high operation speed, high endurance, and a simple structure. Switching between the two states is induced by spin-polarized current flowing through the MTJ [25,26]. The recording layer magnetization switching, by means of the

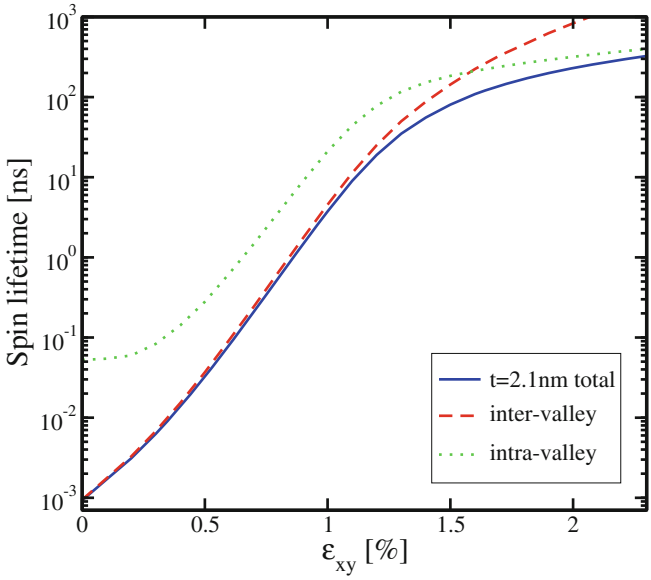

Fig. 1. Dependence of spin lifetime on shear strain for T = 300 K in a film of 2.1 nm thickness. The inter- and intra-valley contributions are also shown...

spin-transfer torque (STT), makes STT-MRAM a promising candidate for future universal memory.

Because the spin-polarized current is only a fraction of the total charge current passing through the cell, the reduction of the current density required for switching and the increase of the switching speed are the most important challenges in STT-MRAM developments. We demonstrated by micromagnetic simulations that, if the recording layer is composed of two parts, a nearly three time faster switching is achieved [27]. Thanks to the removal of the central part in the recording layer the magnetization switching occurs in-plane. This use of the composite structure of the recording layer allows to decrease the switching energy while preserving the thermal stability [28,29].

4 STT-MRAM Based Logic-in-Memory

The introduction of non-volatile logic could help to reduce significantly the heat generation, especially at stand-by, booting, and resuming stages. It is extremely attractive to use the same elements as memory and latches to reduce the time delay and energy waste while transferring data between CPU and memory blocks. The MRAM technology is promising for building logic-in-memory configurations which combine non-volatile memory cells and logic circuits [30,31].

It is even more attractive to use the memory arrays to carry logic operations. In [32,33] MTJ-based reprogrammable logic gates realize the basic Boolean logic

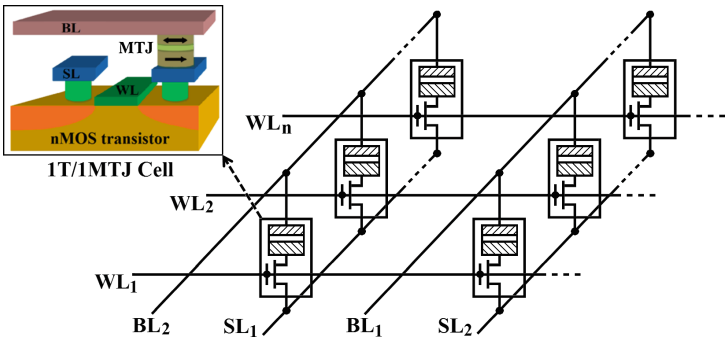

Fig. 2. The common STT-MRAM architecture based on the one-transistor/one-MTJ (1T/1MTJ) structure.

operations AND, OR, NAND, NOR, and the Majority operation. A material implication (IMP) logic gate [34] can be implemented by using any two MRAM memory cells from an MRAM array (Fig. 2) to perform the Boolean IMP operation. A sequence of logical IMP supplemented with FALSE allows to perform any given Boolean operation.

Compared to the TiO_2 memristive switches [35], MRAM provides a higher endurance. Furthermore, the bistable resistance state of the MRAM cell eliminates the need for refreshing circuits. The logic implementation using MRAM cells relies on a conditional switching of MTJs caused by the state-dependent current modulation on the output (target) MTJ. The resistance modulation between the high and low resistance states in the MTJ is proportional to the TMR ratio. The error probability of MTJ-based operations decreases with increasing TMR ratio which is thus the most important device parameter for the reliability [36].

5 Summary and Conclusion

Recent ground-breaking experimental and theoretical findings regarding spin injection and transport in silicon make spin an attractive option to supplement or to replace the charge degree of freedom for computations. Uniaxial stress employed to enhance the electron mobility can also be used to boost the spin lifetime significantly. CMOS-compatible STT-MRAM cells built on magnetic tunnel junctions with a composite recording layer demonstrate a three-fold improvement of the switching time as compared to similar cells with a monolithic layer. The realization of an intrinsic non-volatile logic-in-memory architecture by using MRAM arrays is demonstrated.

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References

1. Appelbaum, I., Huang, B., Monsma, D.J.: Electronic measurement and control of spin transport in Silicon. Nature **447**, 295–298 (2007)
2. Huang, B., Monsma, D.J., Appelbaum, I.: Coherent spin transport through a 350 micron thick silicon wafer. Phys. Rev. Lett. **99**, 177209 (2007)
3. Jansen, R.: Silicon spintronics. Nat. Mater. **11**, 400–408 (2012)
4. Datta, S., Das, B.: Electronic analog of the electro-optic modulator. Appl. Phys. Lett. **56**, 665–667 (1990)
5. Sugahara, S., Nitta, J.: Spin-transistor electronics: an overview and outlook. Proc. IEEE **98**, 2124–2154 (2010)
6. Schmidt, G., Ferrand, D., Molenkamp, L.W., Filip, A.T., van Wees, B.J.: Fundamental obstacle for electrical spin injection from a ferromagnetic metal into a diffusive semiconductor. Phys. Rev. B **62**, R4790–R4793 (2000)
7. Rashba, E.I.: Theory of electrical spin injection: tunnel contacts as a solution of the conductivity mismatch problem. Phys. Rev. B **62**, R16267–R16270 (2000)
8. Dash, S.P., Sharma, S., Patel, R.S., de Jong, M.P., Jansen, R.: Electrical creation of spin polarization in silicon at room temperature. Nature **462**, 491–494 (2009)
9. Li, C., van't Erve, O., Jonker, B.: Electrical injection and detection of spin accumulation in silicon at 500K with magnetic metal/silicon dioxide contacts. Nat. Commun. **2**, 245 (2011)
10. Jansen, R., Deac, A.M., Saito, H., Yuasa, S.: Injection and detection of spin in a semiconductor by tunneling via interface states. Phys. Rev. B **85**, 134420 (2012)
11. Song, Y., Dery, H.: Magnetic-field-modulated resonant tunneling in ferromagnetic-insulator-nonmagnetic junctions. Phys. Rev. Lett. **113**, 047205 (2014)
12. Zutic, I., Fabian, J., Das Sarma, S.: Spintronics: fundamentals and applications. Rev. Mod. Phys. **76**, 323–410 (2004)
13. Fabian, J., Matos-Abiaguea, A., Ertler, C., Stano, P., Zutic, I.: Semiconductor spintronics. Acta Phys. Slovaca **57**, 565–907 (2007)
14. Cheng, J.L., Wu, M.W., Fabian, J.: Theory of the spin relaxation of conduction electrons in silicon. Phys. Rev. Lett. **104**, 016601 (2010)
15. Li, P., Dery, H.: Spin-orbit symmetries of conduction electrons in silicon. Phys. Rev. Lett. **107**, 107203 (2011)
16. Song, Y., Dery, H.: Analysis of phonon-induced spin relaxation processes in silicon. Phys. Rev. B **86**, 085201 (2012)
17. Li, J., Appelbaum, I.: Modeling spin transport in electrostatically-gated lateral-channel silicon devices: role of interfacial spin relaxation. Phys. Rev. B **84**, 165318 (2011)
18. Li, J., Appelbaum, I.: Lateral spin transport through bulk silicon. Appl. Phys. Lett. **100**, 162408 (2012)
19. Osintsev, D., Baumgartner, O., Stanojevic, Z., Sverdlov, V., Selberherr, S.: Subband splitting and surface roughness induced spin relaxation in (001) silicon SOI MOSFETs. Solid-State Electron. **90**, 34–38 (2013)
20. Sverdlov, V.: Strain-Induced Effects in Advanced MOSFETs. Springer, Wien - New York (2011)
21. Jancu, J.M., Girard, J.C., Nestoklon, M.O., Lemaître, A., Glas, F., Wang, Z.Z., Voisin, P.: STM images of subsurface Mn Atoms in GaAs: evidence of hybridization of surface and impurity states. Phys. Rev. Lett. **101**, 196801 (2008)
22. Prada, M., Klimeck, G., Joynt, R.: Spin-orbit splittings in Si/SiGe quantum wells: from ideal Si membranes to realistic heterostructures. New J. Phys. **13**, 013009 (2011)

23. Wilamowski, Z., Jantsch, W.: Suppression of spin relaxation of conduction electrons by cyclotron motion. Phys. Rev. B **69**, 035328 (2004)
24. Osintsev, D., Sverdlov, V., Stanojevič, Z., Makarov, A., Selberherr, S.: Temperature dependence of the transport properties of spin field-effect transistors built with InAs and Si channels. Solid-State Electron. **71**, 25–29 (2012)
25. Slonczewski, J.: Current-driven excitation of magnetic multilayers. J. Magn. Magn. Mater. **159**, L1–L7 (1996)
26. Berger, L.: Emission of spin waves by a magnetic multilayer traversed by a current. Phys. Rev. B **54**, 9353–9358 (1996)
27. Makarov, A., Sverdlov, V., Osintsev, D., Selberherr, S.: Reduction of switching time in pentalayer magnetic tunnel junctions with a composite-free layer. Phys. Status Solidi - Rapid Res. Lett. **5**, 420–422 (2011)
28. Makarov, A., Sverdlov, V., Selberherr, S.: Magnetic tunnel junctions with a composite free layer: a new concept for future universal memory. In: Luryi, S., Xu, J., Zaslavsky, A. (eds.) Future Trends in Microelectronics, pp. 93–101. Wiley, New York (2013)
29. Makarov, A.: Modeling of emerging resistive switching based memory cells. Dissertation, Institute for Microelectronics, TU Wien (2014)
30. Endoh, T.: STT-MRAM technology and its NV-logic applications for ultimate power management. In: 2014 CMOS Emerging Technologies Research (CMOSETR), p. 14 (2014)
31. Natsui, M., Suzuki, D., Sakimura, N., Nebashi, R., Tsuji, Y., Morioka, A., Sugibayashi, T., Miura, S., Honjo, H., Kinoshita, K., Ikeda, S., Endoh, T., Ohno, H., Hanyu, T.: Nonvolatile logic-in-memory array processor in 90 nm MTJ/MOS achieving 75% leakage reduction using cycle-based power gating. In: 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp. 194–195 (2013)
32. Lyle, A., Harms, J., Patil, S., Yao, X., Lilja, D.J., Wang, J.P.: Direct communication between magnetic tunnel junctions for nonvolatile logic fan-out architecture. Appl. Phys. Lett. **97**, 152504 (2010)
33. Lyle, A., Patil, S., Harms, J., Glass, B., Yao, X., Lilja, D., Wang, J.: Magnetic tunnel junction logic architecture for realization of simultaneous computation and communication. IEEE Trans. Magn. **47**, 2970–2973 (2011)
34. Mahmoudi, H., Windbacher, T., Sverdlov, V., Selberherr, S.: Implication logic gates using spin-transfer-torque-operated magnetic tunnel junctions for intrinsic logic-in-memory. Solid-State Electron. **84**, 191–197 (2013)
35. Borghetti, J., Snider, G., Kuekes, P., Yang, J., Stewart, D., Williams, R.: Memristive switches enable stateful logic operations via material implication. Nature **464**, 873–876 (2010)
36. Mahmoudi, H., Windbacher, T., Sverdlov, V., Selberherr, S.: Reliability analysis and comparison of implication and reprogrammable logic gates in magnetic tunnel junction logic circuits. IEEE Trans. Magn. **49**, 5620–5628 (2013)